AN INDUCTIVE POSITION SENSOR ASIC

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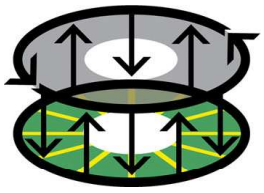
Abstract

A principle and realization of an ASIC for a fast, precise, and high resolution Contact-less Inductive Position Sensor (CIPOS), is described.

The inductive contact-less sensor is suitable for angular or linear position sensing. Advantage of used measurement principle is, that it is strictly ratio metric independent of absolute values. The mechanical robustness, insensitivity to temperature variation, electrical or magnetic fields as well as its mechanical tolerances make the sensor ideal for harsh automotive environment. The sensor fulfils all the requirements for safety relevant applications. The presented ASIC includes sensor excitation, precise input signal analog and digital processing as well as the output signal transmitter. The signal path and main blocks are described.

1. Introduction



CIPOS logo

Today the automotive industry demands position sensors on many different places, e.g. accelerator pedal sensors, turbocharger actuator systems, steering angle sensors, throttle body position sensors, gear box control position sensors, head lamp position sensors, etc. Traditionally these sensors were equipped by potentiometers, which have all the reliability disadvantages of mechanical contact sensors (wear out, open contact etc.). In the

modern cars these potentiometers are replaced by electronic contact-less sensors which are based on different principles: Hall sensors, magneto-resistive sensors or inductive sensors.

The main advantages of inductive sensors for automotive applications are their mechanical variability (linear, rotational, arc segment, axis can go across the sensor,...), high temperature range, simplicity and robustness.

This paper describes an inductive positioning sensor system, consisting of a sensor, developed by Hella KG Hueck & Co, and a sensor ASIC, developed by AMI Semiconductor.

2. Inductive sensor principle

The inductive contact-less sensor consists of a stator and a rotor or cursor. (Fig. 2, 3, 4) The stator contains an excitation coil (which is part of an LC resonance network), receiver coils and electronics for signal processing. The rotor or cursor is a passive element with one closed winding which is designed in a special geometry (Fig. 2, 3, 4).

The inductive coupling between the excitation coil, the rotor or cursor and the three receiver coils leads to 3 ratio-metric signals that are dependent on the angular rotor or linear cursor position (Fig. 3 & 4). By the means of analog and digital signal processing, a signal, linearly dependent on the rotor/cursor position is extracted.

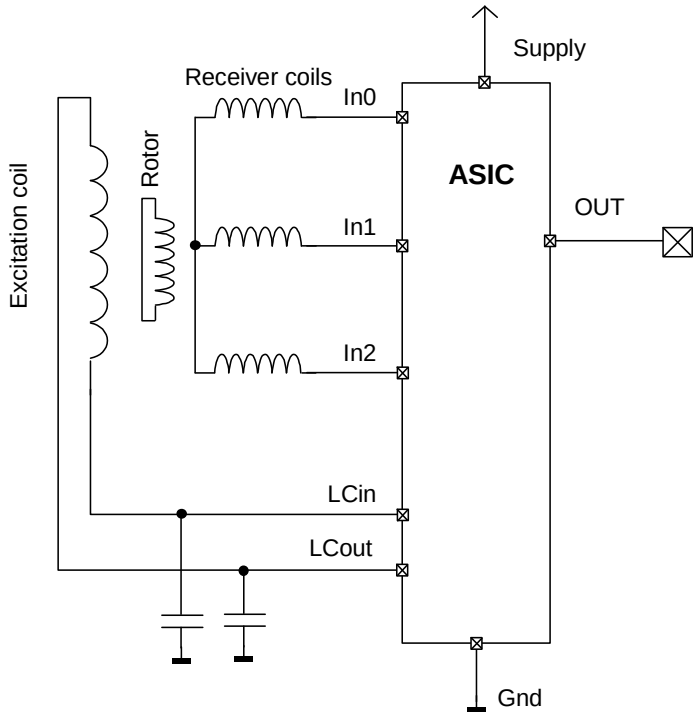


Fig. 1 Simplified application schematic

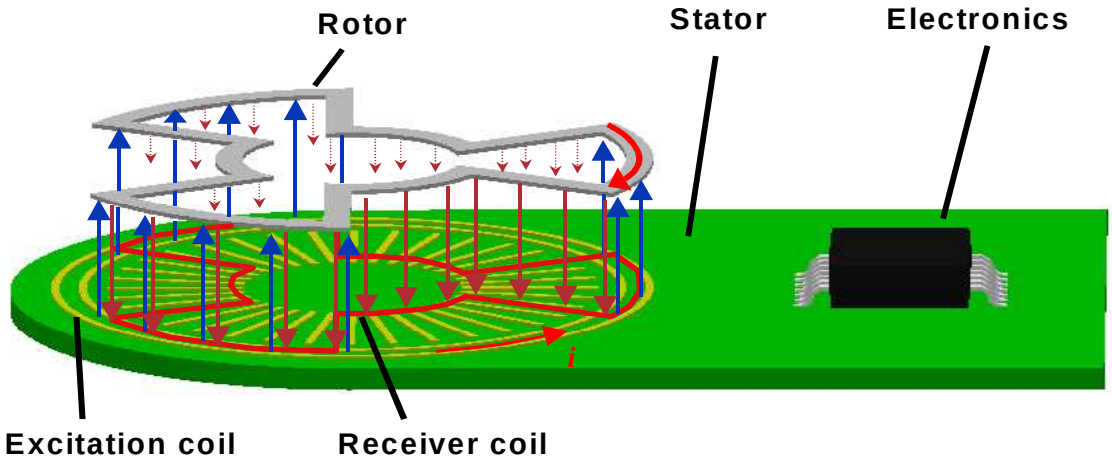


Fig. 2 Rotational sensor principle

An application schematic is shown in Fig. 1 and inductive rotational sensor principle is shown in Fig. 2.

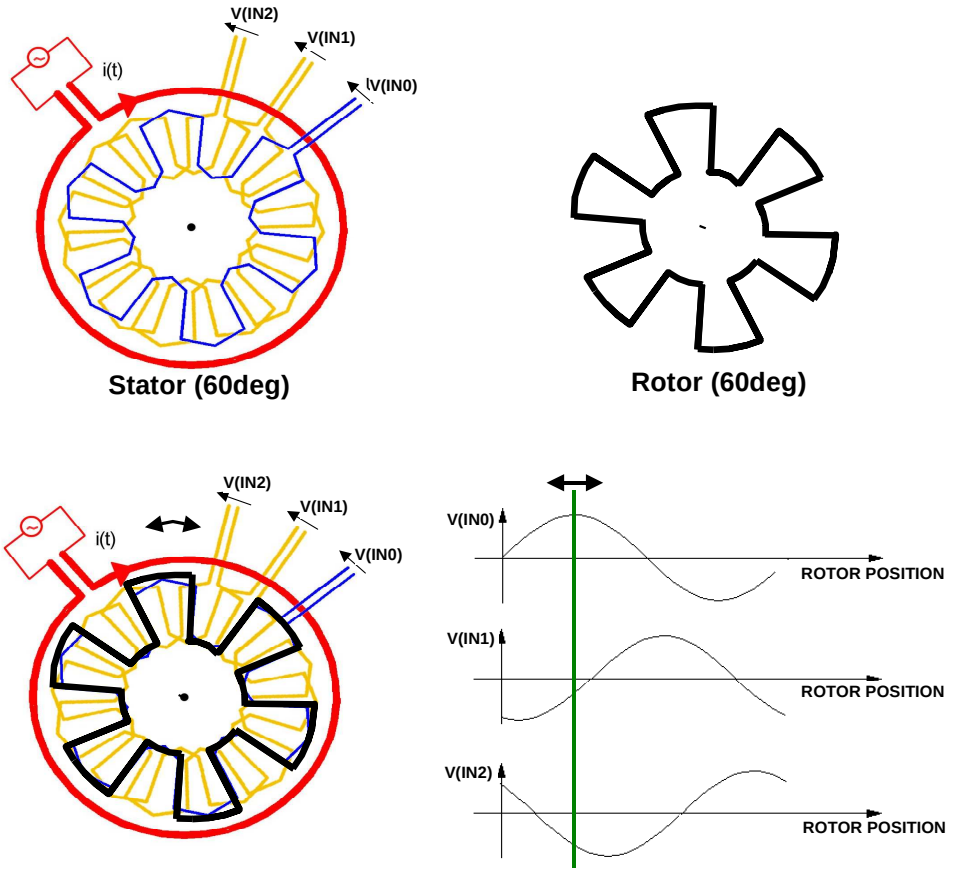


Fig. 3 Rotation sensor - output signals

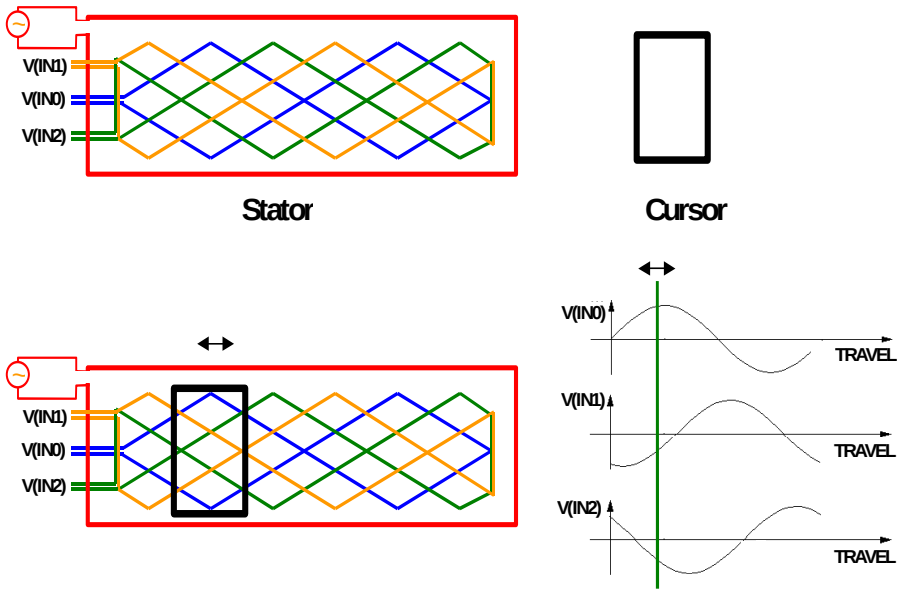


Fig. 4 Linear sensor - output signals

Different rotor/stator constructions allow to build 360, 180, 120, 90, 60,…. degree rotational sensors to adjust the sensor to the required angle range.

3. System description

The block diagram of the inductive sensor positioning ASIC, responsible for all the necessary signal processing, is shown in Fig. 5. The signal path is highlighted.

The LC oscillator driver [4] is used to drive the excitation coil of the sensor. The coil has to be driven with a harmonic current and to minimize the current consumption of the coil driver, the coil is a part of the LC resonance circuit and the driver has only to deliver the losses in the resonance circuit. The LC oscillator is further described in chapter "Oscillator driver".

Outputs of the sensor coils are IN0, IN1 and IN2 signals. Their amplitude depends on the rotor position. The IN0, IN1 and IN2 signals are first band limited by the Low Pass EMC filters to limit the high superposed EMC voltage on all INx pins to ensure low EMC susceptibility. Next, controlled by the digital, the proper combinations of input signals INx are selected in the analog multiplexer.

To create a DC signal from the AC input signal, a synchronous rectifier is used. The gain of the rectifier is a cosine function of the phase shift. Hence the phase shift between the Clock and the signal on the rectifier input is crucial as well as the Clock duty cycle. A very fast clock comparator with short, symmetrical delays is used.

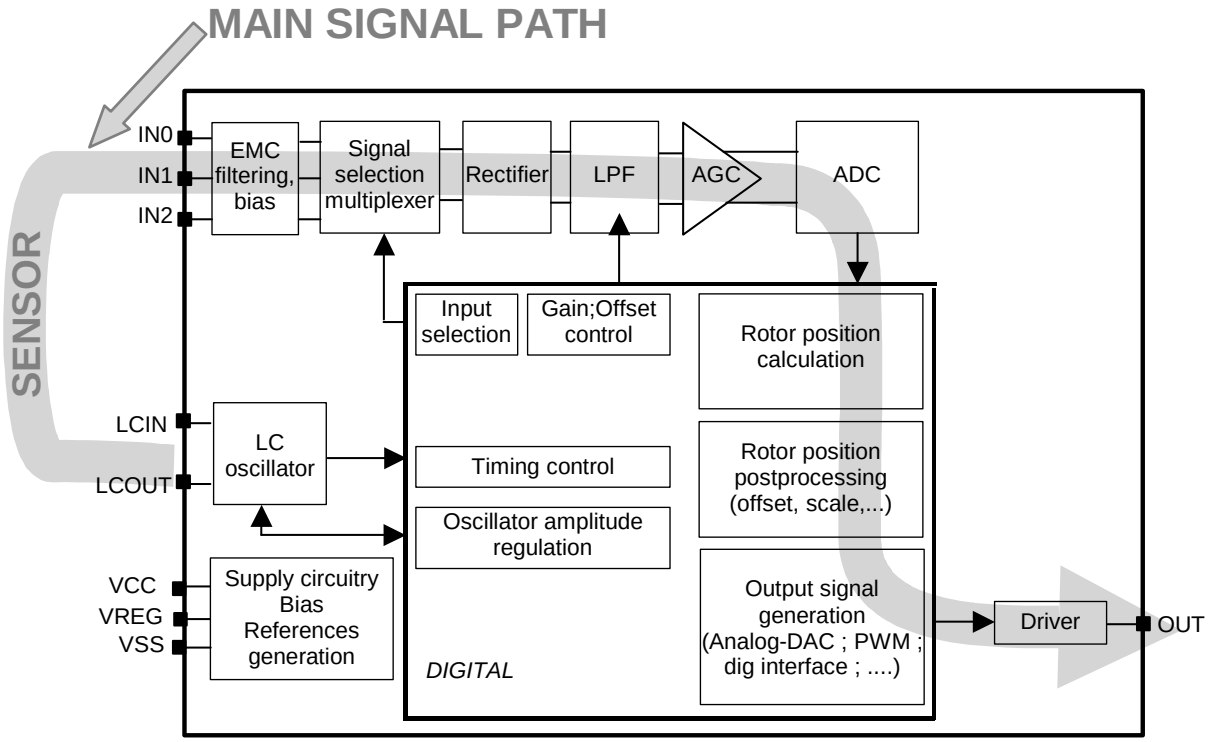


Fig. 5 ASIC block diagram

The second and higher order harmonics from the rectifier and remaining AC common mode signal are filtered by a combined differential/common-mode Low Pass Filter (LPF). The resulting DC signal is in the order of a few mV. Its amplitude varies significantly due to mechanical construction and mechanical tolerances (rotor to stator air gap).

To handle such a signal a high performance automatic gain control block is required [5]. A three stage Automatic Gain Control (AGC) block is implemented as shown in Fig. 6. The AGC gain is continuously adjusted by a finite state machine (FSM) at the end of each rotor position calculation to fully utilize the ADC input voltage range.

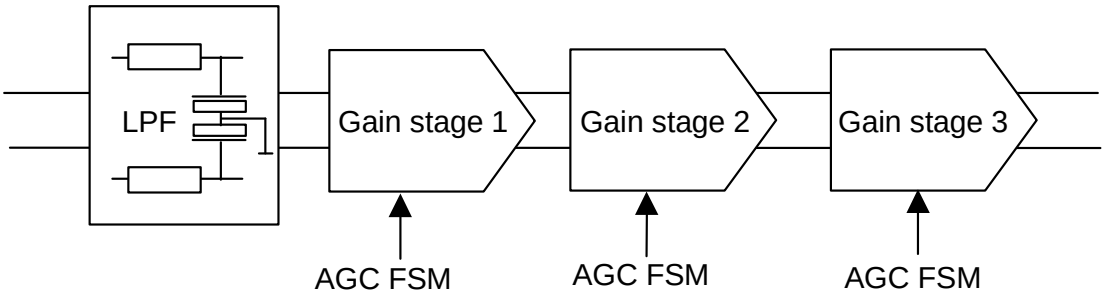


Fig. 6 AGC- gain control stage

Single ended input signal processing typically limits the resolution to 10 bits or 60dB Signal to Noise Ratio (SNR) due to the noise penetrating into the analog circuitry from the digital. This system is based on differential signal processing and achieves a resolution >12 bits.

The presence of a high amplitude common mode signal on the input results in the requirement for a high Common Mode Rejection Ratio (CMRR). This is achieved by full symmetry of the input amplifier (both schematic and layout). To meet the application requirements, the gain stage has to be fully differential, with very small gain non-linearity, high input and output signal dynamic range, high (preferably infinite) input impedance, very high CMRR and small offset. Because the gain stage is also used as a input stage of the connected ADC, high Slew Rate (SR) and gain bandwidth is required. The performance of the gain stage is key for the performance of the whole system and is further discussed in chapter “Automatic Gain Control”.

The analog output signal of the AGC stage is converted into a digital signal by a 12bit second order Sigma Delta converter. Further signal processing to calculate the rotor position is done by a custom DSP block.

The digital position signal is transmitted as an analog signal ratio metric to supply voltage or as a PWM signal or as a digital signal.

3.1 Redundancy requirement for safety relevant applications

For safety relevant applications, a redundant configuration with two independent systems is required. The inductive sensor can be configured as fully redundant. In this configuration, each system has it's own fully galvanic separated excitation coil and its own set of receiving coils. The rotor structure is shared. Each system provides independent output signal. The redundant system application with two excitation coils is shown in Fig. 7.

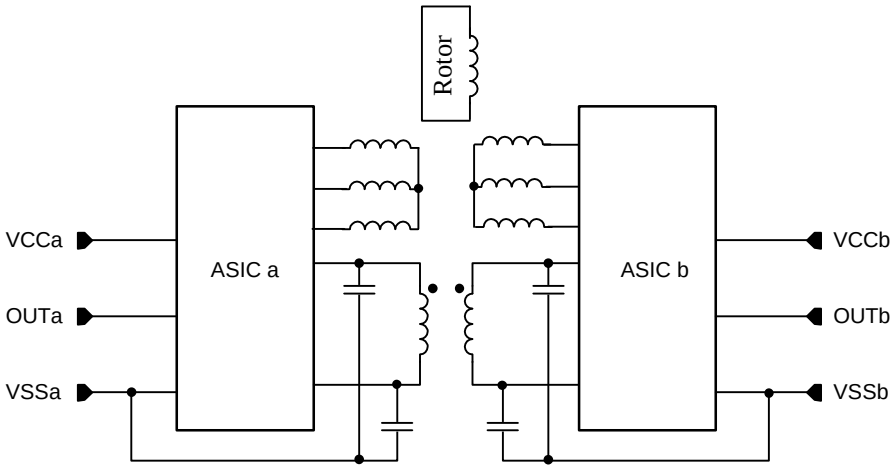


Fig. 7 Redundant application with two excitation coils.

In redundant systems with two excitation coils, the mutual inductance is not negligible (as indicated by the coil coupling in Fig. 7). In the case one of the two systems is not supplied e.g. due to failure on the supply lines, the not supplied ASIC may not overload the other ASIC oscillator. A special oscillator design is required to fulfill this requirement (chapter “Oscillator driver”).

For diagnostic purposes, the oscillator amplitude has to be measured. For this measurement the available Sigma Delta converter is used and the oscillator signals are connected to the ADC inputs with CMOS switches. As seen in Fig. 8, normal CMOS switches have parasitic diodes to ground and supply. These diodes can clip the oscillation amplitude for signal amplitudes >2VBE and short circuits the excitation coil of a system with a failed supply. In this case, the electro-magnetic field induced into the excitation coil of the failing system by the other working ASIC is likely to have an amplitude higher than two diode voltages due to the high mutual inductance between the two excitation coils. The short-circuit on the failing systems coil will disturb/overload the oscillator of the still supplied ASIC.

A special, over supply voltage tolerant pass-gate has to be used in this case. This is described in the next point.

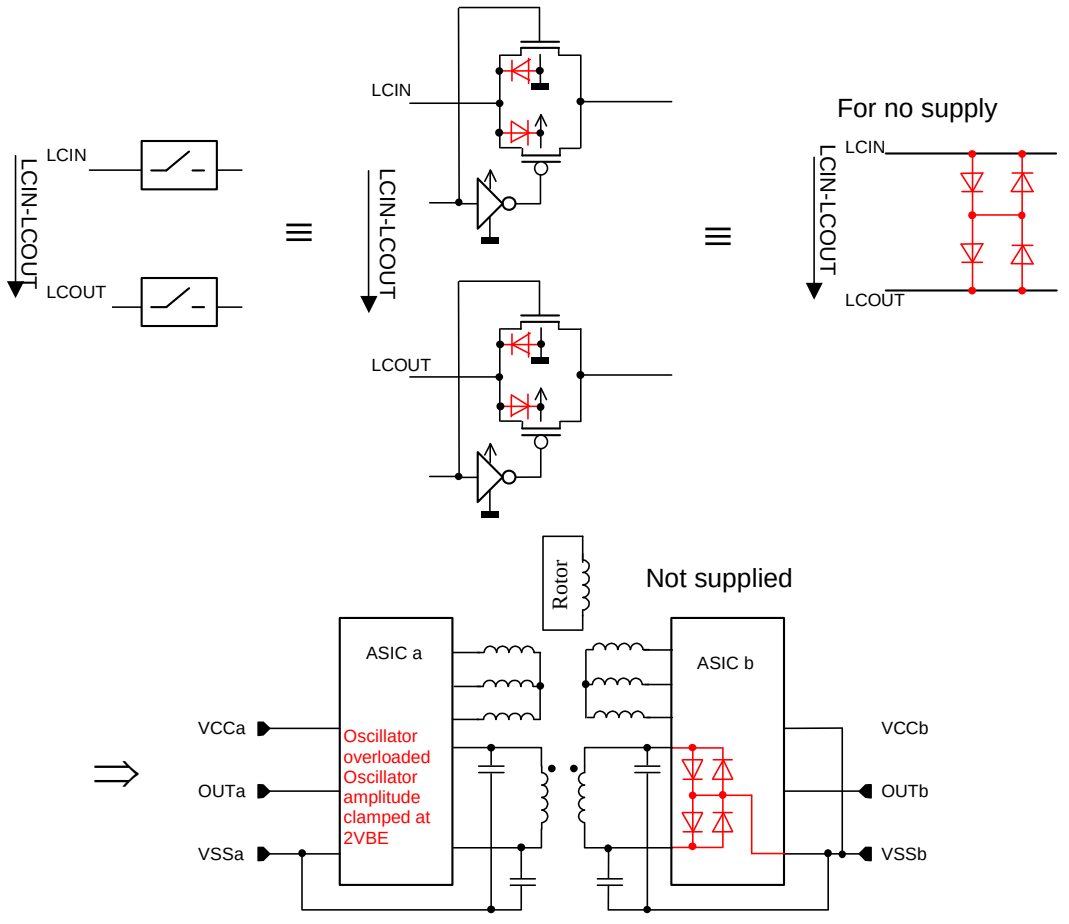


Fig. 8 Oscillator load of not supplied ASIC

The measurement path is always high impedant and does not cause any additional oscillator clipping in the redundant system.

3.2 Over-supply voltage tolerant pass-gate

To avoid interference when the supply is missing, over supply voltage tolerant pass-gate has to be used. Fig. 9 depicts a possible version of the over supply voltage tolerant pass-gate, that prevents undesired interaction through mutual inductance for negative DC shifts.

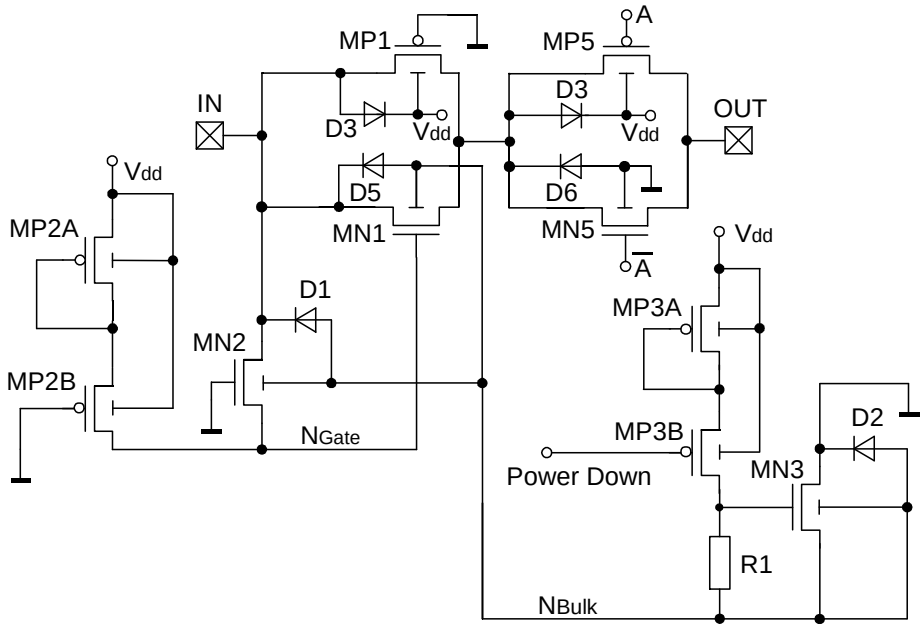


Fig. 9 Negative DC shift tolerant pass-gate

The NMOS of the CMOS pass-gate (MN1 and MP1) has a separate gate and bulk driving circuit, which prevents the build-in bulk-source diode D1 to conduct if the supply of the circuit is failing. If the supply is present ($V_{DD} > 2\ V_{Th}$), the node NGate is biased to $V_{DD} - V_{Th}$ through the transistors MP2A and MP2B. If Power Down is off, the node NBulk is forced to the ground level by transistor MN3 since the gate of transistor MN3 is forced above one threshold voltage thanks to resistor R1 and transistor MP3A and MP3B. The signal Power Down can be replaced by VSS if power down is not required. The switch MN1 is ON with its gate high and its bulk connected to ground. MP3A and MP2A are diode connected and are used to increase the voltage on V_{DD} for which the pass-gate is negative voltage tolerant. On the other hand, it decreases the dynamic range on the input by lowering MN1 gate voltage on node NGate. MP3A and MP2A are optional and can be removed.

If the supply is missing, (i.e. $V_{DD} < 2\ V_{Th}$) both MP2B and MN3 are switched off. The node NBulk (in the considered technology, the n type transistors are in a floating p-well which is not connected to the substrate or ground level) will

follow Vin (the parasitic capacitor at node NBulk will be discharged by D1). The voltage at node NBulk will be limited to min(Vin + V_{BE1}, V_{BE2}) where V_{BE1} and V_{BE2} are the built-in voltages of D1 and D2. Indeed, if V(NBulk) > V_{BE2}, the diode D2 is forward biased and NBulk is discharged through D2. The same happens through D1 if V(NBulk) > Vin + VBE1.

If Vin decreases below the ground level by more than one threshold voltage, the transistor MN2 is activated and the node NGate is forced to Vin, MN1 remains OFF. Node NBulk is floating and only capacitive discharging current flows through diode D1.

In summary, in case of missing supply, the input voltage will be allowed to drop below ground by more than 1 V_{Th} without creating a conductive path.

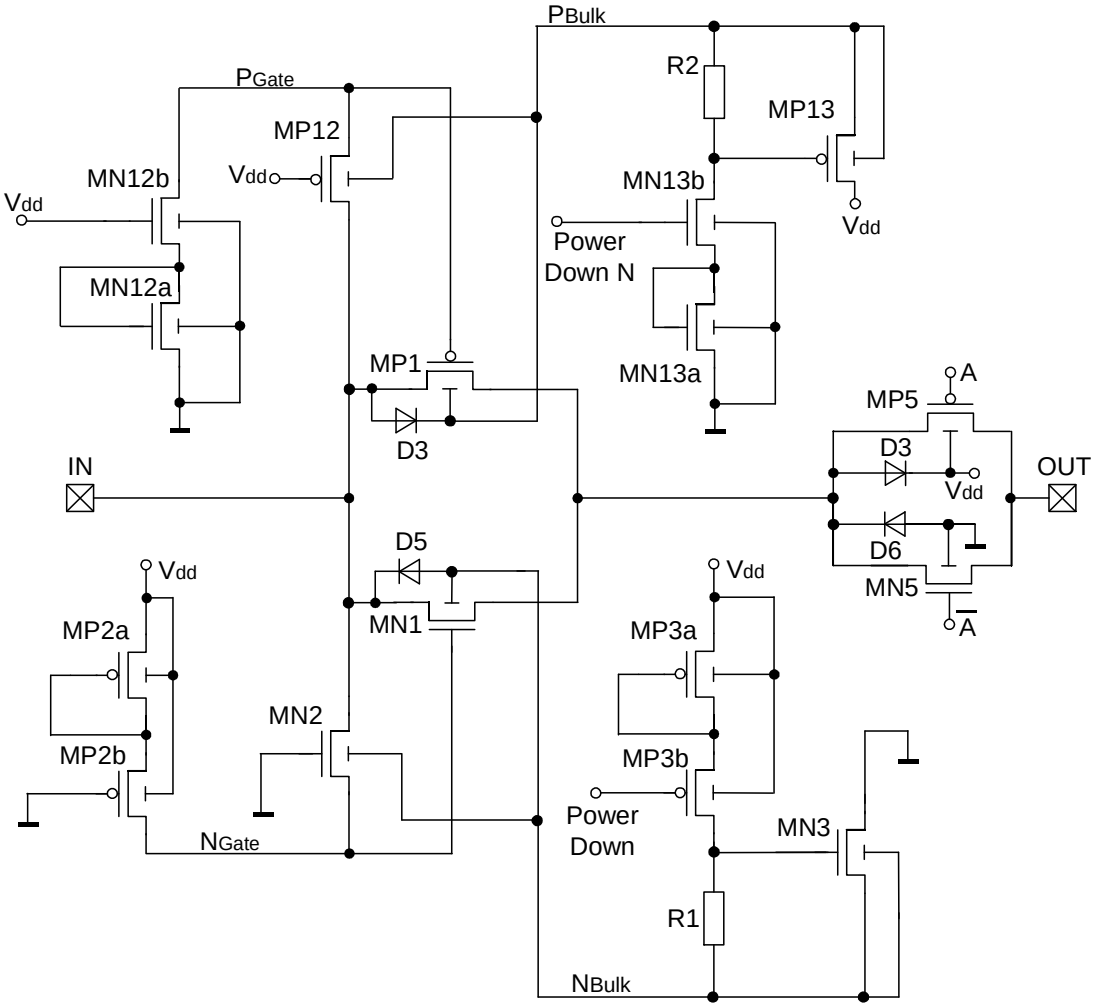


Fig. 10 Both positive and negative DC shift tolerant pass-gate

Out of the scope of the application, the described principle can be equally applied to a positive DC shift tolerant pass-gate (complementary structure to the negative DC shift tolerant pass-gate).

Combining both structures, a pass gate tolerant to both positive and negative DC voltages on the input in case of missing supply can be constructed as shown in Fig. 10.

3.3 Oscillator driver

A classical on chip oscillator driver with two transconductance Gm stages and off-chip RLC network, where all losses are represented by a serial resistance R_S, is shown in Fig. 11.

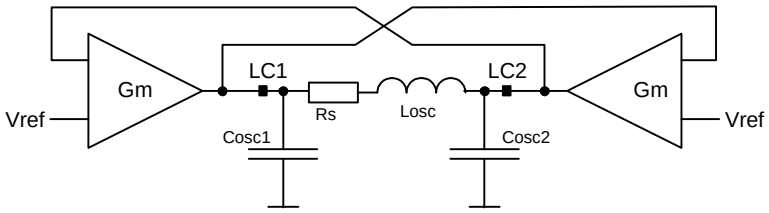


Fig. 11 Oscillator driver

Amplitude control

When we take for simplicity C = Cosc1 = Cosc2, then the oscillation condition (to keep stable oscillations) is

$$G_{m0} = R_S \cdot \frac{C}{L_{OSC}} = 2 \cdot \frac{R_S}{\omega^2 \cdot L_{OSC}^2} = \frac{1}{2} \cdot R_S \cdot \omega^2 \cdot C^2 \qquad (1)$$

To regulate the oscillation amplitude, non-linearity has to be inserted into the circuit. It can be created by limiting the output current of the drivers. The easiest approximation of the driver output current is shown in Fig. 12

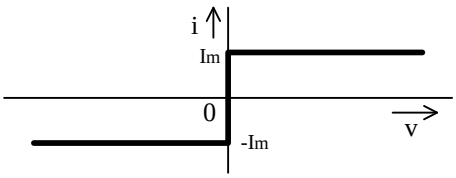


Fig. 12 Driver current (static)

Voltage of steady state oscillations is given by the formula (2)

$$V = 2k \cdot \frac{L_{OSC}}{C \cdot R_S} \cdot I_M = 2k \frac{I_M}{G_{m0}} \qquad (2)$$

Amplitude-voltage regulation is done by a digital control loop, which is controlling the maximum driver current.

$$\Delta V = 2k \cdot \frac{L_{OSC}}{C \cdot R_S} \cdot \Delta I_M = V \cdot \frac{\Delta I_M}{I_M} = V \cdot \delta I \tag{3}$$

A linear voltage step requires an exponential current control. The required exponential function is approximated by a PWL function.

Driver realization

The main challenges for the driver are a wide dynamic range of the output current and high speed (to limit losses the driver must be much faster than the oscillation frequency, which is typically 4MHz) [4].

The wide dynamic range of the output current (0:1984) is obtained by a current DAC and parallel switching of Gm output stages in the driver. Since the relative resolution is limited, instead of using linear 11-bit DAC an exponential type 7-bit DAC has been used. The full 7-bit scale of the DAC is divided into 8 ranges and in each of these ranges the output current step is constant (piece-wise linear approximation of exponential function) – see Fig. 13.

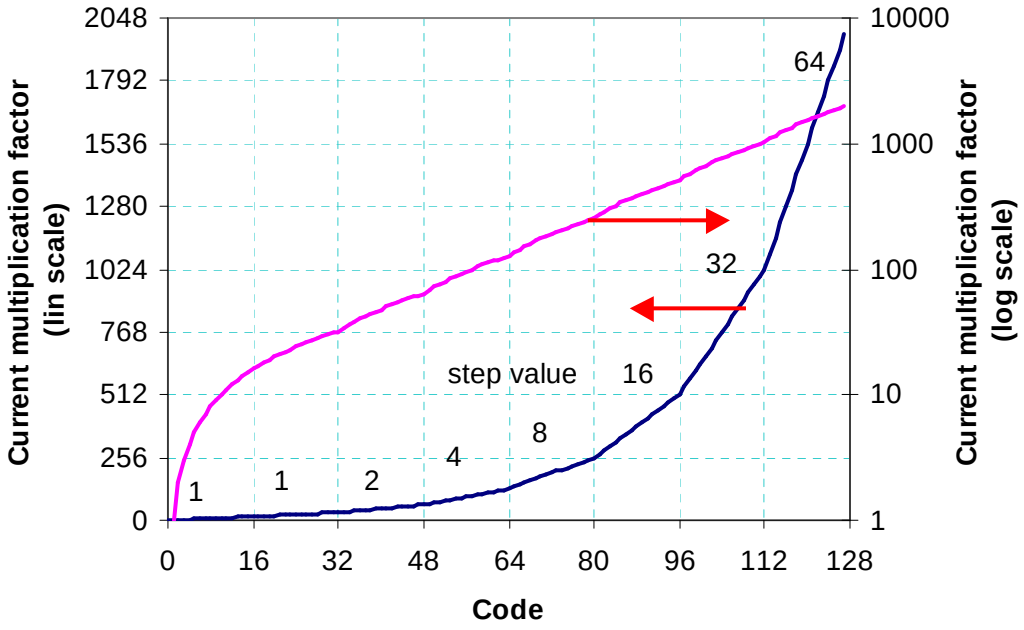


Fig. 13 Current multiplication for 7-bit PWL approximated exponential DAC

Simplified block diagram of the oscillator driver is shown in Fig. 14. It consists of a prescale block (with scaling factors 1, 2, 4 and 8) delivering current *Iref2* into two complementary current mirrors. Both top and bottom current mirrors consist of two parts – one with fixed current outputs of 16, 16, 32 and 64 times *Iref2* and a second part with a 7-bit binary weighted current DAC with output current from 0 to 127 *Iref2*. Oscillator Gm block integrates two functions. When

increasing the code, which increases current, it switches more fixed currents from top and bottom current mirrors to the output. The second function activates more output stages in parallel.

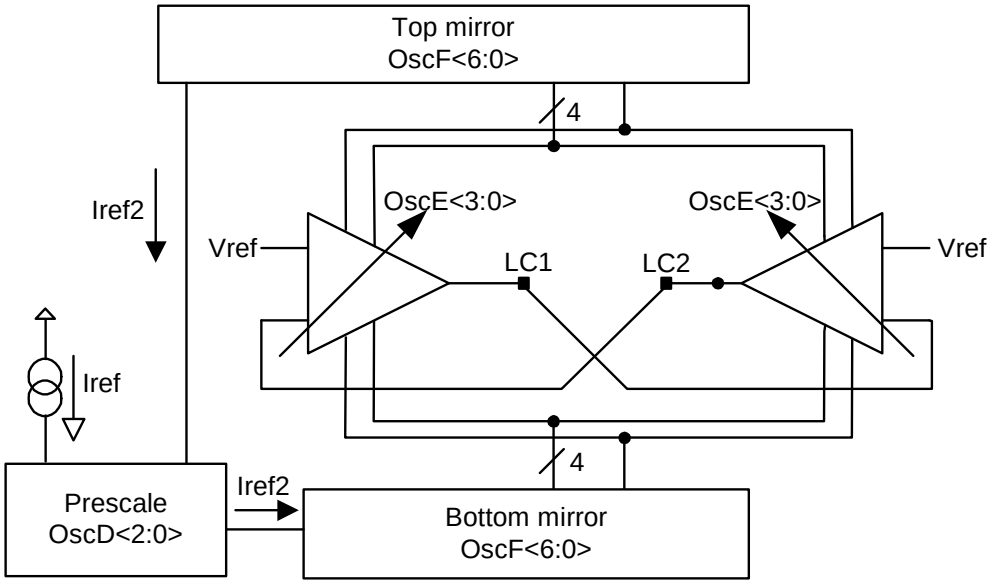


Fig. 14 Simplified diagram of oscillator current limitation

Table 1 Coding of driver control signals

DAC Segment	***7 bit input data B<6:0>***		***Prescaler output Iref2***	***Active Gm stages***	***Control Signal Codes***		
					Iref	***Ibias OTA***	***DAC***
-	***MSBs***	***LSBs***	***units***	**-**	***OscD <2:0>***	***OscE <3:0>***	***OscF<6:0>***
0	000	B3 B2 B1 B0	1	1	000	0000	0 0 0 B3 B2 B1 B0
1	001	B3 B2 B1 B0	1	2	000	0001	0 0 0 B3 B2 B1 B0
2	010	B3 B2 B1 B0	2	2	001	0001	0 0 0 B3 B2 B1 B0
3	011	B3 B2 B1 B0	2	3	001	0011	0 0 B3 B2 B1 B0 0
4	100	B3 B2 B1 B0	4	3	011	0011	0 0 B3 B2 B1 B0 0
5	101	B3 B2 B1 B0	4	5	011	0111	0 B3 B2 B1 B0 0 0
6	110	B3 B2 B1 B0	8	5	111	0111	0 B3 B2 B1 B0 0 0
7	111	B3 B2 B1 B0	8	9	111	1111	B3 B2 B1 B0 0 0 0

Setting of the current limitation is done using 3 independent control busses: prescaler bus OscD<2:0>, Gm-switching bus OscE<3:0> and current mirror bus OscF<6:0>. Simple logic is used to decode these oscillator control buses from the 7 bit input digital word. Table 1 shows how to generate the control signals. The output current can be calculated using following formula

$$I_{out} = I_{unit} \cdot (1 + OscD) \cdot \left[OscF + 16 \cdot \left\{ OscE \bmod 2 + \operatorname{int} \frac{OscE}{2} \right\} \right] \qquad (4)$$

Overdriving output without supply

In redundant systems with two drivers and two mutually coupled excitation coils if one of the systems looses supply or ground connection, it cannot load the other system, which must remain working.

The standard CMOS output driver (Fig. 15a) has intrinsically built in diodes, which will cause loading of the other oscillator if one system looses the supply voltage. Because the oscillator coil is floating, connected only to LCIN and LCOUT pins, it is sufficient to remove only one of the two diodes to prevent loading of the other system. In case an additional PMOS is used (Fig. 15b), the LCx pin can go negative, but the voltage range of the driver is limited (due to voltage needed to open MP1d).

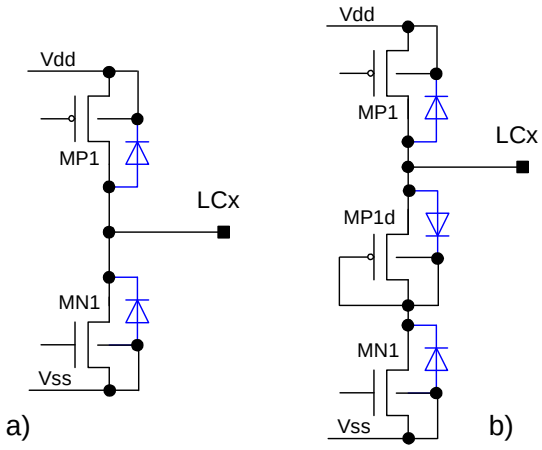


Fig. 15 CMOS driver topology

To allow the LCx pin to go negative when the supply voltage is lost and to not change the voltage range of the driver we use the circuit in Fig. 16. When the chip is powered on, transistor MP6 is on and node NBulk is shorted by MN6 to ground. To enable the driver, signals Ena and EnaN (inverted) are used.

Without supply, the voltage on Vdd is lower than 2 PMOS Vt needed to switch on MP6. MN6 is then off. For negative voltage on the LCx pin (below NMOS Vt) transistors MN5 and MN3 are on connecting Nbulk and Ng1 to LCx potential. This ensures that MN1 is off. All PMOSes connected to LCx potential are also off (MP1, MP3, MP4) and there is no current flowing through the LCx pin. For positive overdrive on LCx bulk diode of MP1 is activated. MP3 is used to increase potential on node Ng2 to cancel the current path through MP1 (Itop is common for both LC1 and LC2 drivers).

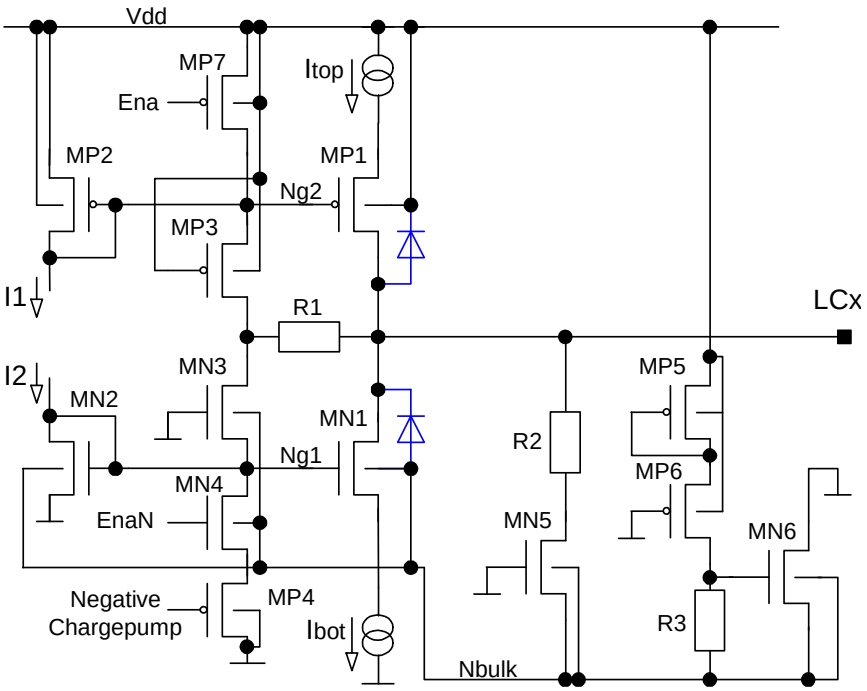


Fig. 16 Output driver topology

3.4 Automatic gain control stage

To accomplish the demanding requirements mentioned at the beginning of chapter three, a fully differential Current Feedback Amplifier (CFA) was used [5]. It provides symmetrical high impedance inputs, accurate and temperature stable gain, simple gain control and wide input dynamic range. Intrinsic input offset is comparable to common Voltage Feedback Amplifier (VFA) structures and is further reduced by build in offset compensation circuit. Typical VFA structures with resistor feedback either suffer from non-zero input current, high noise, limited SR or high input offset.

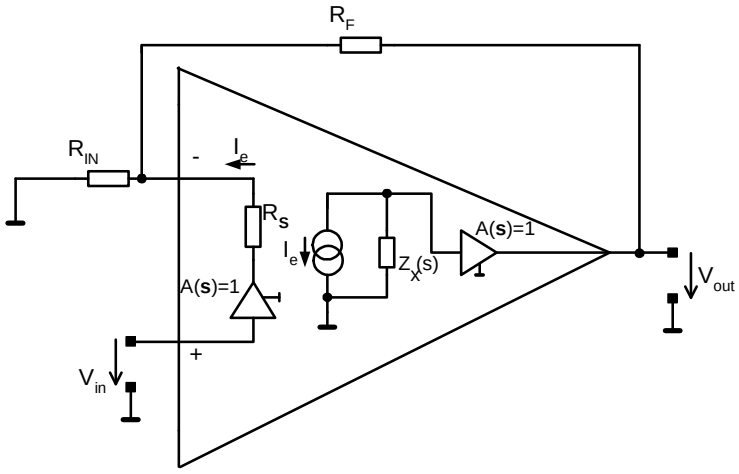


Fig. 17 Standard CFA structure

The standard CFA approach is shown in Fig. 17. The formula describing the gain of this structure is

$$A_{CL}(\mathbf{s}) = \frac{1 + \frac{R_F}{R_{IN}}}{1 + \left(R_F + R_S \left(1 + \frac{R_F}{R_{IN}} \right) \right) \frac{1}{Z_x(\mathbf{s})}} \tag{5}$$

Assuming $R_S = 0$ and $R_F << Z_x(s)$, we can simplify (5) to a form

$$A_{CL}(\mathbf{s}) = 1 + \frac{R_F}{R_{IN}} \tag{6}$$

The requirements of symmetrical high impedance inputs don't allow the direct application of the standard CFA structure. This can be solved by the use of differential CFA amplifier as described in Fig. 18.

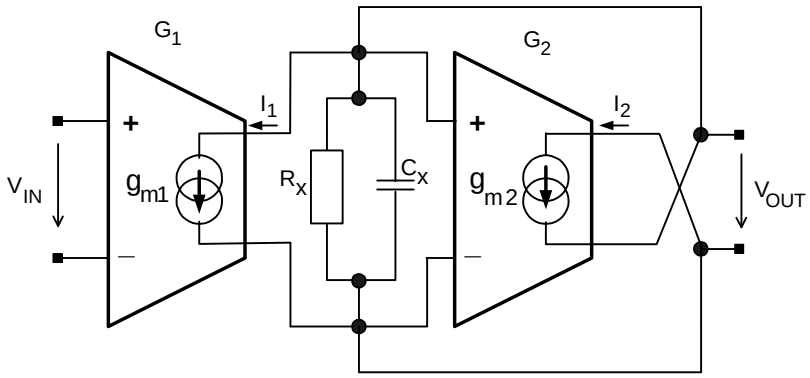


Fig. 18 Differential CFA model

The core is composed of two transconductances gm_1 and gm_2. The CFA gain frequency response is given by

$$A(s) = \frac{-g_{m1} R_X}{1 + g_{m2} R_X + s R_X C_X} \tag{7}$$

By proper design we can easily guarantee that $g_{m2}R_X >> 1$ and simplify (7) into form

$$A(s) = \frac{-g_{m1} R_X}{g_{m2} R_X + s R_X C_X} \tag{8}$$

From (7) is clear that the DC gain is

$$A_0 = -\frac{g_{m1}}{g_{m2}} \tag{9}$$

The main limitation of this topology for gain $A_0 \neq 1$ is the transconductance dependency of the degenerated differential pair on the input voltage amplitude. By a slight modification of the described topology (Fig. 18) we can obtain a gain stage for which the input voltage seen by g_{m1} and g_{m2}; for $g_{m1} = g_{m2}$ are equal even for $A_0 \neq 1$ and thus the transonductance dependences are canceled out. The topology is shown in Fig. 19.

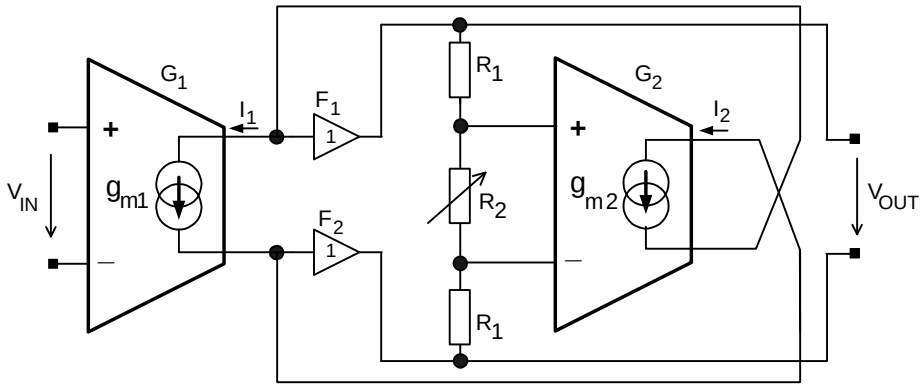


Fig. 19 Improved differential CFA model

The DC gain is

$$A_0 = -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{A_{Rdiv}} \tag{10}$$

where

$$A_{Rdiv} = \frac{R_2}{2R_1 + R_2} \tag{11}$$

For typical case with $g_{m1} = g_{m2}$ the equation can be even further simplified to

$$A_0 = -\frac{1}{A_{Rdiv}}. \tag{12}$$

Equation (12) for DC gain is exactly what is required for VLSI integration - the gain is defined by the ratio of two easily controllable parameters and is independent of its absolute value.

Practically, the gain accuracy can easily be within the range of ± 0.5% without extra trimming circuitry.

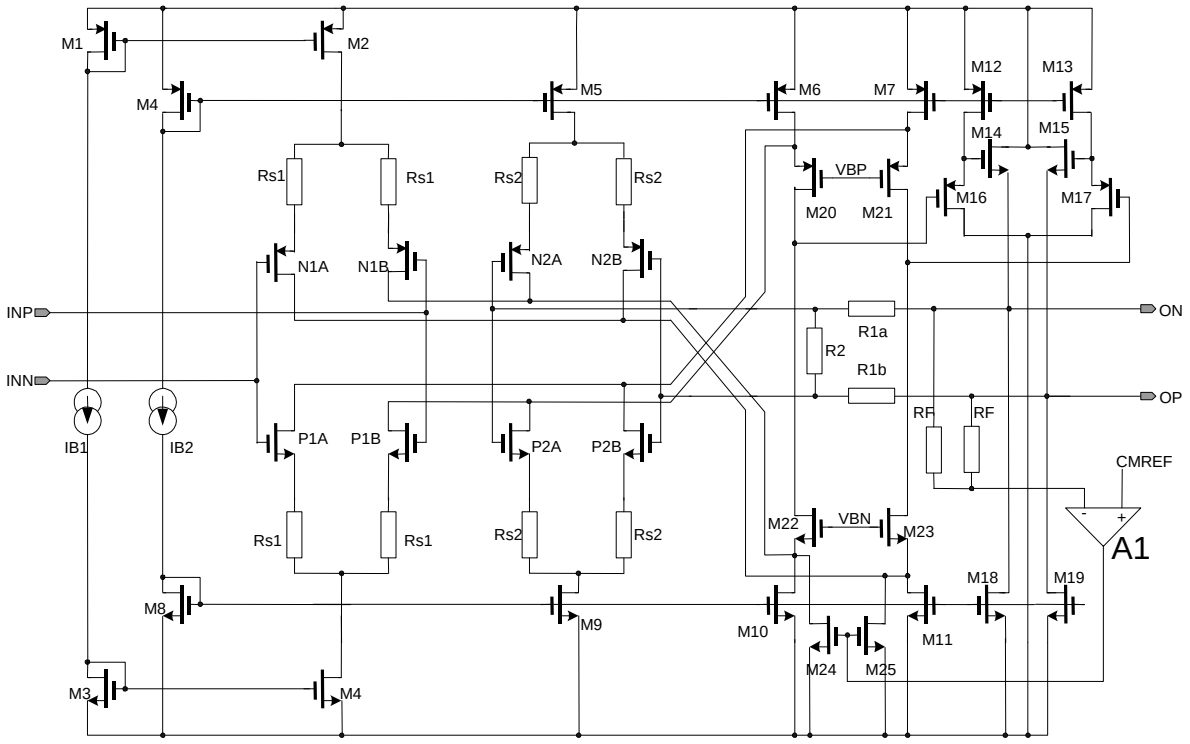


Fig. 20 Differential variable gain CFA

The simplified transistor level schematic is shown in Fig. 20. The structure consists of two complementary, degenerated differential pairs. The input complementary differential pair (N1A, N1B, P1A, P1B) realizes the g_{m1} and differential pair (N2A, N2B, P2A, P2B) realizes the g_{m2}. The folded cascode (M6, M7, M10, M11, M20-23) output impedance corresponds to R_X and C_X of the model (Fig. 18). The simple output followers are realized by M12-19. The gain is adjusted by resistor divider (R1a, R1b, R2). Common mode feedback circuitry (M24-25 , RF and A1) is only symbolically included.
The measured DC gain as a function of input signal amplitude for selected gain 1, 2, 4 and temperature -40°C to 160°C is shown in Fig. 21.

4. Sensor accuracy measurement results

For the evaluation of the full system a configuration with analog output driver ratio-metric to the supply was used. The performance evaluation suffers from the fact that it is difficult to distinguish between errors caused by the ASIC and errors caused by the sensor itself. The presented results cover the overall system performance from mechanical sensor to ASIC analog output.
The measurement results of a standard production system, which includes all imperfections of the sensor coil system and the imperfections and temperature drifts of the ASIC actuator/driver is shown in Fig. 22. The angular position error

remains below 0.1% over the whole input range of the sensor. The measured temperature drift of the full system including analog output drivers for the extended temperature range of -40degC to 160degC is also less than 0.1%. The total system has a maximum accuracy error of ±0.1%.

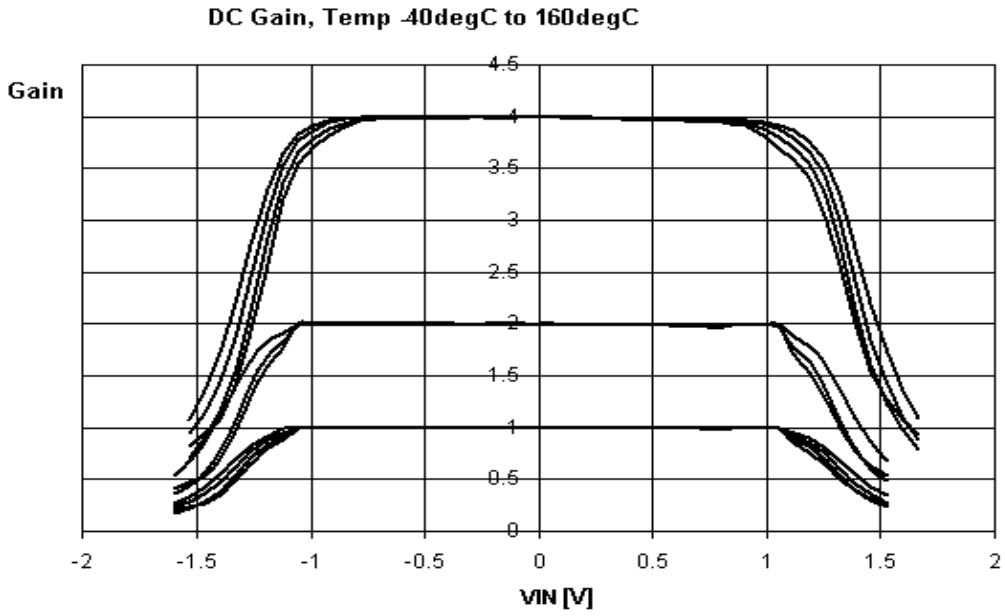


Fig. 21 Measured DC gains adjusted to 1,2 and 4 in temp. range-40 to 160 ℃

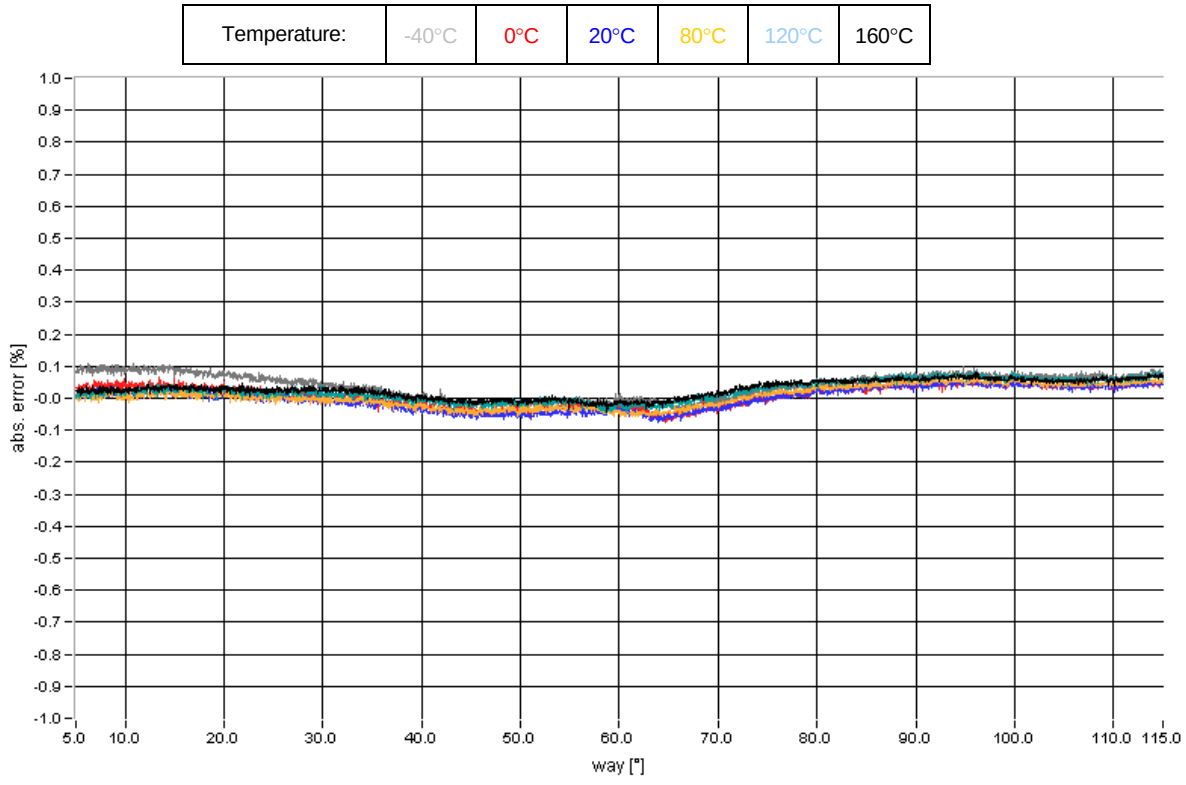


Fig. 22 System accuracy measurement, temperature drift -40ºC .. 160ºC, measured with standard production sensor

5. Hella's CIPOS Sensor: Typical Applications

Due to the particularly large flexibility for possible form factors, the CIPOS measurement principle is used in the automotive industry for very different products. In this section some of these are briefly introduced.

Fig. 23 shows two different forms of electronic accelerator pedals equipped with CIPOS sensors. One can see, depending on the structure concept, different shapes of the sensor are used. In the case of the hanging pedal (left photo) that is a segment sensor, in the case of the standing pedal (right photo) a linear sensor.

Fig. 23 Acceleration Pedals with CIPOS-Sensors

The sensors increasingly become also a component of other functional units. A nice example of it are the solenoid operated throttle valves as seen in Fig. 24 left and the headlamp swiveling module seen in Fig. 26 right.

Beside the spatial also the functional integration of sensors plays an important role in many cases. As an example an electro-powered actuator is shown in Fig. 25.

The electronics contains the stator of the sensor for the acquisition of the actual position of the drive lever, an ASIC for the evaluation of the sensor signals, a further ASIC with micro-controller and power-output stage for the motor control as well as the components for a CAN interface. The sensor thereby is not only spatial but also directly functionally integrated into the actuator electronics.

Fig. 24 CIPOS-Sensors in Throttle-Flap and a Headlamp Swivelling Module

Fig. 25 CIPOS-Sensor in an Actuator

6. Conclusions

The presented inductive position sensor provides a powerful solution, compared to other concepts, suitable for the harsh automotive environment. The sensor is very precise, with no contact between the moving part and the stator, it is especially well suited for use in applications with frequent sensor movements even if an exceptional accuracy is required.

The system is based on the sensors planar coils, one ASIC and few external components. The ASIC provides rotor position conversion rate up to 4k samples/sec. The system is fully operational within 5.5ms after supply connection, and consumes typically 8mA. For safety relevant applications, the sensor can be configured as a dual, fully redundant system. Each channel is fully galvanic separated and provides an independent output signal. Both systems share a common rotor structure. The system fulfills all the current automotive EMC requirements.

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