Molybdenum Gate Technology for Ultrathin-Body MOSFETs and FinFETs

Daewon Ha, *Member, IEEE*, Hideki Takeuchi, *Member, IEEE*, Yang-Kyu Choi, *Member, IEEE*, and Tsu-Jae King, *Senior Member, IEEE*

***Abstract*—Damage-free sputter deposition and highly selective dry-etch processes have been developed for molybdenum (Mo) metal gate technology, for application to fully depleted silicon-on-insulator (devices such as the ultrathin body (UTB) MOSFET and double-gate FinFET. A plasma charge trap effectively eliminates high-energy particle bombardment during Mo sputtering; hence the gate-dielectric integrity (TDDB, $Q_{\rm BD}$) is significantly improved and the field-effect mobility in Mo-gated MOSFETs follows the universal mobility curve. The effects of etch process parameters such as chlorine $(\rm Cl_2)$ and oxygen $(\rm O_2)$ gas flow rate, and source and bias radio frequence powers, were investigated in order to optimize the Mo etch rate and selectivity to $\rm SiO_2$. A highly selective etch process was successfully applied to pattern Mo gate electrodes for UTB MOSFETs and FinFETs without leaving any residue or stringers. Measured electrical characteristics and physical analysis results are discussed.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS), dry etching, FinFET, fully depleted silicon-on-insulator (FD SOI), molybdenum metal gate, sputter, ultrathin body.**

I. Introduction

In order to achieve improved circuit performance and reduced cost per function, the lateral dimensions of bulk-Si MOSFETs have been steadily scaled down, concomitantly with a reduction in gate oxide thickness and increase in channel doping to control short-channel effects. Quantum-mechanical tunneling through ultrathin gate oxides and carrier-mobility degradation due to high channel doping are issues which place limitations on bulk-Si MOSFET scaling, however [1], [2]. Recently, new transistor structures such as the ultrathin body (UTB) MOSFET and double-gate FinFET have been proposed to improve the scalability of the MOSFET, for CMOS technology generations beyond the 65-nm technology node [3]. Since an ultrathin silicon body can effectively suppress short channel effects (SCE), a lightly doped $(< 10^{16}\ \rm cm^{-3})$ or undoped body can be used in order to achieve high carrier mobilities for improved transistor drive current, as well as to minimize variations in threshold voltage (V_T) due to statistical doping variations [4]–[6]. A lack of body doping necessitates the use of gate work function engineering to adjust V_T, however. The range of work functions required for thin-body CMOSFETs is 4.4 V–5.0 V [7], ruling out polycrystalline silicon as a gate material.

In selecting alternative CMOS gate electrode materials, several factors must be considered. These include CMOS process compatibility (e.g., thermal stability during high-temperature annealing steps), impact on gate dielectric reliability, and extendibility with advances in technology (*e.g.*, high-k gate dielectric materials). Several material systems and process integration approaches for achieving multiple gate work functions have been investigated to date: dual metal (Ti/Mo) [8], metal (Ti/Ni) interdiffusion [9], metal alloying (Ru/Ta) [10], fully silicided $(\rm NiSi_{\it x})$ doped poly-Si [11], and tunable-work-function metal (Mo) gate [12], [13]. The tunable-work-function Mo gate technology offers the simplest process, which is advantageous for manufacturing. We have previously demonstrated that multiple values of V_T can be achieved on a single substrate for UTB MOSFETs [14] and FinFETs [15] by selective implantation into the Mo gate material with nitrogen.

This paper discusses various aspects of Mo gate process technology. In Section II, the process details for damage-free Mo sputtering and highly selective Mo dry etching are presented. In Section III, measured electrical characteristics and physical analysis results are discussed. In Section IV, conclusions are drawn.

II. Molybdenum Gate Processes

A. Mo Sputter Deposition

Physical vapor deposition (PVD) (as compared with chemical vapor deposition) provides an important advantage of minimal incorporation of impurities. A DC-magnetron sputtering system (Novellus M2i with Quantum Source) was used in this work to deposit the Mo gate films. This system has two load-lock stations, a wafer degas station, as well as a cooling station. The base pressure of the sputtering chamber is maintained below 5×10^{-8}, and argon (Ar) gas was used for Mo target sputtering. Mo films with 50–150-nm thickness were deposited at 200 °C with 10-mTorr process pressure and 300-W power.

The critical requirements for a gate deposition process are: zero damage to the gate dielectric and good step coverage for nonplanar transistor structures such as the FinFET. Sputtering damage can result in degraded gate-oxide integrity (GOI) and transistor drive current due to degraded field-effect carrier mobility. Damage can be minimized by eliminating high-energy

Manuscript received June 8, 2004; revised October 11, 2004. This work was supported in part by the MARCO Focus Center on Materials, Structures, and Devices, funded by the Massachusetts Institute of Technology, in part by MARCO under Contract 2001-MT-887, and in part by DARPA under Grant MDA972-01-1-0035. The review of this paper was arranged by Editor C.-Y. Lu.

D. Ha, H. Takeuchi, and T.-J. King are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: deawon@eecs.berkeley.edu).

Y.-K. Choi is with the Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology, Daejeon, Korea.

Digital Object Identifier 10.1109/TED.2004.839752

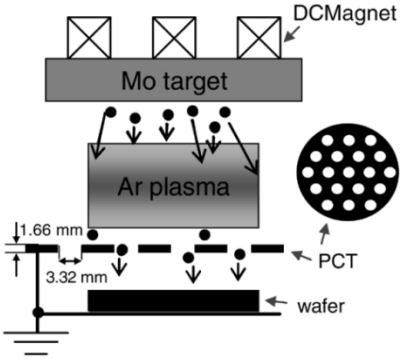


Fig. 1. Schematic of the sputtering chamber with a PCT, which is made of 1.66-mm-thick stainless steel and has arrays of closely packed 3.32-mm-diameter round holes (40.3% aperture area). Sputtering damage can be minimized with the electrically grounded PCT by collecting high-energy ions.

particle bombardment during deposition by interposing an electrically grounded plasma charge trap (PCT) between the Mo target and the wafer; separating the plasma excitation and Mo film deposition [30]. Fig. 1 shows a schematic of the sputtering chamber with the PCT, which is made of 1.66-mm-thick stainless steel and has arrays of closely packed 3.32–mm-diameter round holes (40.3% aperture area). Since the PCT is electrically grounded, it collects high energy ions, as well as a fraction of the neutral Mo atoms which are traveling toward the cathode/sample plane. These particles are deposited onto the PCT, and hence are not deposited onto the wafer surface. Thus, the deposition rate with the PCT is reduced by about 70%, which is roughly proportional to the PCT aperture area.

To investigate the efficacy of the PCT for reducing/eliminating sputtering damage, bulk-Si p-channel MOSFETs were fabricated with Mo gates deposited either with or without the PCT using a conventional gate-first process. Damage to the gate dielectric can be assessed by measuring the gate leakage current density and gate-dielectric lifetime. Gate leakage current densities for Mo-gated PMOS capacitors are compared against those of p^+ poly-Si-gated PMOS capacitors (control samples) in Fig. 2 [16]. The p^+ poly-Si gated devices show a large variation in gate leakage current due to boron penetration. The Mo-gated devices have lower gate leakage with much tighter distributions; the PCT provides $\sim 30\%$ lower gate leakage, even though the electrical stressing condition is more severe than for the control samples, due to the lower (more negative) threshold voltage of the Mo-gated devices; -1.04 V, -1.03 V, and 0.07 V for with and without PCT Mo gate, and p^+ poly-Si gate, respectively. Time Dependent Dielectric Breakdown (TDDB) and Charge-to-Breakdown $(Q_{\rm BD})$ were measured, and are shown in Fig. 3 [16]. The measured transistor gate area is 150 $\mu{\rm m}^2$. For the $Q_{\rm BD}$ measurements, the devices were biased at a constant gate voltage $+4.4$ V. Since the devices have the same threshold voltage, the effective stressing condition is the same for both groups of samples. Note that breakdown of thinner gate oxide occurs by bulk trap generation, not by interface trap generation, and is therefore driven by gate voltage [25]. With PCT Mo sputtering, the gate oxide integrity is significantly improved; indicating that low sputtering damage to gate dielectric is achieved. Fig. 4(a) shows the measured I_D–V_D characteristics of Mo-gated bulk-Si p-channel MOSFETs. The drive current achieved with a PCT sputtered Mo gate is higher due to improved hole mobility as shown in Fig. 4(b), which matches the universal mobility curve. The improved hole mobility is attributed to reduced interface traps (Q_{it}) and/or fixed charge (Q_f) due to the damageless Mo gate sputtering process [16].

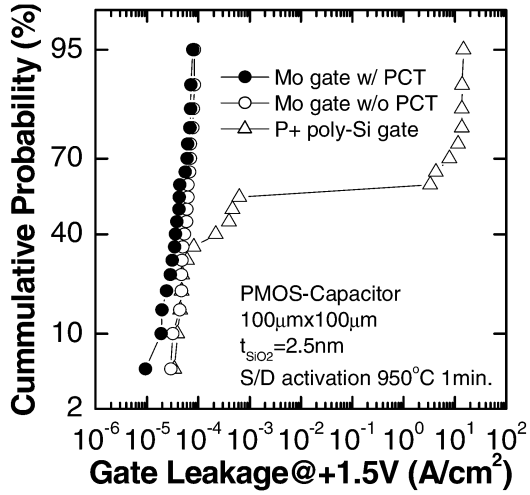


Fig. 2. Measured gate leakage current densities of Mo-gated and p^+ poly-Si gated p-channel MOS capacitors.

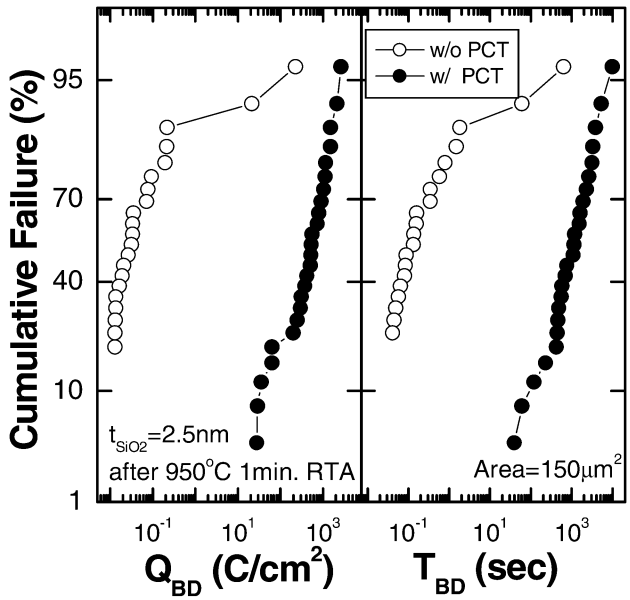
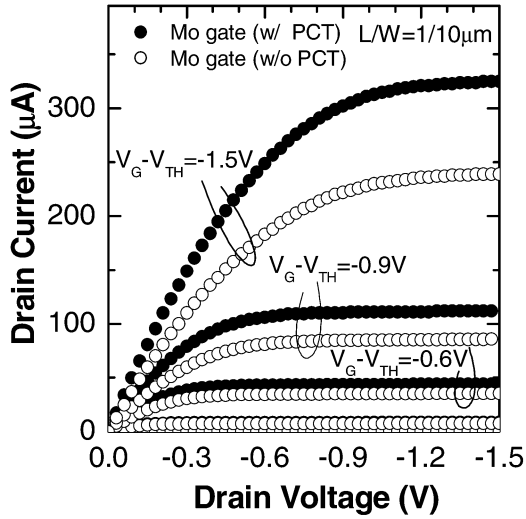


Fig. 3. Measured charge-to-breakdown $(Q_{\rm BD})$ and time dependent dielectric breakdown (TDDB) of Mo-gated p-channel MOSFETs. With PCT Mo sputtering, the gate oxide integrity is significantly improved, indicating that low sputtering damage to gate dielectric is achieved.

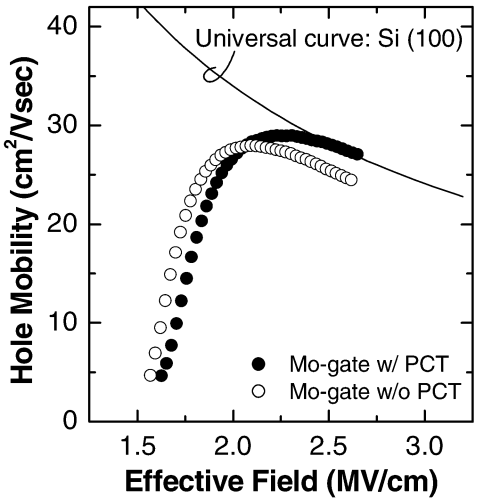
B. Mo Dry Etching

A Transformer Coupled Plasma etcher (LAM Research TCP 9400) was used to etch the Mo gate films. There are two RF power (source, bias) supplies running at the same time during the etching process, which results in a high-density plasma with adjustable substrate bias.

The critical requirements for a gate etch process are: high selectivity to the gate dielectric (SiO_2) and vertical etched profile. Fig. 5 shows the minimum etch selectivity required, as a func-



(a)



(b)

Fig. 4. (a) Measured I_D–V_D characteristics. (b) Measured effective hole mobility of Mo-gated p-channel bulk-Si MOSFETs.

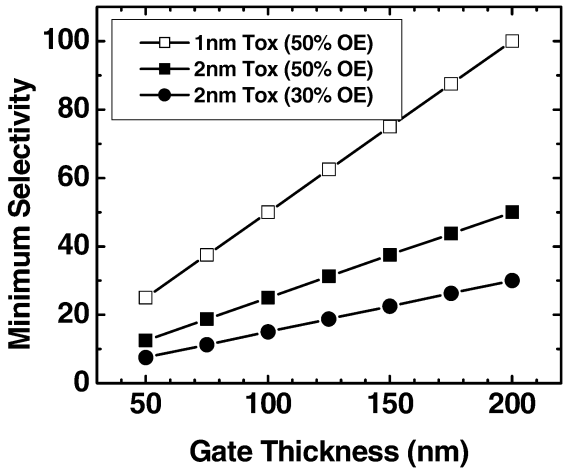


Fig. 5. Minimum etching selectivity required as a function of gate stack thickness.

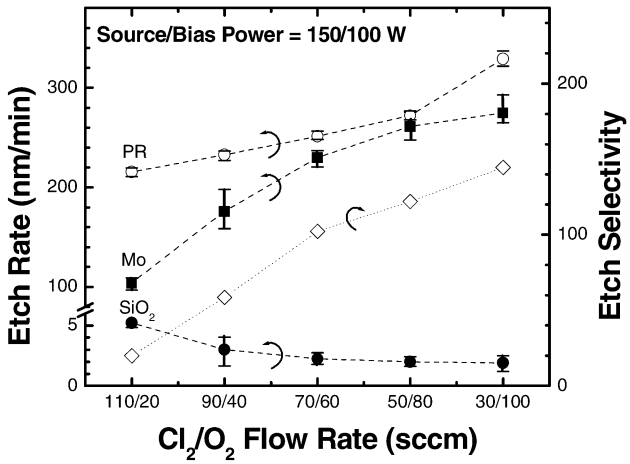


Fig. 6. Etch-rate dependences of Mo, SiO_2, and photoresist (PR) on the oxygen partial pressure in the Cl_2/O_2 gas mixture. The total flow rate was held constant at 130 sccm, and the process pressure was 13 mTorr with 150 W/100 W source/bias RF powers.

tion of gate stack thickness. For example, the etch selectivity must be higher than 25:1, assuming that the thicknesses of the Mo gate and SiO_2 gate oxide are 100 and 2 nm, respectively, and 50% over-etch. Since fluorine (F) and chlorine (Cl) radicals each etch Mo at an appreciable rate, it is possible to use either F-based or Cl-based etching gases such as CF_4, CF_3Cl, Cl_2, and so on [17]. Fluorinated carbon compounds (CF_4, CF_3Cl), which may attack the gate dielectric (SiO_2) [18], are precluded due to the selectivity requirement. We focused on the use of a Cl_2/O_2 gas mixture in this study; the dependences of etch rate and selectivity to SiO_2 on Cl_2/O_2 gas flow rate, source and bias RF powers were investigated.

Fig. 6 shows the dependences of the etch rates of Mo, SiO_2 and photoresist (PR) on the oxygen partial pressure in a Cl_2/O_2 gas mixture. The total gas flow rate was held constant at 130 sccm, and the process pressure was 13 mTorr with 150 W/100 W source/bias RF powers. With sufficient chlorine and oxygen radicals, the addition of oxygen gas increases the Mo etch rate and decreases the SiO_2 etch rate, and hence improves the selectivity. This implies that the surface of Mo can be easily oxidized and reacted with chlorinated gas to sublimate at $\sim 100^\circ$ C in the form of molybdenum oxychlorine (MoO_xCl_y) [19]. Note that more than 75% oxygen results in significant etching of PR, which may prevent PR from being used as a masking material.

Fig. 7 shows the Mo and SiO_2 etch-rate dependences on source power with constant gas flow rate $(Cl_2/O_2 = 70/60\ \mathrm{sccm})$, process pressure (13 mTorr), and bias power (100 W). The etch rates of Mo and SiO_2 increase linearly with source power because more chlorine and oxygen radicals are available, but the selectivity decreases due to the faster increase in SiO_2 etch rate. For source power below 150 W, the etch rate of SiO_2 is constant due to the DC self-bias voltage, so that the etch selectivity is degraded.

Fig. 8 shows the Mo and SiO_2 etch-rate dependences on bias power with constant gas flow rate $(Cl_2/O_2 = 70/60\ \mathrm{sccm})$, process pressure (13 mTorr), and source power (150 W). The Mo etch rate saturates above 100-W bias power, whereas SiO_2 etching rate increases monotonically. Therefore, etch selectivity decreases with increasing bias power. This indicates that energetic ion bombardment does not always increase the Mo etch rate, and that chemical etching plays an important role. Note that the bond dissociation energy of SiO_2 is larger than that of Mo [20].

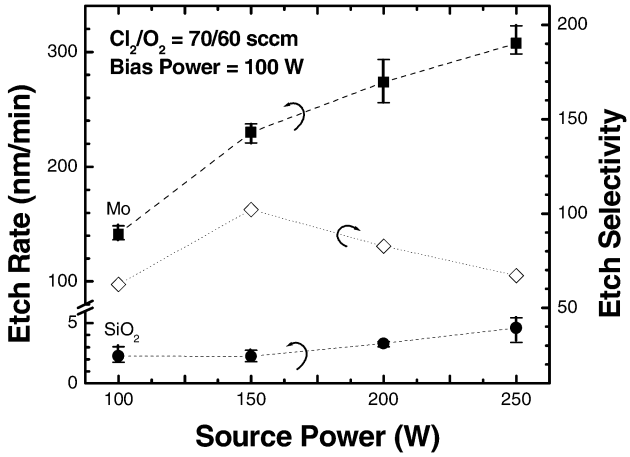


Fig. 7. Etch-rate dependences of Mo and SiO_2 on source power with constant gas flow rate ($Cl_2/O_2 = 70/60$ sccm), process pressure (13 mTorr), and bias power (100 W).

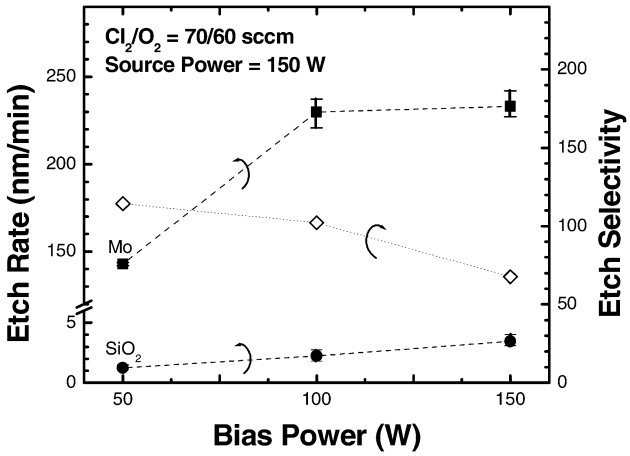


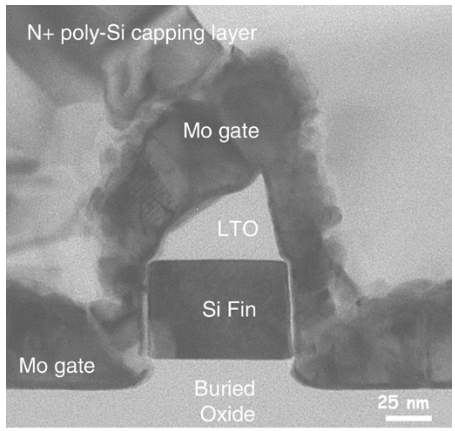
Fig. 8. Etch-rate dependences of Mo and SiO_2 on bias power with constant gas flow rate ($Cl_2/O_2 = 70/60$ sccm), process pressure (13 mTorr), and source power (150 W).

The Mo gate etch process conditions were thus optimized to be as follows: $Cl_2/O_2 = 70/60$ sccm, process pressure $= 13$ mTorr, source/bias RF power $= 150/100$ W, yielding $\sim 100:1$ (Mo:SiO_2) etch selectivity.

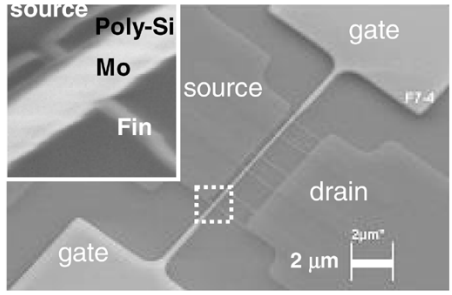
III. Molybdenum-Gated Thin-Body MOSFET Devices

The optimized Mo etch process was used to fabricate thin-body MOSFETs. The detailed process flows for Mo-gated UTB MOSFETs [21] and FinFETs [15] can be found in our previous reports. A conformal and thin Mo-gate film is preferred for thin-body MOSFETs, so that shallow nitrogen implantation can be used to tune the gate work function. Since the projected straggle (ΔR_p) is proportional to implantation energy, the as-implanted nitrogen concentration at the gate oxide interface can be reduced accordingly, to avoid damage to the gate dielectric and to minimize threshold voltage variation. The implanted nitrogen atoms can be diffused to the gate dielectric interface before source/drain implantation by rapid thermal annealing (RTA) in inert gas ambient such as nitrogen or argon.

Fig. 9(a) and (b), respectively, shows transmission electron microscopy (TEM) cross-sectional view and (b) scanning electron microscopy (SEM) plan view [15] of Mo-gated FinFETs. It



(a)



(b)

Fig. 9. (a) TEM cross-section view. (b) SEM plan view [15] of Mo-gated FinFETs.

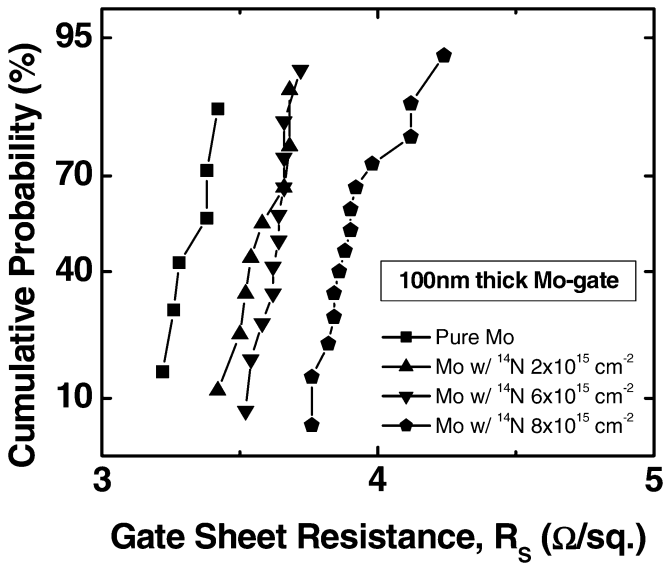


Fig. 10. Sheet resistance (R_S) of 100-nm-thick Mo films for various $^{14}N^+$ implantation doses after 900 °C, 1-min rapid thermal anneal (RTA) in nitrogen ambient. R_S increases slightly with implantation dose, because of increased impurity (N) scattering.

can be seen that the Mo was successfully etched without leaving any residue or stringers, because of the highly selective etch process. Also, the Mo gate film can be seen to be continuous along the Si fin [Fig. 9(a)]. Step coverage for Mo sputtering with PCT is improved due to the filtering of ionized species [28].

Fig. 10 shows the sheet resistance (R_S) of 100-nm-thick Mo films for various $^{14}N^+$ implantation doses after 900 °C,

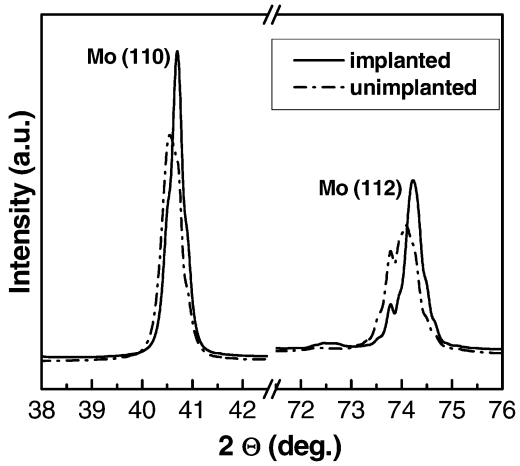


Fig. 11. XRD analysis of $^{14}N^{+}$ implanted (dose $= 1 \times 10^{16}$ cm^{-2}) and unimplanted Mo films after 900 °C, 15-s rapid thermal anneal. The full-width at half maximum (FWHM) for each of the (110) and (112) peaks is narrower for the implanted Mo film.

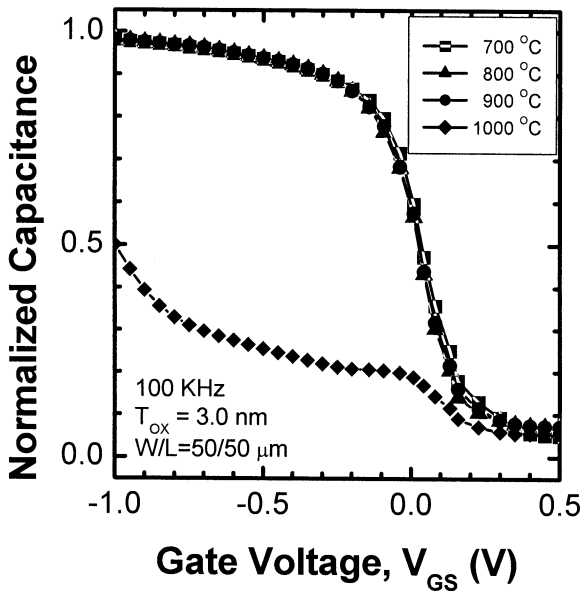
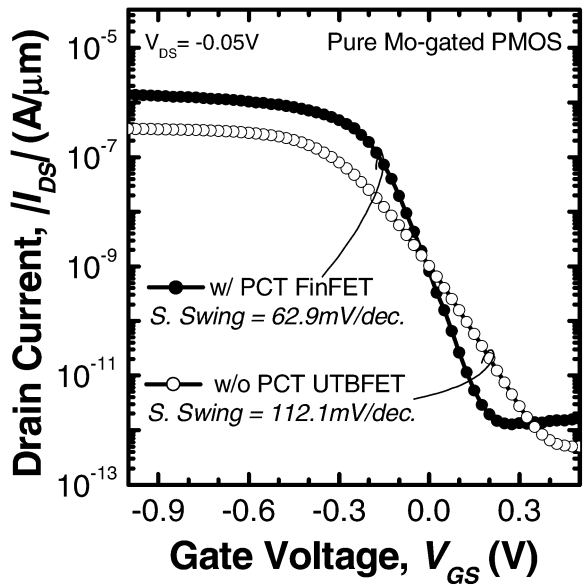
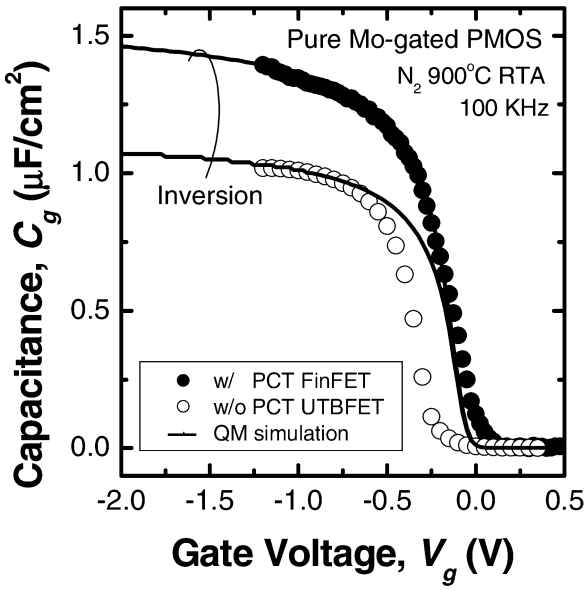


Fig. 12. Measured high-frequency gate-capacitance versus gate-voltage curves of Mo-gated MOS capacitors, showing the thermal stability of Mo on SiO_2 at various temperatures from 700 °C to 1000 °C. All films were annealed for 1 min in nitrogen ambient.



(a)



(b)

Fig. 13. (a) Measured I_D–V_G characteristics. (b) Measured C–V characteristics of p-channel thin-body MOSFETs (p-type body doping concentration $\sim 10^{15}$ cm^{-3}, no nitrogen implantation into Mo-gate). PCT Mo gate sputtering was not used for the UTB MOSFET, whereas PCT Mo gate sputtering was used for the FinFET.

1-min rapid thermal annealing (RTA) in nitrogen ambient. R_S increases slightly with implantation dose because of increased impurity (N) scattering. The average grain size can be estimated from the full-width at half maximum (FWHM) of X-ray diffraction peaks using the Scherer formula, as shown in Fig. 11 [22]. The estimated grain sizes for a pure Mo film and for a Mo film implanted with 1×10^{16} cm $^{14}N^{+}$ are 46.3 and 63.8 nm, respectively. Note that the grain size increases as more nitrogen is incorporated [23].

Fig. 12 shows measured high-frequency gate-capacitance versus gate-voltage curves for Mo-gated MOS capacitors, which were used to investigate the thermal stability of Mo on SiO_2 [14]. Samples were annealed at temperatures from 700 °C to 1000 °C in nitrogen ambient for 1 min. After a 1000 °C, 1 min anneal the capacitance in accumulation decreases, indicating that the Mo gate reacted with the gate-dielectric (SiO_2). These results indicate that Mo is thermodynamically stable on SiO_2 at temperatures up to at least 900 °C, which is adequate for activating implanted source/drain (S/D) dopants, so that it is compatible with a self-aligned (gate-first) transistor fabrication process.

Fig. 13(a) shows the measured I_D–V_G characteristics of p-channel thin-body MOSFETs (p-type body doping $\sim 10^{15}$ cm^{-3}, no nitrogen implantation into Mo-gate). PCT Mo gate sputtering was not used for the UTB device, whereas PCT Mo gate sputtering was used for the FinFET device. The ratios of the gate length to body thickness for these

TABLE I
KEY PROCESS FEATURES OF THIN-BODY DEVICES

	UTB MOSFET	FinFET	
	PMOS	PMOS	NMOS
Gate material	Molybdenum without PCT	Molybdenum with PCT	Molybdenum with PCT
Nitrogen implantation	-	-	5 KeV, 30° tilt $1x10^{16}$ cm^{-2}
EOT (inversion)	2.7 nm	1.9 nm	1.9 nm
Substrate doping	p-type, $1x10^{15}$ cm^{-3}	p-type, $1x10^{15}$ cm^{-3}	p-type, $1x10^{15}$ cm^{-3}
Gate length (L_G)	0.3 μm	1.5 μm	1.5 μm
Body thickness (T_{Si})	15 nm	80 nm	80 nm
L_G/T_{Si}	20	18.75	18.75

devices are 20 and 18.75, respectively, as shown in Table I, more than adequate to suppress short-channel effects [24]; hence, ideal subthreshold swing $(\sim 60\ \mathrm{mV/dec})$ is expected. The UTB MOSFET without PCT sputtered Mo gate shows poor subthreshold swing (112.1 mV/dec), which is likely the result of Mo sputtering damage. On the other hand, the FinFET with PCT sputtered Mo gate shows nearly ideal swing value (62.9 mV/dec). Fig. 13(b) shows the measured C–V characteristics. For the UTB MOSFET without PCT sputtered Mo-gate, a large discrepancy between measured data (open circles) and quantum-mechanical simulation (solid line) [29] exists due to fixed charge (Q_f) and/or interface charge (Q_{it}). For the FinFET with PCT sputtered Mo-gate, negligible discrepancy was observed. These results indicate that Mo gate sputtering damage can be effectively reduced/eliminated by the PCT.

Fig. 14 shows the measured I_D–V_G characteristics of Mo-gated n-channel FinFETs with HfO_2 gate dielectric (p-type body doping $\sim 10^{15}\ \mathrm{cm^{-3}}$). $1\times10^{16}\ \mathrm{cm^{-2}}$ dose of nitrogen was implanted into the Mo gates on each side of the fin at 30-degree tilt with 5 KeV implantation energy. It can be seen that V_T can be adjusted by nitrogen implantation into the Mo gate. The main mechanism of the work function tuning is due to the microstructural and chemical modification [12]. It should be noted that the subthreshold swing is not degraded with nitrogen implantation, because nitrogen does not penetrate into the gate dielectric due to the low implantation energy $(R_p = 6.2\ \mathrm{nm})$. Note that the range of threshold voltage shift for a HfO_2 gate dielectric is smaller than that for a SiO_2 gate dielectric [12], which can be attributed to the Fermi level pinning effect [26], [27].

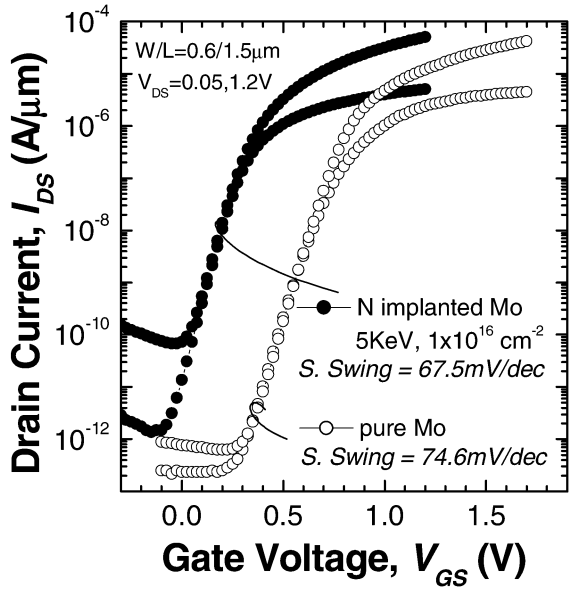


Fig. 14. Measured I_D–V_G characteristics of with PCT sputtered Mo-gated n-channel FinFETs with HfO_2 gate dielectric (p-type body doping concentration $\sim 10^{15}\ \mathrm{cm^{-3}}$). $1\times10^{16}\ \mathrm{cm^{-2}}$ dose of nitrogen was implanted into the Mo gate on each side of the fin at 30-degree tilt with 5-KeV implantation energy. Note that subthreshold swing is not degraded with nitrogen implantation, because nitrogen does not penetrate into the gate dielectric due to the low implantation energy.

IV. CONCLUSION

Damage-free sputter deposition and high-selectivity dry etch processes for Mo gate films have been developed. With a PCT, sputtering damage to the gate dielectric can be eliminated for improved drive current and GOI. Mo gate electrodes can be patterned without leaving any residue or stringers, even for nonplanar FinFETs, with the highly selective etch process. The work function of a Mo gate electrode can be tuned by nitrogen implantation followed by a thermal anneal, to provide a means for adjusting the threshold voltage of thin-body MOSFETs. The nitrogen implant results in a slight increase in sheet resistance, due to impurity (N) scattering, although it results in a slightly larger average grain size. Mo is stable on SiO_2 at temperatures up to at least 900 °C for a moderate anneal time (1 min), so that it is compatible with a self-aligned (gate-first) transistor fabrication process. An optimized Mo gate process (deposition using the PCT, etching using a high-selectivity process, low-energy implantation of $^{14}N^+$ for work function tuning without gate-oxide damage, and post-deposition annealing at 900 °C or lower to avoid reaction with the gate SiO_2) is a viable candidate for future nanoscale CMOS technologies which will require metallic gate materials with tunable work functions for optimized performance.

ACKNOWLEDGMENT

The authors would like to thank K.-S. Shin for helpful discussions on dry etching processes. Transistors were fabricated in the University of California Berkeley Microfabrication Laboratory, and the staff support is gratefully acknowledged, especially that of J. Donnelly for installing PCT into the sputtering system.

REFERENCES

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, pp. 259–288, Feb. 2001.

[2] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Miyazaki, and M. Hirose, "Limit of gate oxide thickness scaling in MOSFET due to apparent threshold voltage fluctuation induced by tunnel leakage current," *IEEE Trans. Electron Devices*, vol. 48, pp. 259–264, Feb. 2001.

[3] International Technology Roadmap for Semiconductors. Semiconductor Industry Association. [Online]. Available: http://public.itrs.net

[4] D. A. Antoniadis, "MOSFET scalability limits and "New frontier" devices," in *Proc. Symp. VLSI Technology*, 2002, pp. 2–5.

[5] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors," in *Proc. Symp. VLSI Technology*, 2000, pp. 174–175.

[6] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFETs: Part I—Effects of substrate impurity concentration," *IEEE Trans. Electron Devices.*, vol. 41, pp. 2357–2362, Dec. 1994.

[7] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate MOSFETs," in *Int. Electron Device Meet.*, 2000, pp. 719–722.

[8] Y.-C. Yeo, Q. Lu, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, T.-J. King, C. Hu, S. C. Song, H. F. Luan, and D.-L. Kwong, "Dual-metal gate CMOS technology with ultrathin silicon nitride gate dielectric," *IEEE Electron Device Lett.*, vol. 22, pp. 227–227, May 2001.

[9] I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion," *IEEE Electron Device Lett.*, vol. 23, pp. 200–201, Apr. 2002.

[10] J. H. Lee, H. Zhong, Y.-S. Suh, G. Heuss, J. Gurganus, B. Chen, and V. Misra, "Tunable work function dual metal gate technology for bulk and nonbulk CMOS," in *Proc. Int. Electron Device Meet.*, 2002, pp. 359–362.

[11] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K.-L. Lee, B. A. Rainey, D. Fried, P. Cottrell, H.-S. P. Wong, M. Ieong, and W. Haensch, "Metal-gate FinFET and fully depleted SOI devices using total gate silicidation," in *Proc. Int. Electron Device Meet.*, 2002, pp. 247–250.

[12] P. Ranade, Y. K. Choi, D. Ha, A. Agarwal, M. Ameen, and T.-J. King, "Tunable work function molybdenum gate technology for FDSOI-CMOS," in *Proc. Int. Electron Device Meet.*, 2002, pp. 363–366.

[13] R. J. P. Lander, J. C. Hooker, J. P. van Zijl, F. Roozeboom, M. P. M. Maas, Y. Tamminga, and R. A. M. Wolters, "A tunable metal gate work function using solid state diffusion of nitrogen," in *Proc. European Solid-State Devices Res. Conf.*, 2002, pp. 103–106.

[14] D. Ha, P. Ranade, Y. K. Choi, J.-S. Lee, T.-J. King, and C. Hu, "Molybdenum gate work function engineering for ultrathin-body silicon-on-insulator (UTB SOI) MOSFETs," *Jpn. J. Appl. Phys.*, vol. 42, no. 4B, pp. 1979–1982, 2003.

[15] Y. K. Choi, L. Chang, P. Ranade, J.-S. Lee, D. Ha, S. Balasubramanian, A. Agarwal, M. Ameen, T.-J. King, and J. Bokor, "FinFET process refinements for improved mobility and gate work function engineering," in *Proc. Int. Electron Device Meet.*, 2002, pp. 259–262.

[16] H. Takeuchi, M. She, K. Watanabe, and T.-J. King, "Damageless sputter deposition for metal gate CMOS technology," in *Proc. 60th Dev. Res. Conf.* , Salt Lake City, UT, 2003, pp. 35–36.

[17] Y. Kuo, "Factors affecting the molybdenum line slope by reactive ion etching," *J. Electrochem. Soc.*, vol. 137, no. 6, pp. 1907–1911, 1990.

[18] M. Schaepkens and G. S. Oehrlein, "A review of SiO_2 etching studies in inductively coupled fluorocarbon plasmas," *J. Electrochem. Soc.*, vol. 148, no. 3, pp. C211–C221, 2001.

[19] Y. Kurogi and K. Kamimura, "Molybdenum etching using CCl_4/O_2 mixture gas," *Jpn. J. Appl. Phys.*, vol. 21, no. 1, pp. 168–172, 1982.

[20] *CRC Handbook of Chemistry and Physics (1985–1986)*, CRC Press, Boca Raton, FL, 1985, pp. F-178–F-178.

[21] D. Ha, P. Ranade, Y. K. Choi, J.-S. Lee, T.-J. King, and C. Hu, "Ultra-thin body silicon-on-insulator (UTB SOI) MOSFET with metal gate workfunction enginnering for sub-70 nm technology node," in *Proc. Int. Conf. Solid-State Devices Material*, 2003, pp. 782–783.

[22] NJB. D. Cullity and S. R. Stock, *Elements of X-Ray Diffraction*, 3rd ed. Englewood Cliffs: Prentice-Hall, 2001.

[23] P. Hones, N. Martin, M. Regula, and F. Levy, "Structural and mechanical properties of chromium nitride, molybdenum nitride, and tungsten nitride thin films," *J. Phys. D: Appl. Phys.*, vol. 36, pp. 1023–1029, 2003.

[24] Y. K. Choi, D. Ha, T.-J. King, and C. Hu, "Nanoscale ultrathin body PMOSFETs with raised selective germanium source/drain," *IEEE Electron Device Lett.*, vol. 22, pp. 447–448, Sept. 2001.

[25] P. E. Nicollian, W. R. Hunter, and J. C. Hu, "Experimental evidence for voltage driven breakdown models in ultrathin gate oxides," in *Proc. Int. Reliability Physics Symp.*, 2000, pp. 7–15.

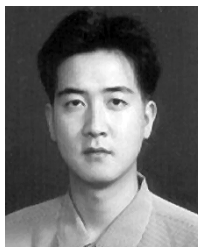
[26] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of high-k gate dielectric materials on metal and silicon gate workfunctions," *IEEE Electron Device Lett.*, vol. 23, pp. 342–344, June 2002.

[27] S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hedge, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates," in *Proc. Int. Electron Device Meet.*, 2003, pp. 307–310.

[28] S. M. Rossnagel, "Sputter deposition for semiconductor manufacturing," *IBM J. Res. Develop.*, vol. 43, no. 1/2, pp. 163–179, 1999.

[29] Shred Simulation. [Online]. Available: http://nanohub.purdue.edu

[30] T. Fuyuki, T. Furukawa, T. Oka, and H. Matsunami, "Deposition of high-quality silicon dioxide by remote plasma CVD technique," *IEICE Trans. Electron.*, vol. E75-C, no. 9, pp. 1013–1018, 1992.



Daewon Ha(M'99) received the B.S. and M.S. degrees in Electrical Engineering from Yonsei University, Korea, in 1993 and 1995, respectively. Since 2000, he has been pursuing Ph.D. degree at the University of California at Berkeley.

In 1995, he joined Samsung Electronics Company, Ltd., Kyungki-do, Korea, where he was involved in the development of 512-Mb and 1-Gb DRAM. His research interests are advanced gate stack materials and device structures for nanoscale CMOS technology, device reliability, and memory technology.

Mr. Ha was the recipient of the Best Paper Award at the 29th European Solid State Device Research Conference (1999) and the Grand Prize at Berkeley's 1st VERTEX Innovators' Challenge Competition (2002).

Hideki Takeuchi (M'00) received the B.E. and M.E. degrees from the University of Tokyo, Tokyo, Japan, in 1988 and 1990, respectively.

He joined ULSI Development Center, Nippon Steel Corporation, Sagamihara, Japan, in 1990, where he was engaged in the development of DRAM processes. From 1997 to 1999, he was a Visiting Industrial Fellow at University of California at Berkeley. He is currently a Research Specialist at University of California at Berkeley. His current research interest is in gate-stack engineering and ultrashallow junction formation.

Yang-Kyu Choi (M'04) received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1989 and 1991, respectively, and the M.S. and Ph.D. degrees from the University of California at Berkeley in 1999 and 2001, respectively.

From January 1991 through July 1997, he was with Hynix Co., Ltd., Kyungki-Do, Korea, where he developed high-density memory devices. He was a post-doctoral Researcher working on nanobio-technology at the University of California at Berkeley from 2001 to 2003. He is currently an Assistant Professor with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejon. His research interests are novel MOSFET structures such as UTBFET and FinFET, nanofabrication technology for bio-electronics, as well as NEMS, and an investigation of quantum phenomena for nanoscale CMOS. He has authored or co-authored over 50 papers, and holds six U.S. patents and 99 Korean patents.

Dr. Choi received the Sakrison Award for the best dissertation in the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in 2002. He also received the Samsung Humantech Thesis Prize in 2000 and a Best Student Paper Award at the International Semiconductor Device Research Symposium in 2001 and the International SOI Conference. His biographic profile was published in 57th *Marquis Whos Who in America*.

Tsu-Jae King (S'89–M'91–SM'01) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA.

From 1992 to 1996, she was a Member of Research Staff at the Xerox Palo Alto Research Center, Palo Alto, CA, working on poly-Si thin-film transistor technology for flat-panel display applications. In 1996, she joined the faculty of the University of California at Berkeley, where she is now a Professor of Electrical Engineering and Computer Sciences. Her research activities are presently in advanced materials, structures, and process technology for nanometer-scale integrated-circuit and micro-electromechanical devices. She has authored or co-authored over 250 publications and holds over 25 patents.

Dr. King received the Ross M. Tucker AIME Electronics Materials Award (1992) for seminal work in polycrystalline silicon-germanium thin films, a National Science Foundation CAREER Award (1998) for research in thin-film transistor technology, and the DARPA Significant Technical Achievement Award (2000) for co-development of the FinFET.