A 1.2V Receiver Front-End for Multi-Standard Wireless Applications in 65 nm CMOS LP

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***Abstract*—A low-power low-voltage wide-band inductor-less multi-standard receiver RF front-end in a digital CMOS 65nm Low Power (LP) process is described. S11 less than -10 dB is measured in the frequency range from 10MHz up to 5GHz. The front-end featuring two gain modes, achieves a voltage gain of 29dB in the high voltage gain mode, and a voltage gain of 23dB in the low voltage gain mode. The 3dB bandwidth of the RF front-end is 2.5GHz. The measured NF at 1GHz is 5.5dB in the high gain mode and 7.7dB in the low gain mode. The front-end achieves an IIP3 of –13.5dBm and –7.5dBm in the high and the low gain mode, respectively. It consumes 13 mA from a 1.2V supply in both gain modes. The implemented front-end occupies a chip area of 670um x 860um.**

I. INTRODUCTION

The proliferation of wireless standards has motivated the wireless industry to look for multiple radio devices. The integration of multiple functions on-chip enables connectivity with different systems at various locations. In order to increase hardware flexibility and functionality, RF designers are trying to design and implement cost-effective, multi-standard RF transceivers. It is a challenge to stretch the design space of an RF front-end in such a way that it satisfies simultaneously the requirements of as many standards as possible. One possibility is the use of tuned RF front-ends based on narrow-band, tunable LNAs [1]. As performance and frequency control in the narrow band LNA are inter-related, the complexity and the occupied chip area of the tuned multi-standard RF front-end grow rapidly as the number of covered standards increases. Another approach is a single wide-band RF front-end that can satisfy the requirements of any standard in a wide frequency range [2], [3]. In combination with a tunable RF filter after the antenna, this seems to be a straightforward and a cost-effective solution for a multi-standard RF front-end. The assumption here is that MEMS devices capable of tunable RF selectivity will be available in a near future.

The aim of this paper is the realization of a multi-standard receiver capable of low voltage operation (1.2V) and low power consumption. It is based on a wide-band inductor-less RF front-end. The design is realized in a baseline 65nm Low-Power (LP) process. Section II of this paper presents the operation of the multi-band receiver front-end, the measurement results are discussed in Section III and conclusions are given in Section IV.

II. MULTI-BAND RECEIVER FRONT-END

The wide-band RF front-end is shown in Fig.1. The first building block in the RF front-end is the inductor-less wide-band LNA. The LNA has single-ended input and differential output. Thanks to the single-ended input an external passive balun for the input matching is not required, and an increase in NF of 1dB to 2dB that is given by available passive baluns is prevented. Therefore, the noise requirements of the wide-band RF front-end can be relaxed. However, since the LNA does not have a balanced input extra attention has to be paid in achieving a high IIP2. The output of the LNA is differential and AC coupled to a source follower, which isolates the LNA from the passive mixer. The passive mixer switches a current and requires a voltage-to-current conversion at the input. This is performed by the resistor R_1. Both the source follower and the voltage-to-current conversion are linear functions.

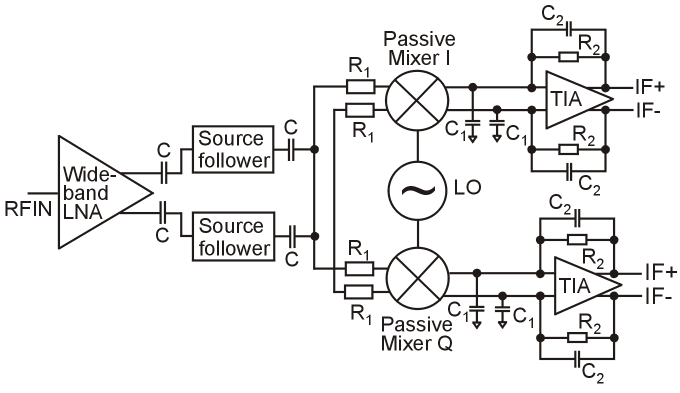

Figure 1. Wide-band receiver front-end

Therefore, the linearity of the RF receiver front-end is maximized. The current at the output of the passive mixer is converted in a voltage by the transimpedance amplifier (TIA) with the R_2-C_2 feedback, performing at the same time a low-pass filtering.

A. Wide-Band Active Balun LNA

A simplified schematic of the wide-band LNA is shown in Fig. 2. The LNA provides a single-ended-to-differential conversion. It consists of a non-inverting common gate amplifier in parallel with an inverting common source amplifier. For the input matching, the input signal is first attenuated by the amplifier input resistance. Then, the common gate stage amplifies the input signal by a voltage gain $g_{m1}R_1$, and the common source stage amplifies the input signal by a voltage gain $-g_{m2}R_2$. Such a configuration cancels the noise associated with g_{m1} [4] when the input resistance of the LNA $1/g_{m1}$ matches exactly the source impedance $R_s = 50ohm$, the noise associated with g_{m1} will cancel out. Moreover, in this case the amplified output signal is balanced. For this condition, the noise is determined by the noise of M_{n2}, and it decreases by increasing g_{m2}. The transconductance g_{m2} can be adjusted as long as the load resistor R_2 is adjusted for the balance, as well. In practice, the noise cancellation and the output signal balance are not ideal. At higher frequencies, the parasitic capacitances of the transistors affect the input matching. Inductance from the bond-wire is used to compensate for the parasitic capacitances. By adjusting the components values the input matching can improve in a wide frequency range. Extra load resistors R_1 and R_2 in series with the PMOS transistors M_{p1} are used for programming the LNA in a low gain mode.

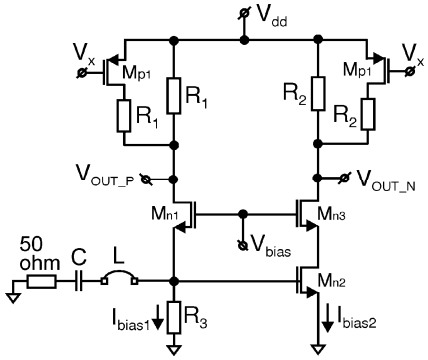

Figure 2. Simplified schematic of the wide-band LNA

B. Source Follower

A simplified schematic of the source follower is shown in Fig. 3. Together with the resistance R_1+ $R_{on,mixer}$ ($R_{on,mixer}$ is the resistance of the mixer when the mixer is ON) performs a voltage-to-current conversion in the following way. The voltage at the drain of M_{n2} is converted in a current through the resistance R_1+$R_{on,mixer}$. The capacitor C plays a role of a DC blocker. The current fluctuations on the resistance R_1+$R_{on,mixer}$ are passed through M_{n1} and sensed on the output impedance of the current source implemented by M_{p1}. The feedback circuit consisting of M_{p2} and R_{p2}, follows these fluctuations by modulating the current source M_{n2}. The capacitor C_{p2} is used to control the peaking of the source follower.

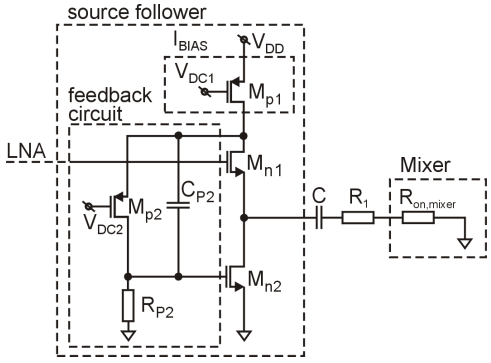

Figure 3. Simplified schematic of the source follower

Assuming that the source follower is perfect then $V_{g1} \approx V_{s1}$ (V_{g1} and V_{s1} are the voltage at the gate and the source of M_{n1}, respectively). The current through R_1+$R_{on,mixer}$ can be approximated by $i=i_1+i_2$, (i_1 is the current through M_{n1}, and i_2 is the current through M_{n2}). Thus, for $i_1 << i_2$, $i_2 \approx i \approx V_{g1}/(R_1+R_{on,mixer})$. The noise figure of the source follower can be improved by increasing the transconductance of M_{n1} and M_{n2}, and/or decreasing R_1+$R_{on,mixer}$.

C. Passive mixer and transimpedance amplifier (TIA)

The passive mixer is AC coupled to the source follower, (see Fig. 4). It commutates the current obtained through the R_1+$R_{on,mixer}$ resistance, and passes it to the transimpedance amplifier (TIA) and the R_2-C_2 feedback, which perform the current-to-voltage conversion. The capacitor C_1 is used to suppress the noise at the higher frequencies. The passive mixer can achieve high gain, moderate noise and high linearity.

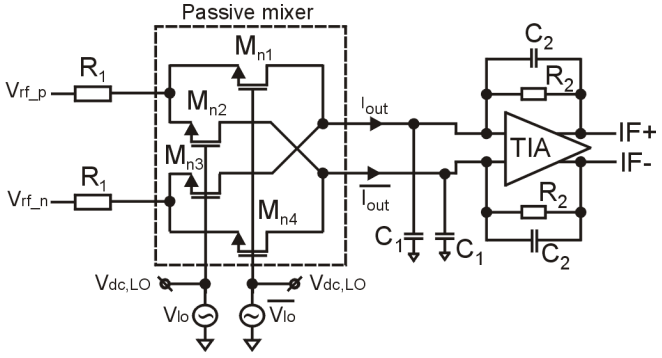

Figure 4. Simplified schematic of the passive mixer

A simplified schematic of the transimpedance amplifier used in this implementation, is shown in Fig.5. It is a simple differential amplifier that consists of a differential pair M_{n1}-M_{n2} loaded with the PMOS transistors M_{p1}-M_{p2}. The OTA insures biasing of the PMOS transistors in such a way that the output voltage of the differential pair achieves maximal swing. The voltage gain of the TIA can be approximated by $A_{TIA,v}=-g_{m1,2}r_{on1,2}\|r_{op1,2}$. Approximately, the variable $g_{m1,2}=g_{m1}=g_{m2}$, where g_{m1} and g_{m2} are the transconductances of M_{n1} and M_{n2}, respectively. Approximately, the variable $r_{on1,2}=r_{on1}=r_{on2}$, where r_{on1} and r_{on2} are the output resistances of M_{n1} and M_{n2}, respectively. And by approximating the variable $r_{op1,2}=r_{op1}=r_{op2}$, where r_{op1} and r_{op2} are the output resistances of M_{p1} and M_{p2}, respectively.

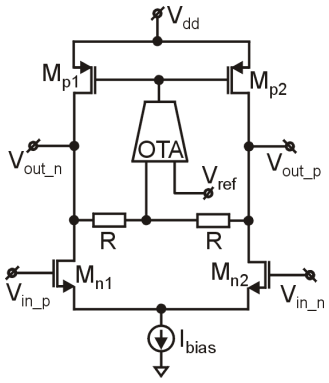

Figure 5. Simplified schematic of the TIA

The conversion gain of the passive mixer together with the transimpedance amplifier (TIA) and the R_2-C_2 feedback can be approximated by $G \approx (2/\pi)(R_2/(R_1+R_{on,mix}))$. The noise figure can be reduced by decreasing R_1+$R_{on,mixer}$, increasing R_2, and by increasing the transconductances of M_{n1} and M_{n2}, and decreasing the transconductances of M_{p1} and M_{p2} in the TIA.

III. Measurement Results

Based on the qualitative description of the building blocks and using the insights related to operation of those, the RF front-end is designed and implemented in a baseline CMOS 65nm LP process. Fig. 6 shows the die photomicrograph.

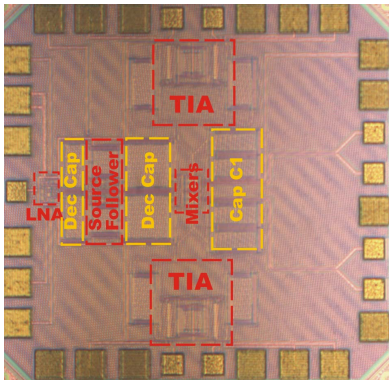

Figure 6. Die photomicrograph

The chip area together with the bond pads is 1mm^2, and the active chip area is approximately 670um x 860um. The power dissipation of the receiver RF front-end is 15.6 mW at 1.2V supply.

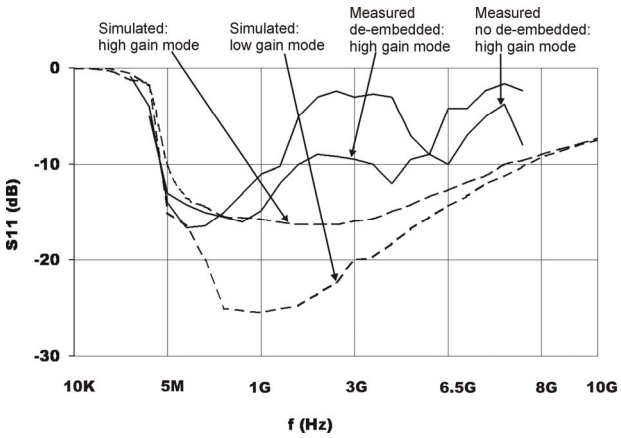

Figure 7. S11 of the receiver RF front-end

In Fig. 7 the S11 of the RF receiver is presented. The dashed lines present the simulated S11 in the low and high voltage gain mode with parasitic extraction including the estimated parasitic of the bond pad and the bond-wire. The solid lines show the measured S11 in the high gain mode with and without de-embedding the transmission line and the SMA connector on the PCB that are connected to the LNA input. First, the characteristic impedance of the transmission line deviates from 50 ohm. Second, the SMA connector is connected to the transmission line in such a way that it introduces discontinuity. Therefore, after the de-embedding of the transmission line and the SMA connector from the measured S11, the obtained results are much closer to the simulated values of S11.

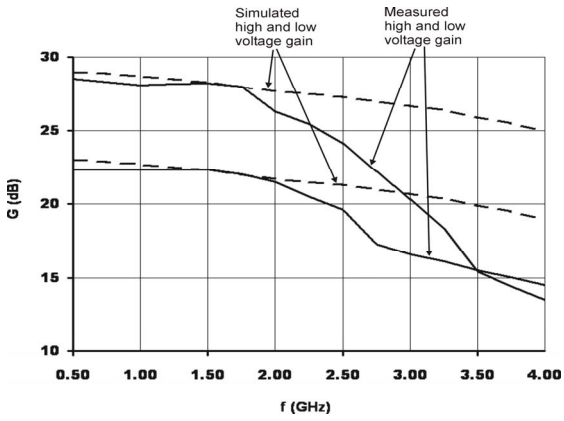

Figure 8. Voltage gain of the receiver RF front-end as a function of RF frequencies

Fig. 8 shows the voltage gain of the RF receiver as a function of the RF frequencies. The dashed lines represent the simulated high and low voltage gain with parasitic extraction.

The solid lines are the measured high and low voltage gain of the RF receiver. The simulated high voltage gain is 29dB, whereas the simulated low voltage gain is 23dB. In both cases the 3dB bandwidth is around 3.5GHz. The measured high voltage gain is close to 29 dB, and the measured low voltage gain is close to 23dB. However, the measured 3dB bandwidth for both cases is around 2.5GHz. The differences between the simulated and measured voltage gain can be explained by discrepancies in S11. The 3dB bandwidth can be further improved by adding an additional amplifier stage before the source follower.

Figure 9 shows the achieved NF of the receiver RF front-end. The dashed lines represent the simulated NF with parasitic extraction. The simulated NF is 4.9-5.5dB in the high gain mode, and 7.4-7.9dB the low gain mode of the RF receiver. The solid lines show the measured NF. The measured NF is 5.5-7.5dB in the high gain mode, and 7.7-9.9dB in the low gain mode of the RF receiver. At the lower frequencies, the measured NF matches the simulated NF. The differences between the simulated and measured NF at the higher frequencies can be explained by discrepancies in S11 and the voltage gain. Since the implemented receiver RF front-end has a single-ended input, it does not require a BALUN when connected to the antenna. Therefore, the NF impairment of typically 1.5 to 2dB is prevented, and a higher NF of the implemented receiver front-end is accepted.

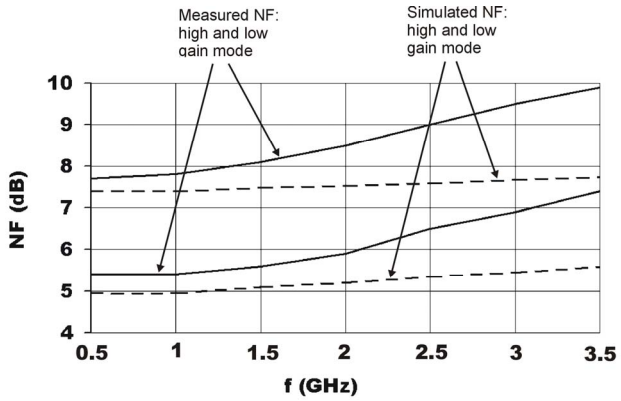

Figure 9. NF of the receiver RF front-end

Figure 10 illustrates the measured IIP3 of the implemented RF front-end in the high gain mode. The two test tones are chosen at 1GHz and 1.001GHz. The frequency of the LO signal is 998MHz. The output fundamental signals are at 2MHz and 3MHz, while the third order intermodulation products are located at 1MHz and 4MHz. The measured IIP3 is -13.5dBm in the high gain mode and -7.5dBm in the low gain mode of the RF front-end.

Analyzing the measured results the following features of the implemented front-end can be highlighted: low power consumption, high voltage gain and small chip area. Apart from this, it operates at a low supply voltage of 1.2V. The front-end has a moderate noise figure and a high *IIP3*.

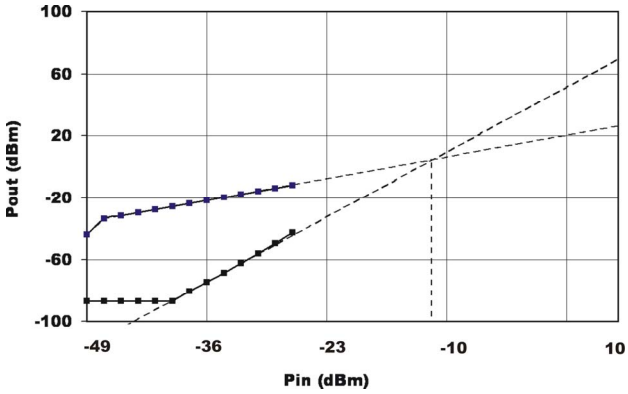

Figure 10. Measured IIP3 in the high gain mode

IV. CONCLUSIONS

In this paper the realization of a wide-band inductor-less RF front-end capable of low voltage operation (1.2V) and low power consumption (15.6mW), is presented. This is an important requirement for modern baseline deep sub-micron CMOS processes and one of the most difficult to fulfill in the RF part of the front-end. In a combination with a tunable RF filter after the antenna it represents a cost-effective solution for a multi-standard RF front-end. S11 lower than -10 dB, is measured in the frequency range from 10MHz up to 5GHz. The front-end achieves a voltage gain of 29dB in a high voltage gain mode, and a voltage gain of 23dB in a low voltage gain mode. The 3dB bandwidth of the RF front-end is 2.5GHz. The measured NF at 1GHz is 5.5dB in the high gain mode and 7.7dB in the low gain mode. The front-end achieves an IIP3 of –13.5dBm and –7.5dBm in the high and the low gain mode, respectively. The front end occupies 670um x 860um of real-estate on chip.

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