TWO-LEVEL AND THREE-LEVEL CONVERTER COMPARISON IN WIND POWER APPLICATION

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ABSTRACT Frequency converters are used in wind turbines because they make it possible to apply the variable-speed concept. They also make it possible for wind farm to become active element in the power system. The traditional frequency converter is back-to-back connected two-level converter, in which the output voltage has two possible values. However, the output voltage is smoother with a three-level converter, where output voltage has three possible values. This results in smaller harmonics, but on the other hand it has more components and is more complex to control. In this paper we study the different three-level converter topologies and make a cost and power loss comparison between the two-level and three-level converters.

1 INTRODUCTION

Low voltage switches can be used in multi-level inverters. These are faster, smaller and cheaper than high voltage switches used in 2-level inverters. When switches are in series, they withstand higher voltages. Multilevel inverters offer better sinusoidal voltage waveform than 2-level inverters due the fact that output voltage can be formed using more than two voltage levels. This causes the THD to be lower. Switching losses are reduced because switching frequency can be lower than in 2-level inverter and also the switching speed is faster with low voltage switches than with high voltage switches that are usually needed in 2-level inverters. Conduction losses are also lower because of low forward-voltage drop. When several voltage levels are used, the dv/dt of the output voltage is smaller thus the stress in cables and motor is smaller [10].

2 THREE-LEVEL INVERTER TOPOLOGIES

2.1 Diode clamped inverter

Diode clamped inverter needs only one DC-bus and the voltage levels are produced by several capacitors in series (Figure 1). Balancing of the capacitors is very complicated and only 3-level diode clamped inverters are commercially available.

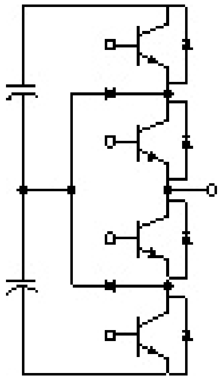

Figure 1. One leg of 3-level diode clamped inverter topology [10].

2.2 Flying capacitor inverter

Flying capacitor inverter needs isolated DC supplies for each DC-bus (Figure 2). This causes the DC-bus structure to the very complicated. [10]

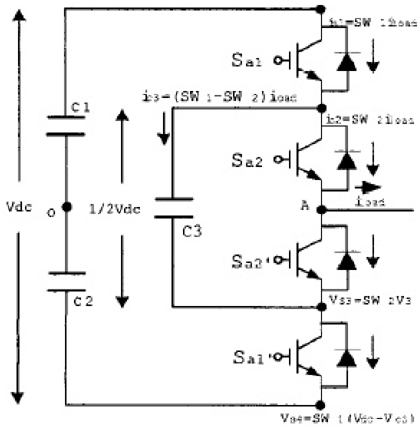

Figure 2. One leg of 3-level flying capacitor inverter topology [9].

2.3 Cascaded inverter

Cascaded inverter needs isolated DC supplies for each DC-bus (Figure 3). This causes the DC-bus structure to the very complicated. [10]

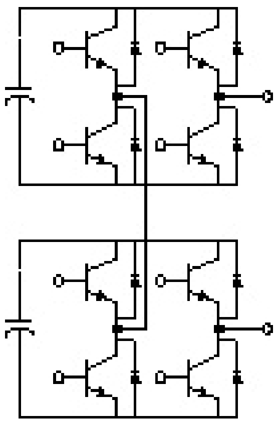

Figure 3. One leg of cascaded H-bridge inverter topology [10].

2.4 Comparison of the 2-level and multilevel inverters

In 2-level inverter output voltage waveform is produced by using PWM with two voltage levels. This causes the output voltage and current to be distorted and the THD of the voltage is poor (Figure 4, left). In 3-level inverter output voltage and current is much more sinusoidal and the THD is better (Figure 4, right).

In 2-level inverter the efficiency of the whole system is dominated by the rectifier losses in light loads (Figure 5). In 3-level inverter the efficiency at full load is better than in 2-level inverter (Figure 6). This means better energy capture of the system. Better efficiency at rated power means also smaller heat sink and better reliability. Efficiency of the 3-level inverter at small power is also improved. The value of P/Pmax is reduced at the knee by 50%.

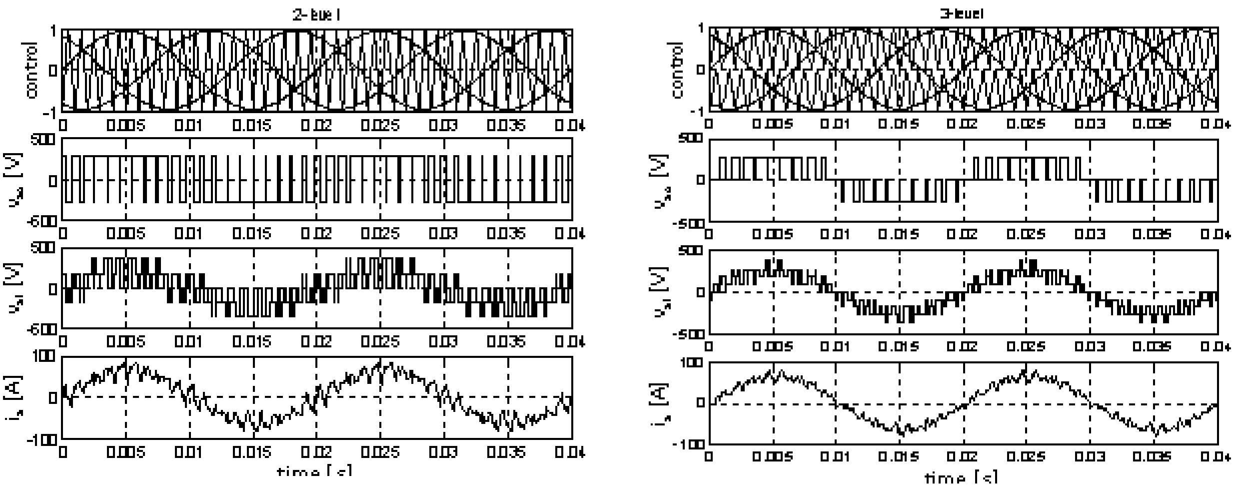

Figure 4. Comparison of the 2-level and 3-level inverter output voltages and currents [10].

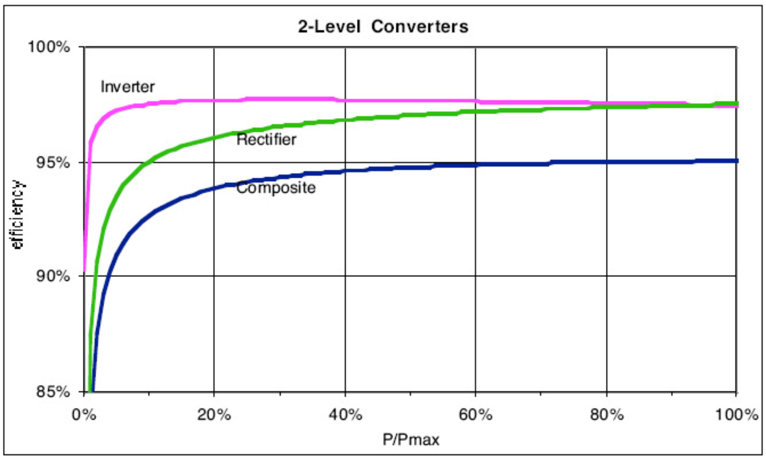

Figure 5. 2-level converter efficiency. Semiconductor conduction and switching loses included [11].

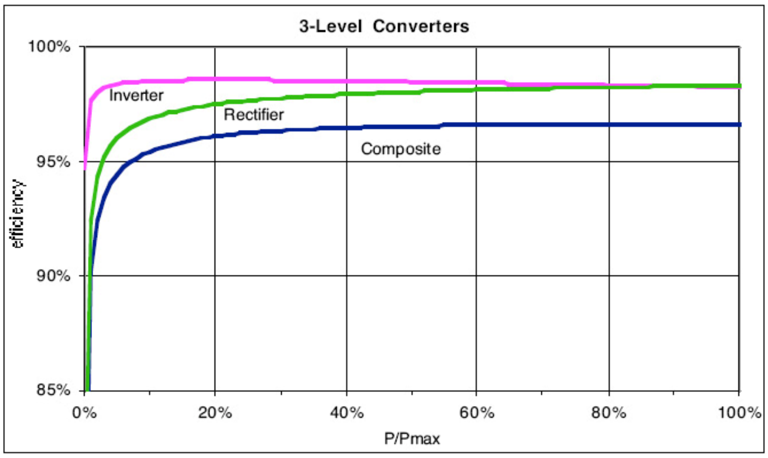

Figure 6. 3-level converter efficiency. Semiconductor conduction and switching loses included [11].

3 COST COMPARISON

In the determination of inverter configuration, usually the cost comparison of different configurations has to be executed. The cost of inverter is affected mainly by the DC-link capacitor, IGBT and the filtering components, while the rest electronics have quite insignificant affects. The good estimation of inverter costs can be done comparing the costs of capacitor and IGBT. The impact of filtering cost can be significant but the evaluation requires a lot of research and is not presented in this paper.

3.1 Determining the size of the DC-link capacitor

Because the cost of DC-link capacitor is remarkable, the sizing should be done carefully. Some optimization should be done to choose most suitable amount and size of capacitors. The size of the DC-link capacitance can be determined from the ripple of a rectifier output voltage. The minimum size of the capacitance can be calculated from [7]

$$C_{\min} = \frac{2 \times P}{\left(U_{\max}{}^2 - U_{\min}{}^2\right) \times f_{\text{rectifier}}}, \tag{1}$$

where P is power in load
$f_{\text{rectifier}}$ is rectifier output frequency

Determining the actual size of the DC-link capacitor, the tolerance of capacitance has to be taken into account. The tolerance of capacitance has to taken into account because the capacitance will decrease during the lifetime. When the actual size of the capacitor is determined the need of serial or parallel connections has to be considered. If there is need for serial connections, the voltage requirement for one capacitor can be calculated as follow [7]

$$U_{\text{cap}} = \frac{U_{\text{applied}} \times \text{Tolerance}_{\max}}{\text{Tolerance}_{\max} + (\text{n}-1) \times \text{Tolerance}_{\min}}, \tag{2}$$

where n is number of capacitors in series.

The permitted voltage ripple was chosen to be ±5% from the average DC-link voltage. The minimum capacitance requirement for two-level converter is 1200μF and for three-level 4800μF. When the voltage and capacitance tolerance requirements were taken into account, the DC-link capacitance was created with three serial and two parallel capacitances in two-level inverter and with two serial and two parallel capacitances in both side of neutral point in three-level inverter. The capacitances for two-level configuration are 2200μF @ 550 VDC and for three-level configuration 6800μF @ 360 VDC, which are standard sizes.

3.2 Cost comparison of two- and three-level inverters

The cost of inverters is mainly dependent on the IGBT and DC-link capacitor. In addition, the cost of three-level inverter includes the clamped diode. The prices of each component realized from distributors and are shown in table 1. for two-level configuration and in table 2. for three-level configuration. The tables include also the total cost of components.

Table 1. Parts, unit price and total cost of two-level inverter configuration. The cost calculation includes only the IGBT and DC-link capacitor prices.

Part	Part ID	Unit price €	Number of unit	Total unit price €
IGBT	SKM145GB123D	38,00	3	114,00
Capacitor	PEH200TX4270M	76,00	6	456,00
			Total cost €	**570,00**

Table 2. Parts, unit price and total cost of the three-level inverter configuration. The cost calculation includes only the IGBT, DC-link capacitor and diode prices.

Part	Part ID	Unit price €	Number of unit	Total unit prices €
IGBT	SKM100GB063D	24,29	6	145,74
Capacitor	PEH200XY4680M	60,50	8	484,00
Diode	SKN130/08	25,00	6	150,00
			Total cost €	**779,74**

The two-level configuration is 27% cheaper than the three-level configuration. The difference is mostly due to the cost of diodes, which are not needed in two-level configuration. The cost comparison is not taking account the effect of the volume to the unit prices. The effect of volume will decrease the unit price, which can affect to the relation between total costs.

4 POWER LOSS COMPARISON

For comparison of power losses in a three-level versus two-level inverter it is enough to compare the maximum power losses. In efficiency point of view, the power losses are averaged over the whole period of the output voltage. The losses are calculated assuming sinusoidal PWM is used.

The modules used in this study are Semikron SKM 100GB063D and SKM145GB123D. In a three-level inverter there are two modules in series in each phase, but in a two-level converter only one module per phase is needed. In addition there are two clamping diodes in the three-level converter. These diodes are of type Semikron SKN130/08.

Most of the power loss occurs in the switches, but there is also some power loss in the DC-link capacitor. The total power loss P_{loss} is

$$P_{\mathrm{loss}} = 3 \cdot P_{\mathrm{con}} + 3 \cdot P_{\mathrm{sw}} + P_{\mathrm{cap}}, \tag{3}$$

where P_{con} is the conduction loss of one phase, P_{sw} is the switching loss of one phase, and P_{cap} is the power loss in the DC-link capacitor.

4.1 Power losses in three-level inverter

In a three-level diode clamped inverter there are four IGBTs and six diodes in each phase.

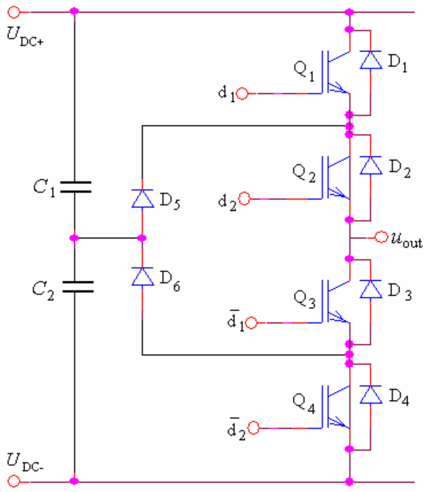

Figure 7. One phase of a three-level diode clamped inverter.

Conduction losses

The conduction losses P_{con} are comprised of losses in the IGBTs and diodes. The conduction losses for each switch can be calculated with equation [1]

$$P_{con} = U_0 \cdot I_{avg} + r_f \cdot i_{rms}^2, \tag{4}$$

where U_0 is the forward voltage drop with zero current, r_{f} is the forward resistance, I_{avg} is the average current and i_{rms} is the root-means-square of the current. The currents for IGBTs Q_1 and Q_4 are [1]

$$I_{avg} = \frac{M\hat{I}}{4\pi}\left[\sin|\varphi| + (\pi - |\varphi|)\cos\varphi\right] \tag{5}$$

$$I_{rms}^2 = \frac{M\hat{I}^2}{4\pi}\left[1 + \frac{4}{3}\cos\varphi + \frac{1}{3}\cos(2\varphi)\right], \tag{6}$$

where $\hat{I}$ is the peak current of the output voltage, φ is the phase difference between the output current and voltage and M is the modulation index. The currents for Q_2 and Q_3 are [1]

$$I_{avg} = \frac{\hat{I}}{\pi} - \frac{M\hat{I}}{4\pi}\left[\sin|\varphi| - |\varphi|\cos\varphi\right] \tag{7}$$

$$I_{rms}^2 = \frac{\hat{I}^2}{4} - \frac{M\hat{I}^2}{4\pi}\left[1 - \frac{4}{3}\cos\varphi + \frac{1}{3}\cos(2\varphi)\right] \tag{8}$$

The currents for the diodes D_5 and D_6 are [2]

$$I_{avg} = \frac{\hat{I}}{\pi} - \frac{M\hat{I}^2}{4\pi}\left[\cos\varphi + \frac{2}{\pi}\sin|\varphi| - \frac{2}{\pi}\cos\varphi\right] \tag{9}$$

$$I_{rms}^2 = \frac{\hat{I}^2}{4} - \frac{M\hat{I}^2}{2\pi}\left[1 + \frac{1}{3}\cos(2\varphi)\right] \tag{10}$$

In principle the diodes from D_1 to D_4 don't carry any current, because the current of Q_1 commutes to D_5, the current of Q_4 commutes to D_6 and the current of Q_2 commutes to Q_3. This is demonstrated in [1].

The values for U_0 and r_f are acquired from the module datasheet, and in this case they are for the IGBTs: U_{CE0} = 1,05 V and r_f = 12,12 mΩ. [3]

Conduction losses for the IGBTs Q_2 and Q_3 can be also calculated based on the equation

$$P_{con} = \frac{1}{2\pi}\int_0^{\pi} i(\varpi t)\cdot u_{CE}(\varpi t)d(\varpi t), \tag{11}$$

where i is

$$i(\varpi t) = \hat{i}\cdot\sin(\varpi t) \tag{12}$$

and u_{CE} is

$$u_{CE}(\varpi t) = U_{CE0} + r\cdot\hat{i}\cdot\sin(\varpi t). \tag{13}$$

U_{CE0} is the collector-emitter voltage with zero current and $\hat{i}$ is the output peak current. There is no need to take into account the modulation function, because the current of Q_2 and Q_3 is pure sinusoidal. Also the modulation index M can be excluded, because now it is M = 1 for the maximum power loss calculation. Calculating the integral from equation (11) and combining equations (12) and (13), we get for the conduction losses

$$P_{con/Q2} = \frac{U_{CE0}}{\pi}\cdot\hat{i} + \frac{r}{4}\hat{i}^2. \tag{14}$$

The integral is from 0 to π, because the Q_2 and Q_3 conducts only half of the output period.

Setting $M = 1$, $\varphi = 0°$ and $\hat{i} = 130$ A we can calculate the conduction losses for each switch. In reality the phase difference is never 0°, as it would then be pure resistive load and there would be no current through the diodes. Simply put the phase shift expresses how the current divides between the IGBTs and diodes. In this case we can assume $\varphi = 1°$, which is almost the same as $\varphi = 0°$ in the power loss point of view, but the current goes also through the diodes.

The values for U_0 and r_f are acquired from the module datasheet, and in this case they are for the IGBTs: U_{CE0} = 1,05 V and r_f = 12,12 mΩ. For the diode typical values are 0,85 V and 0,42 mΩ, when the junction temperature is assumed to be 25 °C. The calculated power losses are presented in Table 3. For comparison also equation (14) is used to calculate the conduction power loss for Q2. [3], [5]

Table 3. The conduction power losses of each switch.

	Q_1 or Q_4	Q_2 or Q_3 (equation(14))	D_5 or D_6
I_{avg}	10,3 A	41,4 A	31,7 A
I^2_{rms}	3586 A^2	4224 A^2	639 A^2
P_{con}	54,3 W	94,7 W (94,7 W)	27 W

As can be seen from the Table 3 the equations (14) and (4), (7) and (8) give the same answer for the conduction loss of the IGBT Q_2.

Thus the total maximum conduction power loss per phase is 2·(54,3 + 94,7 + 27) W = 352 W.

Switching losses

There are only two commutations per output period in IGBTs Q_2 and Q_3, so the switching losses of these IGBTs are excluded. The switching losses can be calculated with equation

$$P_{sw} = \frac{1}{T} \cdot f \int_T ed(\varpi t), \tag{15}$$

where f is the switching frequency and e is the switching energy

$$e = ki, \tag{16}$$

where k is a curve fitting constant. The module's maximum current is 130 A, and the E_{on} and E_{off} are almost linear at the region 0 A … 130 A, so the first order approximation is enough. The current i is

$$i = \hat{i} \sin(\varpi t). \tag{17}$$

Inserting equations (16) and (17) in (15) and integrating from 0 to $\pi/2$ we get

$$P_{sw/Q1} = 2 \cdot \frac{1}{2\pi} \cdot f \cdot \int_0^{\frac{\pi}{2}} k \cdot \sin(\varpi t) d(\varpi t). \tag{18}$$

Solving this we get

$$P_{sw} = \frac{k \cdot f \cdot \hat{i}}{\pi}. \tag{19}$$

The constant k can be acquired from the module datasheet. For IGBTs it comprises of the switch-on energy and the switch-off energy. Now k is 5,5 mWs/120 A + 3,5mWs/130A = 68,6 µWs/A, when the gate resistance is 10 Ω. The first part is the on-energy and the second part is the off-energy. However, the gate resistance is assumed to be 17 Ω at our application, so the switching energy has to be scaled to it. The scaling factor for E_{off} is 1 and for E_{on} it is 5,5/4 = 1,375. Now we get k = 79 µWs/A. Inserting this and setting the switching frequency f = 10 kHz we get for IGBTs $P_{sw/Q1}$ = 33 W per switch.

The switching losses for the diodes D_5 and D_6 can be calculated with the same equation (19) taking into account there is only switch off energy. This is expressed in the constant k. However, the manufacturer doesn't give any value for the switch-off energy in the diode datasheet, so we exclude the diode switching losses from the study.

Losses in the DC-link capacitor

The DC-link capacitor losses can be determined by the ESR value of capacitance and the current through the capacitor. The ESR value can get form datasheet of capacitor while the current can be evaluated with the help of charge and discharge times of the capacitor with the functions presented in [6]. When the charge and discharge currents are evaluated, the current through the capacitor can be estimated from charge and discharge currents [7]

$$I_{RMS} = \sqrt{I_{CRMS}^2 + I_{DCRMS}^2}, \tag{20}$$

where I_{CRMS} is RMS value of charge current
I_{DCRMS} is RMS value of discharge current

When the configuration of DC-link capacitance is taken into account, the total losses of capacitors are evaluated to be 670W in two-level inverter 520W in three-level inverter. The losses and the parameters, which were used for calculation, are shown in table 4.

Table 4. Charge and discharge currents, ESR, losses per unit and total loss. In the calculation of total loss, amount of capacitors were used six for two-level and four for three-level.

Configuration	I_{CRMS} [A]	I_{DCRMS} [A]	I_{RMS} [A]	ESR [mΩ]	Loss/unit	Total loss
Two-level	31,6	26,9	41,5	65	112	670
Three-level	73,2	62,3	96,1	14	129	520

The amount of capacitors was six for two-level configuration and four for three-level configuration. The calculation of total losses of DC-link capacitor in three-level configuration demands quite tricky evaluation of the current through capacitors. In this paper, the losses were estimated by calculating the losses of half of total capacitors. Halving the total losses of three-level configuration is based on that both the upper and lower part of the DC-link capacitor bank is used only half time in one period. This estimation can give too optimistic results and should be researched further.

Total power losses

The total power loss in three-level frequency converter is $3\cdot(P_{con} + P_{sw}) + P_{cap} = 3\cdot(352\text{ W} + 2\cdot 33\text{ W}) + 520\text{ W} = 1774\text{ W}$.

4.2 Power losses in two-level inverter

Conduction losses

The conduction losses in the IGBTs can be calculated with equation [2]

$$P_{con/Q1} = \frac{1}{2}\left(\frac{U_{CE0}}{\pi}\cdot\hat{i} + \frac{r_f}{4}\cdot\hat{i}^2\right) + M\cdot\cos\varphi\left(\frac{U_{CE0}}{8}\cdot\hat{i} + \frac{r_f}{3\pi}\cdot\hat{i}^2\right), \qquad (21)$$

where U_{CE0} is the collector-emitter voltage with zero current. The conduction losses in the diodes are calculated with equation

$$P_{con/D1} = \frac{1}{2}\left(\frac{U_{f0}}{\pi}\cdot\hat{i} + \frac{r_{fd}}{4}\cdot\hat{i}^2\right) - M\cdot\cos\varphi\left(\frac{U_{f0}}{8}\cdot\hat{i} + \frac{r_{fd}}{3\pi}\cdot\hat{i}^2\right), \qquad (22)$$

where U_{f0} is the forward voltage drop at zero current and r_{fd} is the forward resistance of the diode. Setting the same values as in the three-level case $M = 1$, $\varphi = 1°$, $\hat{i} = 130$ A and from datasheet $U_{CE0} = 2$ V, $r_f = 12{,}5$ mΩ, $U_{f0} = 1{,}2$ V and $r_{fd} = 5{,}8$ mΩ we get $P_{con/Q1} = 122{,}7$ W and $P_{con/D1} = 7{,}1$ W. So the total maximum conduction power loss per phase is $2\cdot(122{,}7 + 7{,}1)$ W = 260 W. [8]

Switching losses

The IGBT switching losses can be calculated with a simplified equation [2]

$$P_{on+off} = \frac{1}{\pi}\cdot f_s\cdot\left[E_{on}(\hat{i}) + E_{off}(\hat{i})\right], \qquad (23)$$

where E_{on} is the on-energy, E_{off} is the off-energy and f_s is the switching frequency. The switching energys are dependent on junction temperature and DC-link voltage. The module datasheet gives $E_{on} = 26$ mJ and $E_{off} = 15$ mJ, when the peak current is 130 A and the gate resistance is 6,8 Ω. However, the gate resistance is assumed to be 17 Ω at our application, so the switching energy have to be scaled to it. The scaling factor for E_{off} is 1,17 and for E_{on} it is 1,57. Now we get $E_{on} = 41$ mJ and $E_{off} = 17{,}5$ mJ. Assuming the switching frequency f_s is 10 kHz the IGBT switching power loss is 186 W per switch. [8]

Again, the manufacturer doesn't give any value for the switch-off energy in the diode datasheet, so we exclude the diode switching losses from the study.

Losses in the DC-link capacitor
The power losses in the DC-link capacitor are 670 W in a two-level converter, as calculated in chapter 3.1.

Total power losses

The total power loss in two-level frequency converter is $3\cdot(P_{con} + P_{sw}) + P_{cap} = 3\cdot(260\text{ W} + 2\cdot186\text{ W}) + 670\text{ W} = 2566\text{ W}$.

4.3 The result
The power losses in a two-level converter are bigger than in a three-level converter, 1774 W and 2556 W respectively. Both converters have the same DC-link voltage and output power. The higher power loss in a two-level converter is due higher U_{CE0} and switching energy of the module.

4.4 Discussion
The equation (4) is a little suspicious, because there are two currents used: average and root-means-square. Usually, when the same equation is presented elsewhere, the currents are either instantaneous or effective, but always the same current for the first and the second part is used [2], [4], [5]. It would be interesting to study the losses with a simulation model, where the input is instantaneous current and the voltage/current dependency is a table from the module datasheet.

The switching dead time has also some effect on the power losses, but it is excluded from this study.

5 CONCLUSIONS
The cost and power losses were compared in two-level and three-level converters. It was discovered that the two-level configuration is 27% cheaper than the three-level configuration, but the power losses are 44 % higher in a two-level converter than in a three-level converter. The different three-level converter topologies were also studied. The most suitable three-level topology for wind power application is diode clamped inverter because it can use one only DC-bus from where the different voltage levels are produced by capacitors in series.

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