ON THE FEASIBILITY OF APPLICATION OF CLASS E RF POWER AMPLIFIERS IN UMTS

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ABSTRACT

This paper investigates the feasibility of the application of class E RF power amplifiers in UMTS. A typical class E circuit has been designed and simulated, in conjunction with a linearization scheme based on the EER principle. The EER testbench uses ideal building blocks, since the emphasis is on the operation of the amplifier itself. Three different technologies have been used for the active device (Si BJT, GaAs HBT and CMOS) in order to examine the influence of the device technology on the PA performance. Relevant parameters have been monitored and put in the table form, for comparison of technologies. The simulation results indicate that class E PAs can successfully be used for power amplification of WCDMA RF signal and that GaAs technology is offering the highest efficiency.

1. INTRODUCTION

Expansive development of wireless communication systems during the last decade has particularly put the design of RF power amplifiers (PAs) in focus. Handsets are battery-operated devices and the talk-time will directly depend on the efficiency of the power amplifier in the transmitter. Power consumption of other blocks in the transceiver (DSP/baseband circuitry, oscillators, mixers, filters, LNA etc.) is often negligible to that of the PA. Efficiency and linearity are opposing requirements in the PA design and much research is focused on how to improve the efficiency of PA circuits while still satisfying the linearity requirements for a given system. Wireless communication systems nowadays make use of several modern digital modulation formats. From the PA designer point of view, these modulations can be roughly divided to those with constant envelope (e.g. GMSK) and those with non-constant (variable) envelope of the modulated RF carrier (e.g. O-QPSK). While constant envelope systems theoretically allow the utilization of non-linear PAs, variable envelope systems necessitate linear amplifiers. The third generation (3G) of wireless communication systems, also known as Universal Mobile Telecommunications System (UMTS), is an ambitiously devised system, which will provide a wide range of multimedia services (moving picture transfer etc.), and high data-rates must be supported for both uplink and downlink. Therefore, a modulation technique with high spectral efficiency has been chosen, since spectrum is an expensive resource nowadays. UMTS utilizes a Wideband Code Division Multiple Access (WCDMA) air interface, and uses Hybrid Phase Shift Keying (HPSK) modulation. The modulated RF signal has a non-constant envelope, thus requiring linear amplification in the transmitter path. The basic goal in this paper is to investigate whether a class E PA, in a conjunction with a linearization technique, has potential for application in UMTS. Class E PA circuits have been designed for maximum efficiency, using three different technologies. Their performance has been investigated in conjunction with the Envelope Elimination and Restoration (EER) concept.

2. CLASS E POWER AMPLIFIER

Class E power amplifiers were introduced by Sokal and Sokal in 1975 [1]. Since then, a considerable amount of the scientific work has been done on this intriguing type of circuit. Due to its inherently high efficiency, it represents an attractive solution for portable radio devices, enabling longer operation time. The basic, single-ended class E circuit in its original form is depicted in figure 1. The circuit consists of an active device, an RF choke and surrounding passive elements that form the load network. The transistor is operated as a switch: in the ON state it is heavily overdriven by the input signal, and in the OFF state it is in the cut-off state. It alternately opens and closes at operating frequency, and the duty cycle can be arbitrarily chosen, but 50 % is the most common value. The sinusoidal output voltage is obtained as a result of the switching action of the device and the transient response of the load network. The analysis of the class E operation has been performed many times in the literature [1, 3, 7], and it is known that the required conditions that the load network must satisfy are

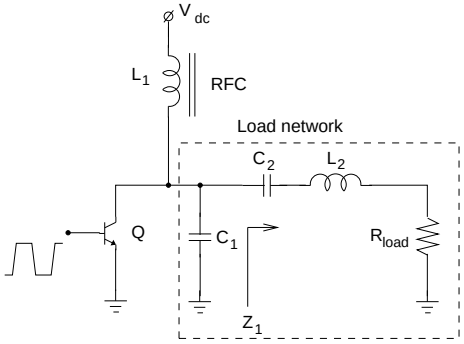

Figure 1. Basic circuit diagram of a class E PA

$$Z_1(\omega) = R_{load}(1 + j1.152) \quad (1)$$

$$Z_1(n\omega) = \infty, \ n = 2, 3, \ldots \quad (2)$$

and $C_1 = 0.1837/(\omega R_{load})$ where ω is the angular frequency of operation and R_{load} is the load resistance, determined by the supply voltage and desired output power as $R_{load} = 0.577 V_{dc}^2 / P_{out}$. These conditions provide the so-called "soft switching", a unique feature of the class E circuit, which results in an efficiency of 100% in a theoretically ideal case. The above equations are obtained as a result of an idealized analysis of the circuit employing an ideal switch, with zero on-resistance and instant switching action. Recently, new and improved design equations have been published by Sokal, that take

into account the influence of the transistor finite on-resistance, finite Q-factor of the load network and parasitic series resistances of passive elements on the output power and efficiency [2].

3. CLASS E PA AND EER

In the case of class E PAs, it is difficult to talk about linearity, since the circuit does not really perform an amplification: the input signal is seen just as information for triggering the active device, i.e. the switch, and the amplitude of the output voltage is entirely determined by the supply voltage and load network elements. In one of his early papers Raab points out that these circuits are rather power converters than amplifiers [3]. Class E PAs are suitable only for constant envelope systems and any information contained in the amplitude of the input signal will be lost at the output. However, there are ways to linearize the operation of the class E PA by making use of the suitable linearization technique. One linearization scheme is called EER and its block diagram is given in figure 2. EER is particularly suitable

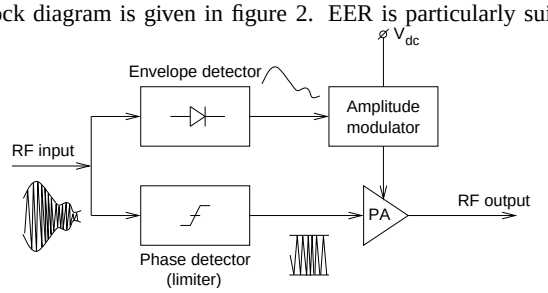

Figure 2. Block diagram of the EER principle

for class E PAs, since all voltages in the load network of the class E circuit are (in the ideal case) proportional to the supply voltage. Therefore, by changing the supply voltage it is possible to control the amplitude of the output signal. The input signal, which has a variable envelope, is passed through the phase detector (limiter) and brought to the input of the class E stage. Thus, the information contained in the phase of the input signal will be preserved in the output signal, and the envelope will be reconstructed through modulation of the supply voltage. From a theoretical point of view, this is a perfect concept: it combines linear power amplification with the high efficiency of the class E amplifier. The output signal is a truthful replica of the input signal, and the inherently high efficiency of the class E PA remains constant.

4. CLASS E PA PERFORMANCE IN DIFFERENT TECHNOLOGIES

In practice, the EER schematic will result in lower overall efficiency than the class E alone, and the whole concept is attractive only if it can offer superior efficiency to conventional class A/AB power amplifiers, while still satisfying the linearity requirements. Therefore, it is of high interest to optimize the PA for the highest possible intrinsic efficiency. Technology is one of the crucial issues, and in this paper we have used three different devices to perform a technology benchmarking: Si BJT ($f_T \approx 23\mathrm{GHz}$), GaAs HBT ($f_T \approx 50\mathrm{GHz}$) and CMOS18 technology ($f_T \approx 60\mathrm{GHz}$). The power amplifiers have been designed for operation at 1.95 GHz, which corresponds to the central frequency of the UMTS uplink band (1920-1980 MHz), and with a target output power of approximately 500 mW (27 dBm). All three designs are based on the original simple topology given in figure 1, each with roughly optimized network elements, in order to take into account different intrinsic characteristics of the used devices. In this way conditions for a fair comparison of technologies are provided.

Transistor sizing is an important issue and the first step in the PA design. In the simulated PA designs, the devices were properly sized to give the desired output power and to avoid unrealistic high current densities that could result in reliability problems. Dimensions of the BJT and the HBT have been chosen such that the peak current of the device is below the value that corresponds to the maximum f_T on the f_T vs. I_c plot. A large MOS transistor has been used in order to provide low on-resistance and thus minimize losses during the ON-state. Before presenting the simulation results, definitions of some basic figures of merit for PAs will be given. Efficiency of a power amplifier is defined as

$$\eta = \frac{P_{out}}{P_{dc}} \tag{3}$$

where P_{out} is the output RF power and P_{dc} is the supply power. This parameter is also referred to as output or collector/drain efficiency. A more realistic measure of the amplifier's performance is the power added efficiency (PAE), which takes into account the input power. PAE is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{4}$$

where P_{in} is the input power for the power amplifier. PAE significantly differs from η when the power gain is lower than 10 dB, for example, which is often the case with power amplifiers. Since the power gain of PAs is defined as $G_p = P_{out}/P_{in}$, the PAE also can be expressed as $PAE = \eta(1 - 1/G_p)$. In all three designs, the transistor input terminal (base/gate) was driven by a sinusoidal voltage with the appropriate DC offset. A similar approach has been used like in [4]. From a theoretical point of view, the ideal driving signal for class E PAs is a squarewave or trapezoidal voltage [2]. This is one of major disadvantages of class E PAs, since at frequencies in GHz range, it is difficult to efficiently generate such pulses. For this reason, a sinusoidal driving signal has been used, as an approximation and as a realistic option. Results of simulations are presented in

Table 1. Simulation results for three Class E PAs

Parameter	Technology		
	BJT	HBT	CMOS18
Frequency (GHz)	1.95	1.95	1.95
Supply voltage (V)	3	3	1.2
Output power (mW)	498	482	410
Output eff. η (%)	79	89.6	79.6
PAE (%)	75	86	-
Power gain (dB)	13.5	14.3	-
Peak $V_{c/d}$ (V)	8.6	10.56	3.85
Peak $I_{c/d}$ (mA)	480	556	1288
Breakdown (V)	12	19	4

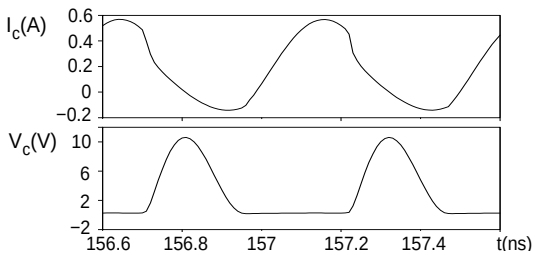

Figure 3. Simulated collector current and voltage

table 1, and the characteristic class E waveforms for the PA employing an HBT are displayed in figure 3. First, it can be noticed from table 1 that a comparable performance was achieved with all three devices. Output efficiency, η, is close to 80% for circuits with BJT

and MOSFET, and almost 90% for the PA employing HBT. The drop in the efficiency from the theoretical 100% value is caused by several phenomena. A transistor can only approximate the switching action, and will exhibit finite turn-on and turn-off transitions. Especially the finite collector/drain current fall time will have a detrimental effect. Thus, there will be a certain overlapping of non-zero voltage and current that will introduce losses. In addition, the transistor has a finite on-resistance, which causes dissipation during the ON state of the RF cycle. In [6], it was shown that efficiency degrades with on-resistance as

$$\eta = \frac{1}{1 + 1.4\frac{r_{ON}}{R_{load}}} \tag{5}$$

where r_{ON} is the on-resistance of the transistor. During the ON state, a bipolar device (BJT or HBT) is in saturation, and a MOS device is in linear (triode) region. Collector-to-emitter saturation voltage, V_{CEsat}, depends on the actual type of the device under consideration, but also on the frequency of operation [2]. In circuits employing HBT and BJT it was around 0.2V, and V_{ds} was somewhat lower in the CMOS PA. MOS model level 9 shows that R_{dsON} for the given transistor changes almost linearly from 0.105Ω to 0.16Ω when V_{ds} changes from 0 to 0.2V and the gate is constantly driven with $V_{gs} = 1.8$V. In the CMOS design, a very low R_{load} has been used of only 0.88Ω. This is necessary because of the low supply voltage, which is imposed by the breakdown limitation of the device (4V for the intrinsic gate breakdown). Taking into account $R_{load} = 0.88\Omega$, a good agreement is obtained between the simulated efficiency η and the theoretical prediction in (5). In table 1, PAE and power gain for the CMOS circuit were omitted. Due to the imperfection of the active device model it was not possible to accurately determine the input power for this design. MOS level 9 model was used. It does not model the intrinsic resistance of the MOS device, that is seen by the source driving the transistor. Namely, at high frequencies, the input impedance of a MOS transistor is no longer purely capacitive, but has a real part as well, which is dissipating power. In [5] the relation between the input power, series gate resistance and other transistor parameters was derived, but it was not taken into account that apart from the series gate resistance, the MOS model has to include the non-quasi static resistance of the channel. Therefore, for accuracy reasons, PAE and power gain are not given in table 1 for the MOS PA.

5. CLASS E AND WCDMA SIGNALS

In figure 4, a block diagram of the linearization concept based on the EER principle is presented. WCDMA baseband signals I and Q are generated by the system simulator SPW, with a 3.84 Mcps chiprate, and imported into the circuit simulator SpectreRF. The modulated RF

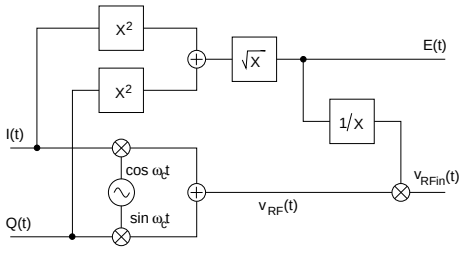

Figure 4. Linearization circuit

signal is obtained by IQ modulation as

$$v_{RF}(t) = I(t)\cos(\omega_c t) + Q(t)\sin(\omega_c t) \tag{6}$$

and can also be presented as

$$v_{RF}(t) = E(t)\cos(\omega_c t + \phi(t)) \tag{7}$$

This signal has a variable envelope (see fig. 6) and a peak-to-average power ratio (crest factor) of 5.7 dB. In the original EER schematic, the envelope of the RF signal is obtained by passing it through the amplitude detector, but it can also be done by the baseband signal processing, as $E(t) = \sqrt{I^2(t) + Q^2(t)}$. The presented linearization scheme contains a minor modification of the original EER. The RF signal coming from the IQ modulator is being multiplied by the reciprocal value of the envelope. The underlying idea is to generate the constant envelope sinusoidal signal with the preserved phase information , i.e. zero crossings. Thus, a signal

$$v_{RFin}(t) = \cos(\omega_c t + \phi(t)) \tag{8}$$

is obtained , which is more suitable for the class E PA, since it was designed for a constant envelope sinewave drive. From the linearization circuitry, signals $E(t)$ and $v_{RFin}(t)$ are fed to the class E circuit, as depicted in figure 5. Signal $v_{RFin}(t)$ is multiplied by the appro-

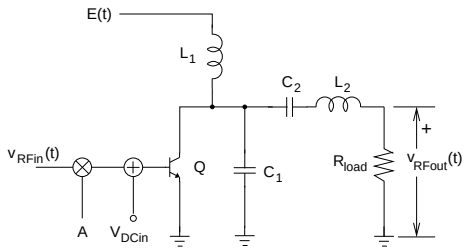

Figure 5. Class E PA with EER applied

priate constant A and a DC offset voltage V_{DCin} is added, in order to obtain the optimum driving signal for the active device. Values of A and V_{DCin} have been determined for each device separately. Envelope signal $E(t)$ is fed through a small inductance L_1. An RF choke can not be used in the circuit now, since it would have a suppressing effect on higher spectral components in $E(t)$. In figure 6, the orig-

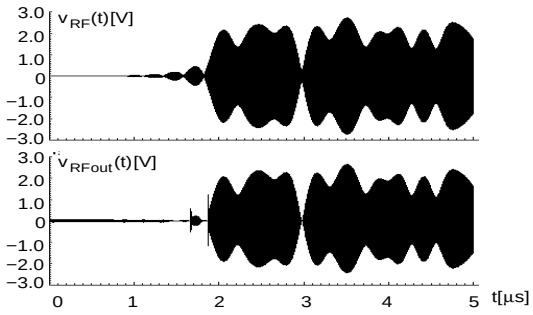

Figure 6. The original and output WCDMA RF signal

inal WCDMA RF signal and the output RF signal from the PA are given. Visual inspection shows that the original variable envelope is almost perfectly restored in the output signal. The first $2\mu s$ of the simulation should be neglected, until the WCDMA baseband generator enters the stable operation. The ACPR measurements of the output signal show that the demonstrated operation satisfies WCDMA requirements. The technical specification for WCDMA specifies the minimum $ACPR_1$=33 dBC and $ACPR_2$=43 dBc. The simulated performance of the PA is given in the table 2. Power spectral densities

Table 2. Simulated ACPR performance of the linearized PA

	Technology		
Parameter	BJT	HBT	CMOS18
$ACPR_1$ (dBc)	39.7	34.4	37
$ACPR_2$ (dBc)	55.9	53.6	46.9

used for calculation of the ACPR are obtained from the results of 35 μs transient simulation in SpectreRF circuit simulator. The waveform calculator of Spectre RF has been used in calculations. In figure 7, the power spectrum of the output signal is displayed. It is important to note that all blocks in the linearization schematic (multipliers, adders, square and square root functions) are ideal and do not introduce any delay nor distortion. This is of crucial importance, since the EER technique is particularly sensitive to delay mismatch in the envelope and phase path. The ACPR of $v_{RF}(t)$ signal, generated by an ideal IQ modulator, is 65 dBc and 85 dBc, for $ACPR_1$ and $ACPR_2$, respectively. Therefore, the output signal exhibits a certain degradation, even though the building blocks in the EER circuit are ideal. Reasons for such behaviour are multiple. First, the amplifier introduces certain amount of phase distortion. Secondly, the assumption that the amplitude of the output signal is linearly dependent on the supply voltage does not hold in practice. Theoretically, the amplitude of the output signal from an ideal class E PA, supplied by V_{DC}, is $V_{out} = 1.074V_{DC}$ and the ratio V_{out}/V_{DC} remains constant when V_{DC} changes [3]. This is not the case in practice, since there is the entire set of voltage-dependent effects of a transistor, such as nonlinear parasitic output capacitance. In figure 8, it is shown how the amplitude of the output signal depends on the supply voltage, for the PA based on the HBT. Factor k is defined as $k = V_{out}/V_{DC}$. It can be noticed that k is smaller than the theoretical value of 1.074, which is explained by the non-idealities of a real circuit and inevitable losses. But the non-constant V_{out}/V_{DC} ratio is a more significant shortcoming, since it will have a direct impact on the linearity and ACPR performance. The PAE also changes with the supply voltage, and the corresponding plot for HBT based PA is given in figure 9.

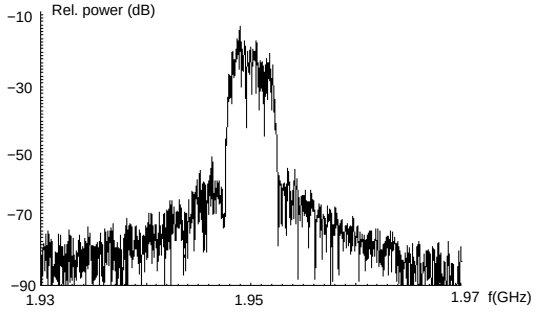

Figure 7. Power spectral density of the output signal

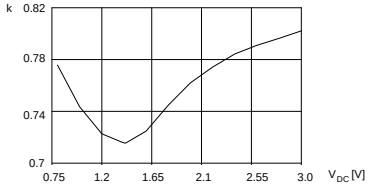

Figure 8. Non-constant V_{out}/V_{DC} ratio in a class E PA

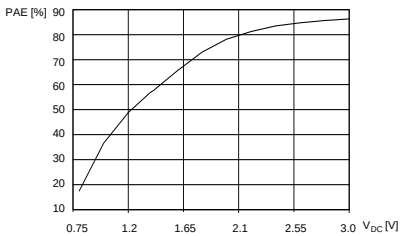

Figure 9. PAE dependence on the supply voltage

6. CONCLUSIONS

In this paper results of an investigation into the class E PA capabilities for utilization in UMTS are presented. Class E circuits with three different active devices were designed and simulated. The results of the simulations show that a comparable performance is achieved with all three technologies, but the GaAs is the most promising option. A linearization testbench based on the EER principle has been designed and applied, and the ACPR performance was simulated. All three PAs exhibited performance that satisfies the requirements prescribed by the UMTS standard. These simulations indicate that class E PAs, given the appropriate signals from the linearization circuitry are provided, can successfully be used for power amplification of WCDMA RF signal. According to our best knowledge, this is the first report in literature that quantitatively investigates the operation of class E PAs for UMTS. The presented results indicate that a further investigation on this type of PAs and the linearization circuits is of high importance. The ACPR performance can be improved by adding a predistortion block in the envelope path, that would compensate the nonlinearity caused by non-constant k factor. In practice, the nonidealities and limitations of the EER blocks will have negative effect on the ACPR, and extensive research has to be done on the practical implementation. Reduced efficiency of the class E stage at lower supply voltages indicates that an advanced hybrid solution in the form of a combination of linear (e.g. class A) and switching type PA should be considered, in order to obtain a satisfying overall efficiency performance at all power levels.

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