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Chip–Package Resonance in Core Power Supply Structures for a High Power Microprocessor

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Abstract

Advanced microprocessors have high current demands at low voltage and require low impedance power across a broad frequency range. Silicon circuits want to look out from their power terminals and see a power supply impedance that is less than or equal to a target impedance. Decoupling capacitance on the chip and package inductance form a parallel RLC circuit that has a high impedance at the chip–package resonant frequency. Circuits on the chip are not able to get the power that they need at this resonant frequency. The RLC parameters have been experimentally measured for a 70 watt microprocessor and an equivalent circuit has been developed. Chip capacitance is a strong function of bias voltage. SPICE simulation of the equivalent circuit reveals the extent of the chip–package resonance issues. The power supply impedance is determined in the resonant frequency band. Time domain simulations show the maximum excursions expected for the power supply voltage onboard the microprocessor chip.

Introduction

The silicon core circuits on a microprocessor (μP) or ASIC chip perform best when they are supplied with a constant power voltage with a small tolerance, usually 5%. It is relatively easy to find a Voltage Regulator Module (VRM) that meets the 5% tolerance at DC. By using feedback, the VRM holds the core power supply constant up to the bandwidth of the regulator, usually between 1kHz and 1MHz. At higher frequency, decoupling capacitors, usually located on the Printed Circuit Board (PCB), store charge and give energy back to the PCB as needed to hold the power supply voltage constant. With decoupling capacitors, it is possible to make a low impedance power distribution system on the PCB that meets a target impedance and is effective up to several hundred MHz [1].

As clock frequencies increase, the circuits on the silicon chip like to see a low power supply impedance and constant voltage up to several GHz. There is some amount of capacitance on chip that provides decoupling at the highest frequencies. But at lower frequency, current must come in through the electronic packaging, which is inductive in nature. The inductance of the package is in parallel with the capacitance of the chip and forms a parallel RLC resonant circuit, which resonates at some characteristic frequency. The circuits on the chip see a high impedance power supply at this frequency, which may cause problems.

This paper describes the circuit involved with chip–package resonance. Lab measurements are used to determine the RLC parameters for this circuit. The circuit is analyzed in SPICE both from the perspective of the PCB and from the active μP circuitry. Model to hardware correlation is demonstrated.

Power Supply Impedance

A target impedance may be calculated for any electronic system from the allowed voltage ripple and the maximum transient current. A μP that has 1.8V core voltage and consumes 70 watts of power has an average current of 39 amps. It may have a maximum transient current of 20 amps as the processor goes into active and inactive states. For this μP,

$$Z_{target} = \frac{Vdd \cdot 5\%}{trans\ current} = \frac{1.8\,V \cdot 0.05}{20\,A} = 4.5\ mOhms \qquad (1)$$

The power distribution system should be designed so that the impedance presented to the active circuits is less than or equal to the target impedance. This assures that the supply will remain within it's 5% tolerance under all conditions.

The transient current can come with a very fast edge rate. The μP may be inactive for a long time and then suddenly begin working on a problem. Many of the gates on the silicon chip become active in just a few clock cycles. The rise time for the current consumed by the active circuits may be as fast as 1 nSec. The μP may stop working on the problem just as quickly. It may repeat this starting and stopping process over and over again at any fundamental frequency as determined by program code. From the silicon circuit's perspective, the target impedance should be met at all frequencies that can be stimulated by the active circuits. The target impedance should be met from DC up to twice the clock frequency, because the clock circuitry draws current on each edge.

Decoupling capacitance on the silicon chip is low impedance at high frequency (1GHz) because capacitor impedance is inversely proportional to frequency. But at some lower frequency (e.g. 100 MHz), the capacitance on the chip is not low enough in impedance and does not contain enough charge to deliver the current needed by the circuits. Current must come from the PCB by way of the electronic package (and socket if there is one). The package and socket are inductive. The inductance of the package forms a parallel RLC circuit with the capacitance of the chip and resonates at the frequency

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C}} \qquad (2)$$

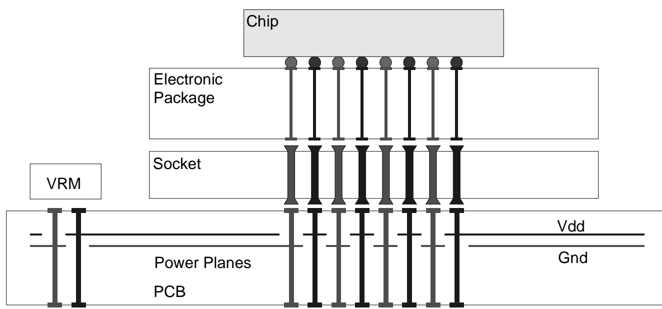

Figure 1: Chip on Package on printed circuit board (PCB) with decoupling capacitors and voltage regulator module (VRM).

where L is the equivalent series inductance of the packaging and C is the total capacitance on chip between the core voltage and ground nodes. At this frequency, the circuits on the chip look out and see a high impedance, usually much higher than the target impedance. Problems arise if program code ever causes the chip to draw current near the chip–package resonant frequency. The circuits will be starved for current and the power supply voltage measured on chip will be out of specification. A charge pump located on the silicon chip may be used to mitigate this problem [2].

Physical Structure

Figure 1 shows a cross section of a chip mounted on an electronic package, which is attached to a PCB through a socket. The Power path starts at a VRM and continues through the Vdd power plane of the PCB to get to the vicinity of the microprocessor. It continues up through the PCB vias to the pads, through the socket and up through the electronic package where it finally reaches the chip. With every current, there is an associated return current. Return current takes a similar path from the chip, down through the package and socket to the PCB pads and vias and finally on the PCB ground plane back to the VRM.

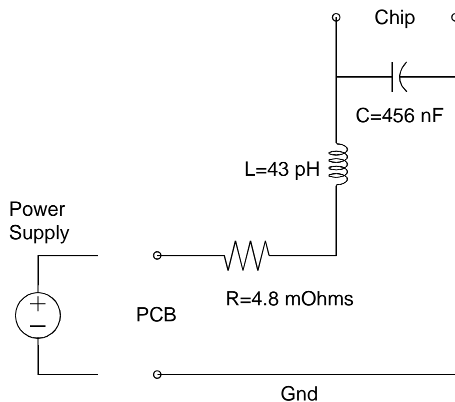

Figure 2: Simple RLC circuit for analysis.

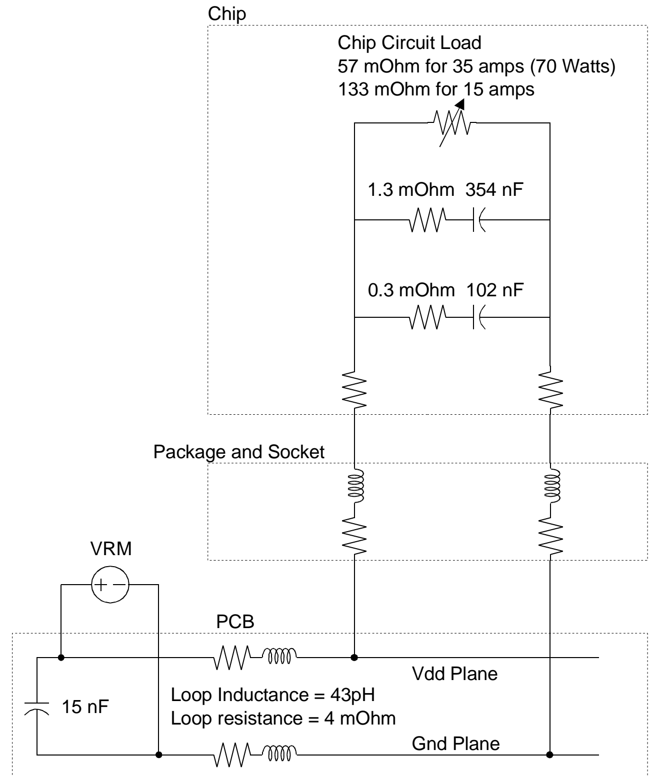

Figure 3: Circuit topology from physical structure. Gnd impedances are the same as Vdd impedances.

The physical structure is electrically modeled as resistor, inductor and capacitor (RLC) components as shown in figure 2. There is usually a high degree of symmetry between the Vdd and Gnd paths in the physical structure. Electrically, both paths are equally important. The schematic reveals the high degree of symmetry between Vdd and Gnd physical structures. The parameter values of each of the components are based on measurements and are discussed in a later section. An inductance and resistance is associated with every path through which current flows. The major capacitances of the system are identified.

Chip–Package Resonance

The properties of the circuit shown in figure 2 can be observed using a simpler circuit. Figure 3 shows a schematic diagram that exhibits the properties of chip package resonance, but the identity of the physical components is lost. The circuit may be stimulated from the chip side to see the parallel RLC resonance properties or it may be stimulated from the printed circuit board side to see the series properties.

Figure 4a shows the simulated results for the parallel circuit stimulated from the chip nodes. The PCB nodes are AC shorted together by an ideal power supply of Vdd volts. One AC amp is forced into the chip nodes and voltage is measured. Voltage is interpreted as impedance because 1 amp is forced. This is known as a parallel resonance because the inductor and capacitor provide separate parallel paths for source current. This is the case when the chip is in normal operation. There is a peak in impedance at the parallel resonant frequency. The PCB node is relatively quiet because of the low impedance of the PCB power distribution network,

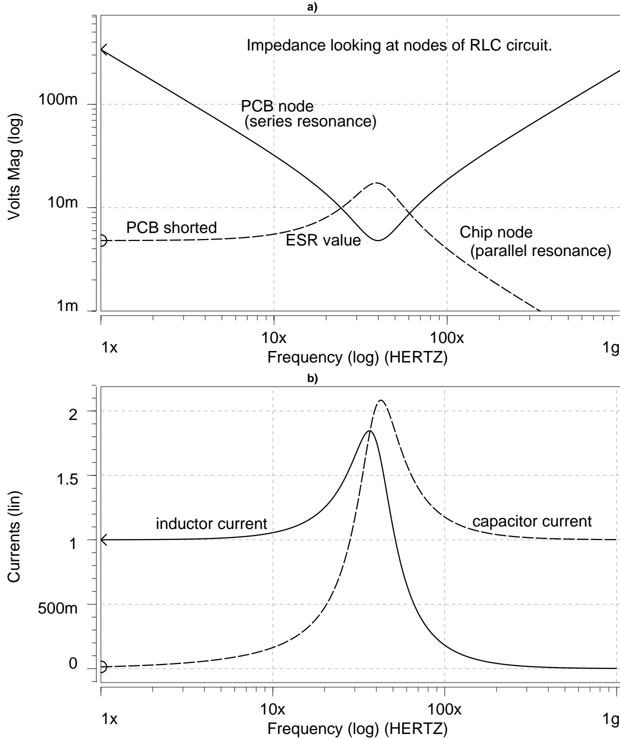

Figure 4: Simulation of simple RLC circuit. a) Parallel resonance with structure stimulated from chip and series resonance with structure stimulated from PCB. b) Current in the inductor and capacitor for the parallel circuit. .

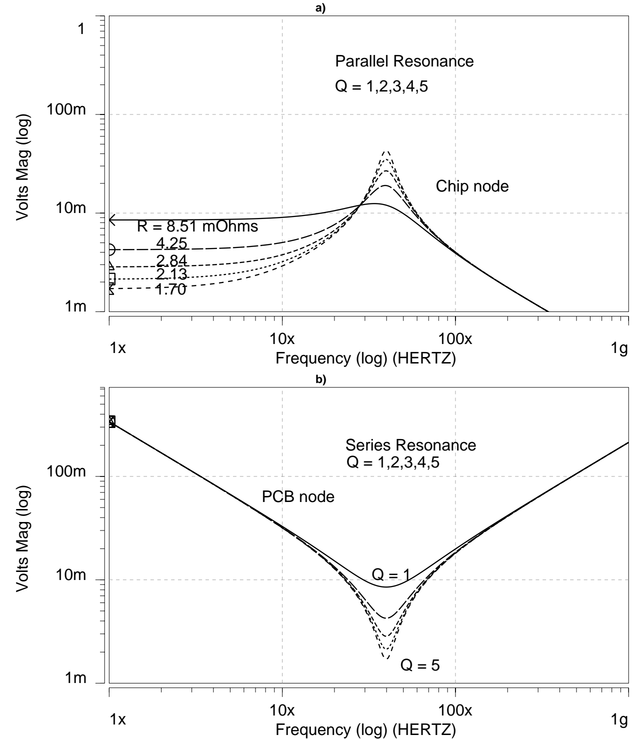

Figure 5: Resonance with several values of Q. a) Parallel circuit looking at Chip node. b) Series circuit looking at PCB node.

but there is much noise at the chip node. This is because energy is transferring back and forth between the chip capacitance and package inductance. The currents in the inductor and in the capacitor are shown in figure 4b. Even though the circuit is stimulated with 1 amp, more than one amp circulates through the reactive elements at resonance, resulting in an impedance peak.

Figure 4a also shows the simulated results when the circuit is stimulated by a 1 amp source from the PCB nodes. No DC power source is present. This is known as a series circuit because the inductor and capacitor are in series and the same current must flow through both elements. At series resonance, the impedance observed from the PCB nodes is a minimum. The negative reactance of the capacitor cancels out the positive reactance of the inductor so the impedance is resistive. Series resonance is associated with a minimum of impedance and parallel resonance is associated with a maximum in impedance. The RLC components are easily identified with portions of the series resonance curve. The capacitor is responsible for the downward (–20 dB/decade) part of the curve, the resistor determines the minimum impedance, and the inductor is responsible for the upward (+20 dB/decade) part of the curve.

The depth of the resonances are determined by the Q of the circuit. Q for a series circuit is

$$Q=\frac{\omega_0 \cdot L}{R}=\frac{\sqrt{1/LC}\cdot L}{R}=\frac{\sqrt{L/C}}{R} \quad , \tag{3}$$

where the resonant frequency $\omega_0=1/\sqrt{LC}$. Figure 5 shows the same resonant series circuit where the value of R is adjusted to make the Q = 1, 2, 3, 4 and 5 (R = 8.51, 4.25, 2.84, 2.13, 1.70 mOhms). Figure 5a shows the chip node for the parallel circuit and figure 5b shows the PCB node for the series circuit. Clearly, as R decreases and makes the Q higher, the series resonance becomes deeper and the parallel resonance becomes higher.

The simplified circuit demonstrates the dynamics of what happens when the chip capacitance resonates with the package inductance. For the parallel circuit, the PCB node remains quiet while the chip node has excessive voltage. Similar behavior is expected for a chip mounted on a package in an actual application. It is fairly easy to measure the voltage on the PCB nodes but difficult to measure voltage on chip nodes. PCB level measurements give very little indication of chip level voltages during chip–package resonance.

The role of resistance has been demonstrated. Normally, resistance in the power supply circuit is minimized to reduce IR drop and voltage regulation. But in the case of chip–package resonance, resistance helps because it lowers the Q of the circuit. In the next section, RLC parameter values for the physical structure are determined by measuring the series circuit from the PCB nodes. After RLC parameter values are determined, a SPICE model is simulated to determine the

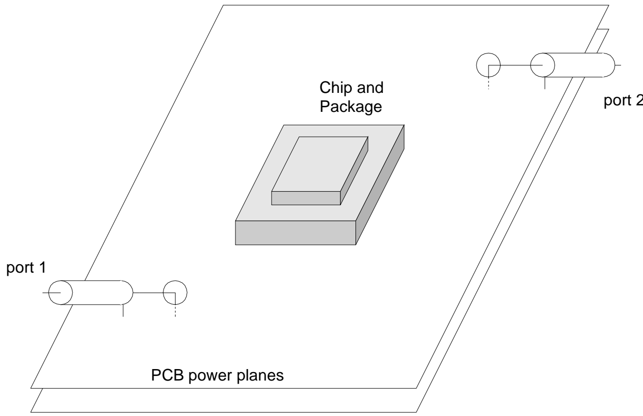

Figure 6: Measurement structure consisting of silicon chip mounted on the package on the PCB.

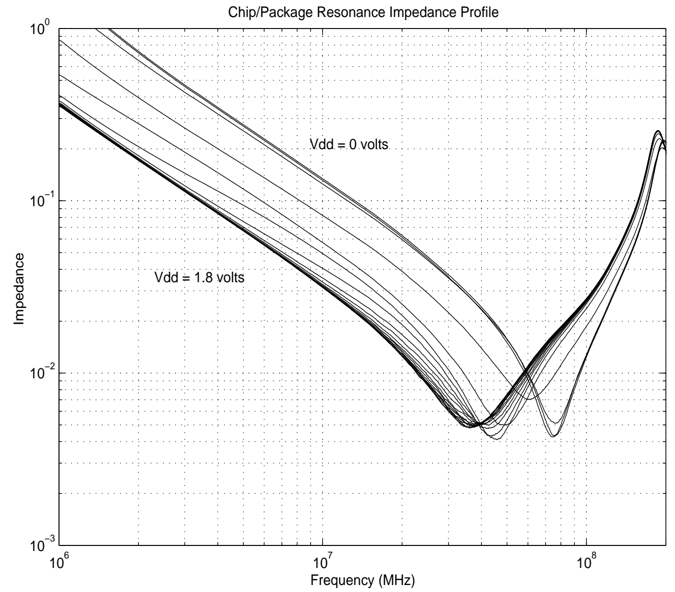

Figure 7: Measurement of silicon chip mounted on package and PCB. The capacitance of the chip is a strong function of bias voltage.

voltages that a chip will see from the parallel circuit during actual operation.

Measurements

Chip−package series resonance is measured on a microprocessor mounted on a bare PCB. There are no decoupling capacitors or other components on the PCB, only the power planes and the microprocessor are present. The measurement is made with a vector network analyzer (VNA) as described in [3]. Figure 6 shows a diagram of how the measurement is made. Calibration is performed by soldering the 50 ohm coax probes of port 1 and port 2 together with no device under test. The "through" calibration forces a flat line which is set to 0 dB. The parallel combination of the two coaxes is 25 Ohms, which becomes the reference impedance. The VNA gives S21 readings in dB, which are converted to impedance by the equation:

$$|S_{21}| = 20\log_{10}\frac{|Z_{plane}|}{25} \quad \text{and} \quad |Z_{plane}| = 25\cdot 10^{\frac{|S_{21}|}{20}} \tag{4}$$

These equations are valid when the plane impedance is much less than 25 Ohms.

Figure 7 shows the results of the series chip−package resonance measurement. Measurements are taken under several bias conditions. Under zero bias, the chip has the least capacitance. The capacitance increases dramatically when the power supply is raised past the first threshold voltage. This is because channels form under many of the FET gates and much of the thin oxide area of the chip appears as capacitance across the power supply. This chip has many intentionally−designed thin−oxide capacitors as well as many gates contributing the chip capacitance. There are no other components on the PCB so the chip comes up in an unknown state. There is no clock, so only leakage current is drawn.

Table 1 shows the RLC circuit parameters that are calculated from the impedance curves. By measuring the impedance and frequency in the capacitive portion of the curve the capacitance is calculated from

$$Z = \frac{1}{j\,\omega\,C} \quad \text{and} \quad C = \frac{1}{\omega Z} = \frac{1}{2\,\pi\,freq\,Z} \tag{5}$$

The Equivalent Series Resistance (ESR) for the circuit is the impedance where the curve bottoms out (S21(2) and freq2). The Equivalent Series Inductance (ESL) is calculated from knowledge of the capacitance and resonant frequency

$$f_0 = \frac{1}{2\,\pi\,\sqrt{L\cdot C}} \quad \text{and} \quad ESL = \frac{1}{(2\,\pi\,f_0)^2\,C} \tag{6}$$

Capacitance is a strong function of bias voltage but ESR and ESL are not.

Figure 8 shows the capacitance, ESR and ESL curves calculated in table 1. The capacitance at zero bias is due to the metal and junction capacitance of the diffusions. Capacitance goes up by nearly a factor of 5 when the chip is

PCB capacitance: 15 nF

Volts bias	current (amps)	S21(1) (dB)	freq 1 (MHz)	S21(2) (dB)	freq 2 (MHz)	Cap (nF)	ESR (mOhms)	ESL (pH)
0	0.00	−45.00	9.64	−75.26	75.31	102	4.3	44
0.1	0.00	−45.00	9.56	−75.23	76.29	103	4.3	42
0.2	0.00	−45.00	9.06	−74.07	75.64	110	4.9	40
0.3	0.00	−45.00	5.79	−71.06	60.17	180	7.0	39
0.4	0.01	−45.00	4.15	−74.20	48.48	258	4.9	42
0.5	0.02	−45.00	3.10	−75.78	45.25	350	4.1	35
0.6	0.03	−45.00	2.60	−75.16	43.71	420	4.4	32
0.7	0.05	−50.00	4.45	−74.43	42.60	437	4.7	32
0.8	0.08	−50.00	4.36	−74.12	41.68	447	4.9	33
0.9	0.11	−50.00	4.31	−73.77	41.33	452	5.1	33
1	0.15	−50.00	4.28	−73.86	40.27	455	5.1	34
1.1	0.19	−50.00	4.27	−73.83	38.23	456	5.1	38
1.2	0.24	−50.00	4.26	−74.08	37.58	457	4.9	39
1.3	0.29	−50.00	4.26	−74.08	37.10	458	4.9	40
1.4	0.35	−50.00	4.26	−74.11	37.26	458	4.9	40
1.5	0.41	−50.00	4.26	−74.23	36.46	458	4.9	42
1.6	0.46	−50.00	4.26	−74.31	37.58	457	4.8	39
1.7	0.53	−50.00	4.27	−74.17	37.26	457	4.9	40
1.8	0.60	−50.00	4.27	−74.31	36.78	456	4.8	41

Table 1: Calculated RLC circuit parameters for several bias voltages.

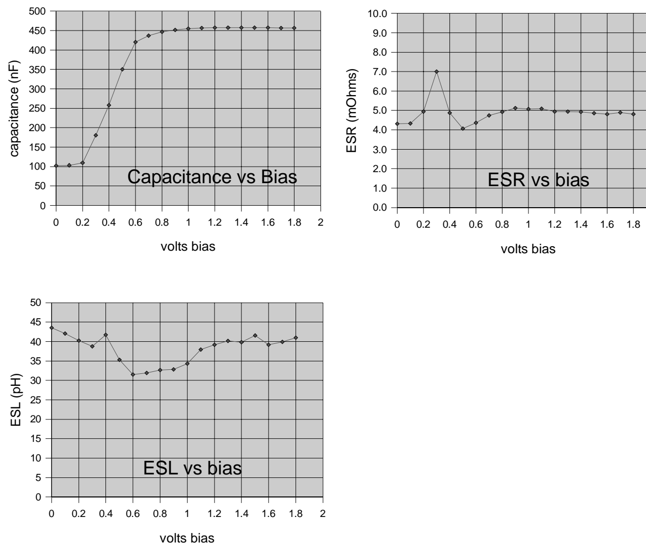

Figure 8: Derived values of capacitance, ESR and ESL from table 1.

biased at the operating voltage as discussed above. The ESR has an interesting peak just as the capacitance is ramping up. This is because channels are forming under the CMOS gates. The channels are weak and therefore highly resistive as the gates pass through the FET threshold voltage. When the channels are completely formed, the ESR drops down to nearly it's initial value, with a slightly more resistance due to the diffusion contacts and the FET channels. The ESL stays relatively constant around 40 pH.

Equivalent Circuit

From the measured results, the parameters of figure 3 are obtained. The total loop inductance is 43 pH. The total loop resistance is 4.8 mOhms and the chip capacitance is 456 nF under 1.8V bias, the chip operating voltage.

The parameters of figure 2 are a little less obvious. By separate measurement, the capacitance of the PCB is known to be 15 nF, which does not contribute to the chip−package resonance frequency. The only other major capacitance in the system is in the chip which is 102 nF with 0V bias and 456 nF with 1.8V bias. To obtain these capacitances, the 1.3 mOhm resistor is opened up to a high impedance at 0V bias and given the value of 1.3 mOhms when the chip is biased at 1.8V. The on−chip resistances are not calculated individually but are chosen to satisfy the loop ESR under the two bias conditions. This correctly accounts for the capacitance under two bias conditions.

The package, socket and PCB contribute resistance and inductance. To obtain 4.3 mOhms under 0V bias and 4.8 mOhms under 1.8V bias, a 4 mOhm loop resistance is used for the packaging. The total loop inductance is 43 pH. The solution is not unique.

The series circuit of figure 2 is simulated in SPICE. The results are shown in figure 9 along with the measured results. There is good model to hardware correlation with 0V bias and 1.8V bias.

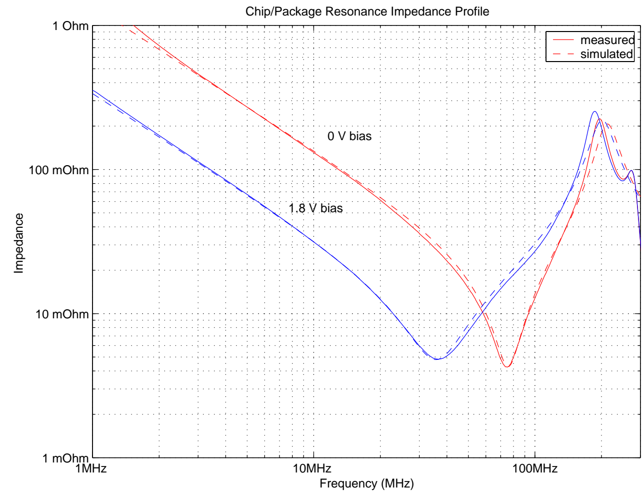

Figure 9: Measured and simulated results for series chip−package resonance when stimulated from PCB. The circuit of figure 2 is simulated.

SPICE Simulation from Chip Perspective

The most important issue is the impedance presented to the chip power terminals and the noise seen by the circuits. It is very difficult to measure this because the chip is flipped over and the power terminals are not available for measurement. It is however easy to simulate the circuit in SPICE with the topology and parameters from above. Figure 10a shows the simulated impedance of the chip looking out into the package terminal of figure 2. The chip sees an

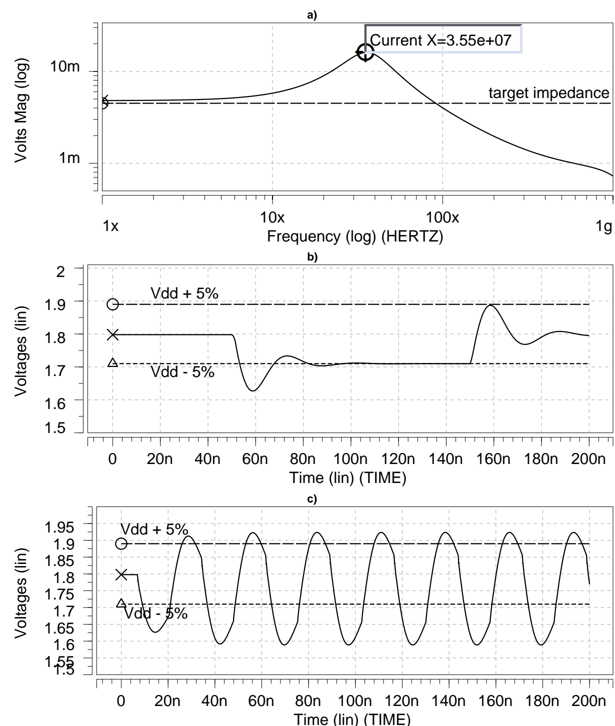

Figure 10: Spice simulation of chip−package resonance when stimulated from chip.

impedance greater than the target impedance at the chip−package resonant frequency, 35.5 MHz. Above this frequency, the on−chip capacitance supplies current at low impedance and below this frequency, the PCB supplies the current.

Figure 10b shows a time domain waveform where the circuits on chip abruptly demand a 20 amp current transient and then stop demanding the current. Ringing is apparent. Because the power distribution system meets the target impedance at low frequencies, the waveform settles out at exactly 5% below the power supply voltage. But the impedance peak at 36.5 MHz has caused the circuit to ring and exceed the 5% limit when the chip demands the current transient.

The worst thing that can happen is for the chip to demand this current transient over and over again at the chip−package resonant frequency. This is simulated in figure 10c. When stimulated at 36.5 MHz, the power supply voltage exceeds both the +−5% limits. Current is swinging back and forth between the on−chip capacitance and the package inductance. Series resistance in the chip, package, socket and PCB have made the Q of the circuit low enough that the target impedance is only exceeded by a factor of two. The problem can be much greater with highly inductive or very low resistance circuits.

Conclusions

The inductance of an electronic package and capacitance of a chip form a parallel resonant circuit. This presents a high impedance to the chip power terminals which may exceed the target impedance at the chip−package resonant frequency. The parallel RLC circuit has been quantified by measuring the characteristics of the series RLC circuit from the PCB side. This is much easier than measuring the characteristics of the parallel circuit from the chip side. Chip capacitance is a strong function of bias voltage. After the parameters of the RLC circuit are identified, SPICE simulation is used to determine how the parallel resonance can disturb the chip supply voltage and impact the operation of the chip.

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