

# A 10 Bit Current-Mode CMOS A/D Converter with a Current Predictor and a Modular Current Reference

Soung Hoon SHIM<sup>†</sup>, Nonmember and Kwang Sub YOON<sup>††</sup>, Member

**SUMMARY** This paper describes a 10 bit CMOS current-mode A/D converter with a current predictor and a modular current reference circuit. A current predictor and a modular current reference circuit are employed to reduce the number of comparator and reference current mirrors and consequently to decrease a power dissipation. The 10 bit current-mode A/D converter is fabricated by the 0.6  $\mu\text{m}$  n-well double poly/triple metal CMOS technology. The measurement results show the input current range of 16  $\mu\text{A}$  to 528  $\mu\text{A}$ , DNL and INL of  $\pm 0.5$  LSB and  $\pm 1.0$  LSB, conversion rate of 10 Msamples, and power dissipation of 94.4 mW with a power supply of 5 V. The effective chip area excluding the pads is 1.8 mm  $\times$  2.4 mm.

**key words:** current-mode, current predictor, modular current reference circuit, A/D converter

## 1. Introduction

As the VLSI technology develops rapidly, it is becoming a common practice recently that several functional chips have been integrated into one chip to implement a mixed signal processing system (system-on-a-chip). The mixed signal processing system for a portable low-power image signal application requires a high resolution/low power A/D converter to interface with a digital signal processor. The conventional A/D converter architectures for image signal processing include the voltage-mode full-flash and the voltage-mode two-step flash architectures. If these conventional architectures are utilized to design a 10 bit resolution A/D converter, it requires 1,024 and 64 comparators, respectively [1]. Therefore it results in increasing both a chip area and a power dissipation. Another design technique proposed in the literature to minimize a power dissipation is a folding and interpolation method [2]–[6]. It can achieve a high speed and low power consumption because it does not require a high speed sample and hold circuit. However, it suffers from a low resolution due to the device mismatches within a folding and interpolation circuit. It is found in the literature [7] that the architecture of the pipelined A/D converter is suited to high speed and low power application. But it requires a precise timing control technique, which makes chip implementation difficult due to process variations and device mismatches.

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In this paper, a 10 bit multi-step current-mode A/D converter with a current predictor and a modular current reference circuit is proposed to reduce not only the number of comparator and current reference but also to decrease a power dissipation and chip area.

## 2. Design of the 10 Bit Current-Mode A/D Converter

The block diagram of the designed 10 bit A/D converter with a clock timing diagram for  $\phi_1$ – $\phi_4$  is illustrated in Fig. 1. The proposed current-mode A/D converter consists of a track/hold circuit, a current predictor, a modular current reference circuit, a 5 bit flash converter, a current subtraction amplifier, a digital error correction circuit, a binary encoder, and latch circuits. During the first data conversion cycle, the current predictor determines the analog input current range of  $I'_{in}$ , to be held by the track/hold circuit. The current predictor generates the thermometer codes corresponding to MSB and MSB-1, and these thermometer output codes control the current generation circuit within the modular current reference circuits, as shown in Fig. 6.  $I'_{in}$  from the track/hold circuit is applied to the input of the current generation circuit within the modular current reference circuit and converted to the appropriate value shown in Table 1 in order to feed the 5 bit flash converter block. The output thermometer codes of the 5 bit flash converter and current predictor are converted into 6 bits by the binary encoder. During the second data conversion cycle, the amount of the analog current associated with the 4 bit generated by the 5 bit flash converter is subtracted from the output current of the modular current reference circuit in the current subtraction amplifier. The subtracted current is amplified by  $2^4$  times and recycled back to the 5 bit flash converter block, where the final thermometer codes corresponding to the 5LSB's are determined. The 1 bit of the 5LSB's is utilized for digital error correction [8].

The circuit diagram of the two bit current predictor is shown in Fig. 2. The current predictor converts the range of the analog input current into the four output levels as follows;

$$\frac{1}{4}aI_{FS} < I_{in} < \frac{1}{4}(a+1)I_{FS} \quad (a = 0, 1, 2, 3) \quad (1)$$

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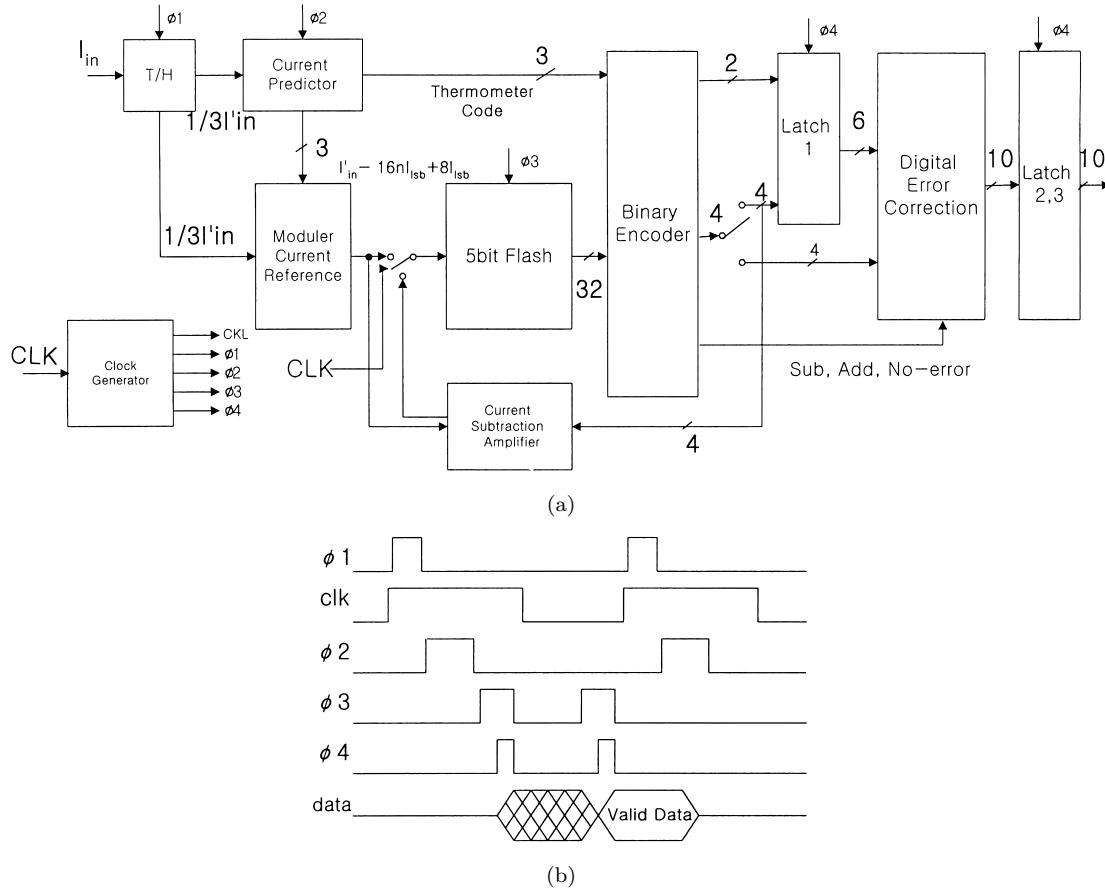


Fig. 1 (a) Block diagram and (b) clock timing diagram of the 10 bit current-mode ADC.

**Table 1** The generated current in the current generation circuit within the modular current reference circuits associated with the thermometer code of the current predictor.

Thermometer code of the Current predictor	The generated current
000	$I'_{in}$
001	$I'_{in} - 16I_{lsb}$
011	$I'_{in} - 32I_{lsb}$
111	$I'_{in} - 48I_{lsb}$

( $I_{lsb}$ : a magnitude of current of the upper 6 bit LSB)

where  $I_{FS}$  is the full scale of the analog input current. The input current controlled by the thermometer code of the current predictor is described in Table 1. The current predictor generates the thermometer code and the generated thermometer code ( $P_{out1}$ ,  $P_{out2}$ , and  $P_{out3}$ ) is fed into the binary encoder and controls the modular current reference circuit. Utilization of the two bit current predictor, the modular current reference circuit, and the recycling technique allows the number of comparators to become

$$\#comparator(N) = 0.5 \cdot 2^{N/2} \quad (2)$$

where  $N$  is the resolution of the A/D converter. It is noted that the upper/lower eight comparators for digital error correction are ignored in (2).

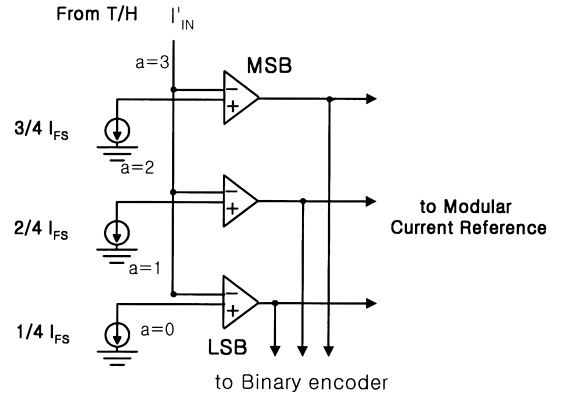


Fig. 2 Circuit diagram of the current predictor.

According to (2), the number of comparators in the proposed A/D converter can be reduced to 70 percent, compared with those in the two-step flash architecture [9]. Figure 3 illustrates the comparison of the number of comparators for the full flash, two-step flash, and the proposed A/D converter.

The conventional 5 bit current-mode flash converter requires the current references ranging from  $1I_{LSB}$  to  $32I_{LSB}$ , where  $I_{LSB}$  is equal to a magnitude of current of the upper 6 bit LSB. In order to reduce

the power consumption of the A/D converter, a modular current reference circuit illustrated in Fig. 4 is proposed in this paper. The 32 current references shown in Fig. 4 are grouped into the four modules with the identical structure. Each module generates the eight current references ranging from  $1I_{LSB}$  to  $8I_{LSB}$ .  $I''_{in}$  is applied to the 8 comparators in the module #1 circuit. And  $I''_{in} - 8I_{LSB}$ ,  $I''_{in} - 16I_{LSB}$ , and  $I''_{in} - 24I_{LSB}$  are applied to the 8 comparators in the module #2, #3, and #4 circuit, respectively. The modular current reference circuit employs a current-mode high speed current comparator circuit [10]. Figure 5 shows the circuit diagram of the current subtractor circuit within the modular current reference circuit.

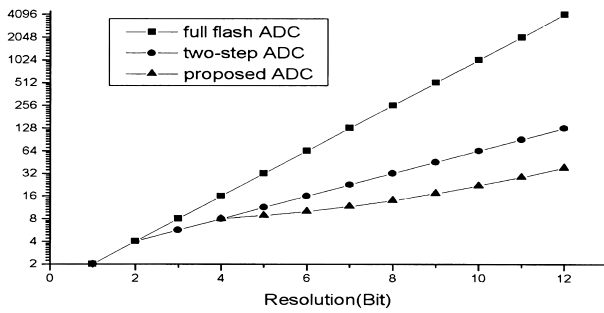


Fig. 3 Comparison of the number of comparator.

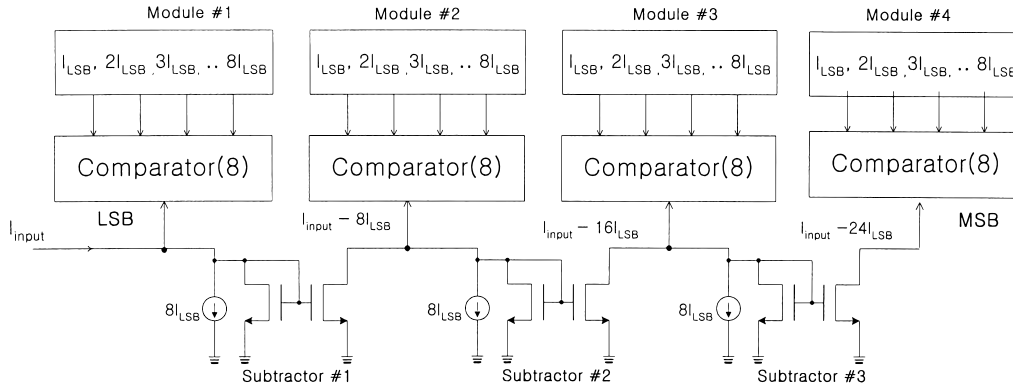


Fig. 4 Circuit diagram of the modular current reference.

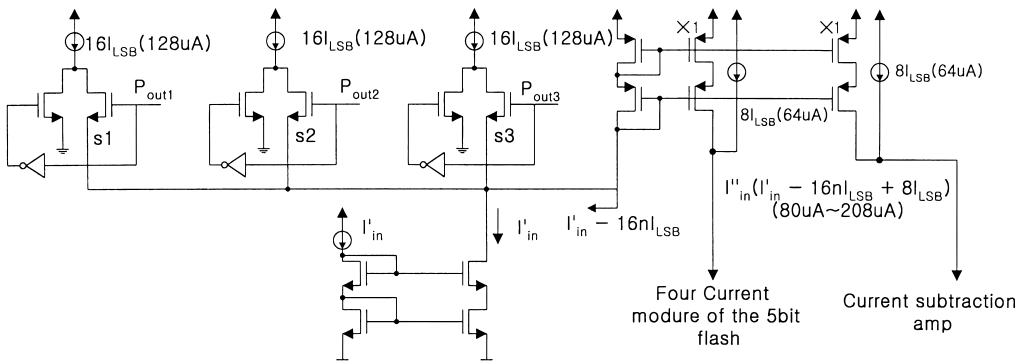


Fig. 5 Circuit schematic of the current generation circuit within the modular current reference circuit.

If the condition,  $9I_{LSB} < I''_{input} < 10I_{LSB}$  is met in the modular current reference circuit, this condition is identical to  $1I_{LSB} < I_{input} - 8I_{LSB} < 2I_{LSB}$ . The thermometer codes associated with this condition are generated by the modular current reference circuit. In this manner, the magnitude of the current reference can be reduced by decreasing the magnitude of the input current. It results in a reduction of both power consumption and chip area.

In order to compare a power consumption of an  $n$  bit flash converter with a conventional current reference circuit and a modular current reference circuit, the magnitude of the currents required by a conventional current reference circuit and a modular current reference circuit are described by (3) and (4), respectively.

$$(1 + 2 + 3 + \dots + 2^N)I_{lsb} = \frac{2^N(2^N + 1)}{2}I_{lsb} \quad (3)$$

$$m \left( 1 + 2 + 3 + \dots + \frac{1}{m}2^N \right) I_{lsb} + (m-1)\frac{1}{m}2^N I_{lsb} \\ = 2^N \left( \frac{1}{m}2^{N-1} + \frac{m-1}{m} + \frac{1}{2} \right) I_{lsb} \quad (4)$$

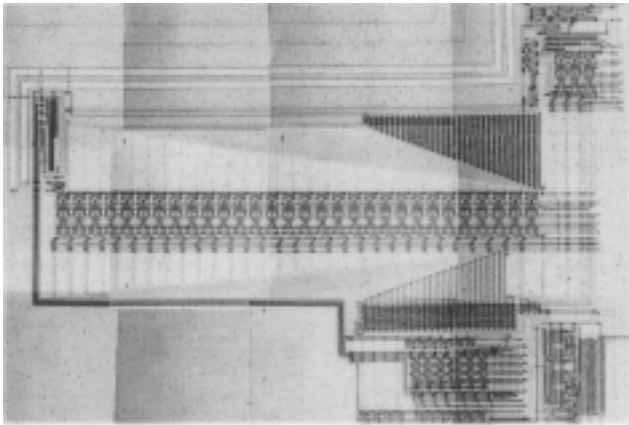
where  $I_{lsb}$  and  $m$  is a magnitude of the LSB current reference and a number of module, respectively.



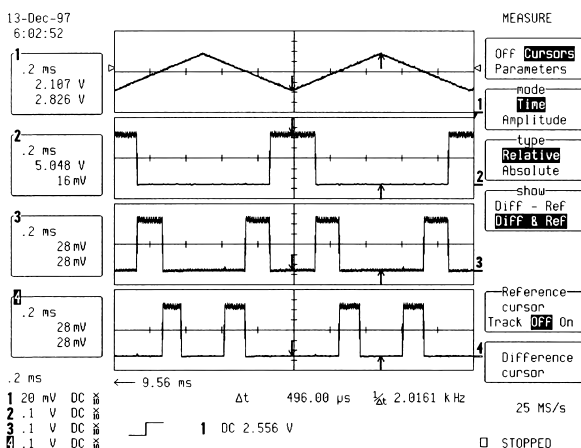
flow of the upper 6 bits to the full adder and subtractor circuits, and it achieves a digital error correction.

### 3. Experimental results

The designed 10 bit A/D converter is fabricated by the 0.6  $\mu\text{m}$  n-well double poly/ triple metal CMOS technology. The chip microphotograph of the A/D converter is shown in Fig.9. The effective chip area is 1.8mm  $\times$  2.4mm. The measured output thermometer codes ( $P_{\text{out1}}$ ,  $P_{\text{out2}}$ , and  $P_{\text{out3}}$ ) from the current predictor circuit with a triangular wave of 1 kHz and a clock of 100 kHz are shown in Fig. 10. These three output codes are applied to the binary encoder through the three input NOR gates. It can be seen from Fig.10 that each thermometer code is generated everytime each code is falling downward. The propagation delay time of the current predictor is measured to be 5 ns, as illustrated in Fig. 11. The measured output wave from the modular current reference circuit with a triangular wave of 1 kHz and a clock of 100 kHz is shown in Fig. 12. The load resistor of 10k $\Omega$  is connected to the output ter-

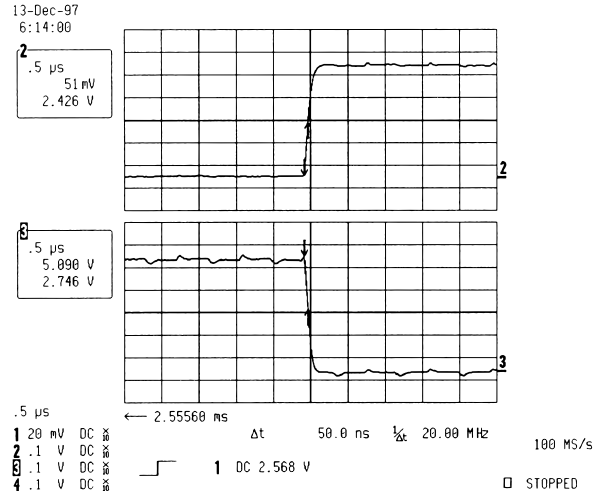


**Fig. 9** Chip microphotograph of the 10 bit current-mode A/D converter.

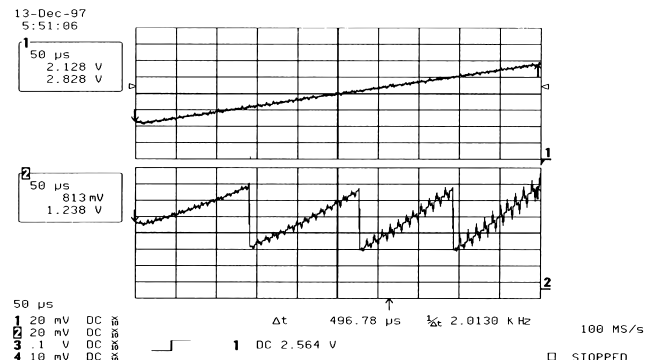


**Fig. 10** The measured output code plot of the current predictor circuit.

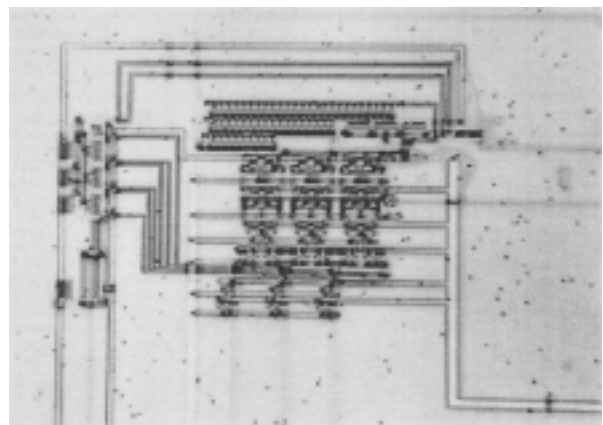
minal of the modular current reference circuit. It is noted that as the output codes applied from the current predictor, the operation of the current subtraction occurs in the modular current reference circuit. The glitches in the measured data result from the sampling



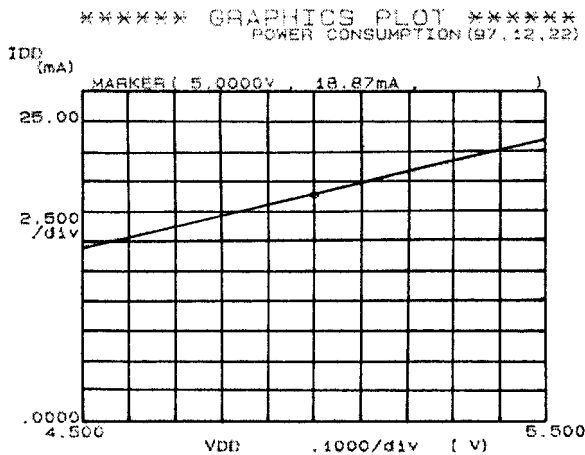
**Fig. 11** The measured delay time of the current predictor circuit.



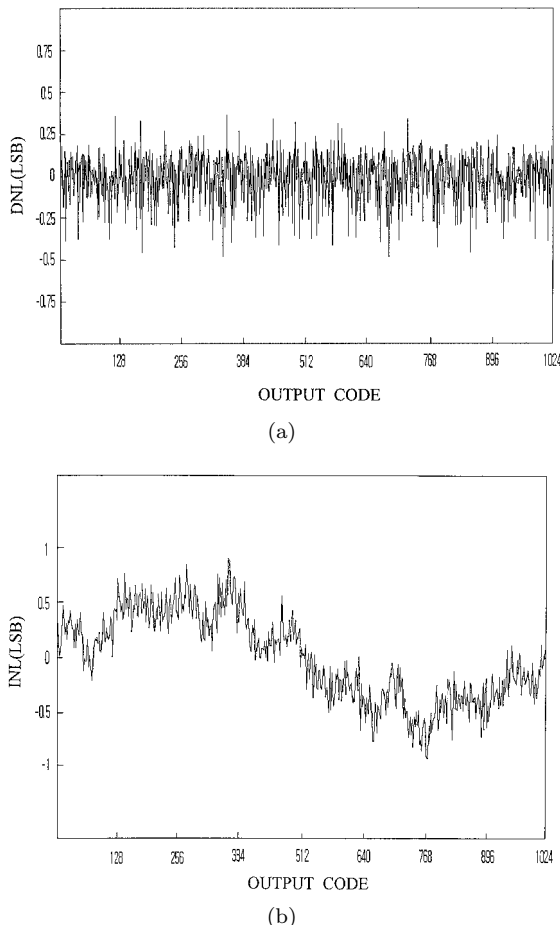
**Fig. 12** The measured output characteristic of the modular current reference circuit.



**Fig. 13** Chip photograph of the current predictor and modular current reference.



**Fig. 14** Plot of the total measured current versus the power supply voltage of the 10-bit current-mode A/D converter.



**Fig. 15** Plot of the measured (a) DNL error and (b) INL error as a function of the output codes.

clock and their magnitudes are amplified as the magnitude of the input current signal becomes larger. It can be seen in Table 1 that as the magnitude of the input current signal becomes larger, the magnitude of the

**Table 2** Summary of the measured results on the 10-bit A/D converter.

Resolution	10 bit
Conversion rate	10 Msamples/s
INL	$\leq \pm 1.0$ LSB
DNL	$\leq \pm 0.5$ LSB
Power dissipation	94 mW
Supply voltage	+5 V
Analog input range	$16 \mu\text{A} \sim 528 \mu\text{A}$
Technology	$0.6 \mu\text{m}$ CMOS n-well
Effective Chip area	$1.8 \text{ mm} \times 2.4 \text{ mm}$

current subtracted from the modular current reference circuit increases. The microphotograph of the modular current reference circuit with the current predictor is illustrated in Fig. 13. A curve of a total current versus a power supply voltage measured by HP 4145B in Fig. 14 shows the measured power consumption of 94.4 mW at the power supply of 5 V. The measured INL and DNL of the designed A/D converter, as shown in Fig. 15, are  $\pm 1.0$  LSB and  $\pm 0.5$  LSB, respectively. The maximum data conversion rate limited by  $\pm 0.5$  LSB of DNL is measured to be 10 Msamples/s. The measured performances of the designed A/D converter are summarized in Table 2.

#### 4. Conclusion

A 10-bit CMOS current-mode A/D converter with a current predictor and a modular current reference circuit was designed and successfully fabricated by the  $0.6 \mu\text{m}$  n-well double poly/triple metal CMOS technology. A current predictor and a modular current reference circuit in the 10-bit A/D converter are employed not only to reduce the number of comparator and reference current mirrors, but also to decrease a power dissipation. The measured power consumption, maximum data conversion rate, INL, and DNL of the designed A/D converter are 94.4 mW, 10 Msamples/s,  $\pm 1.0$  LSB, and  $\pm 0.5$  LSB, respectively.

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