A Model for the Analytical Definition of Multi-V_{DD}, Multi-T Dynamic Tests in Nanometer Digital Circuits

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***Abstract*—As IC technology scales down, interconnect issues are becoming one of the major concerns of gigahertz System-on-Chip (SoC) design. Voltage distortion (power supply noise) and delay violations (signal and clock skews) dramatically contribute to signal integrity loss. Temperature variations and gradients along the die, due to (variable) power consumption, also have a negative impact on SoC behavior. As a consequence, performance degradation, reliability problems and, ultimately, functional error occur. Detection of physical defects in emerging nanometer semiconductor technologies requires the detection of dynamic faults, namely delay test. In addition, process variations must be taken into account, leading to the specification of acceptability windows and time slacks. In previous works, it has been demonstrated that parametric tests using variable power supply voltage (multi-V_{DD} test) and temperature (multi-T test) can be rewardingly applied to production and lifetime test. In this paper, a simple analytical model to define those dynamic parametric tests and the resulting test strategy are presented. Faults are unrestrictedly defined to describe the impact of physical defects, system operation, process variations, un-modeled layout-dependent parasitics, etc. on the timing response of the Core Under Test (CUT) and modeled as variations of the load capacitances of logic gates with respect to their nominal values. Simulation results allow the capabilities of the proposed approach to be demonstrated.**

I. INTRODUCTION

DETECTION of physical defects in emerging nanometer semiconductor technologies is a challenging task, requiring static and dynamic test, namely delay test [1]. For static test, fault detection is associated with the occurrence of Boolean Differences in the Core Under Test (CUT). For dynamic test, timing (or performance) errors must be addressed. Hence, to screen out defective parts, logic values and timing responses (the time periods required by the circuit to respond to input test vectors) must be compared to their fault-free counterparts. Dynamic BIST (Built-In Self Test) is required, especially if lifetime self-test is part of product specification. Dynamic test must account for process variations, which drive the need to define acceptability windows (instead of single values), and to specify time slacks [2]. Device operation may introduce two additional sources of performance variations, whose impact on system performance must be accounted for: (1) power noise induces power supply voltage variations (ΔV_{DD}), and (2) power consumption induces thermal variations, including temperature gradients along the die.

The use of low values of V_{DD} for the detection of design flaws (Very Low Voltage testing, VLV) was proposed in [3][4]. VLV testing operates a CUT (Core Under Test) at reduced V_{DD} and speed to detect functional (logic), timing or power supply current (I_{DDQ}) failures. For instance, lowering V_{DD} eases the detection of resistive bridging defects. In fact, with VLV testing the pull-up / pull-down MOSFET on-resistances significantly increase with lower V_{DD} [5]. The detection of delay faults can also be improved by VLV test [6].

A multiple-clock scheme for the detection of delay faults at nominal V_{DD} has been proposed [7].

The authors have developed semi-empirical models which relate the variation of the propagation delay of logic gates (Δt_{pd}) and signal paths (ΔT_{pd}) with V_{DD} variations (ΔV_{DD}) [8], T variations (ΔT) [9] and both of them [10]. The formulation of the models has been proven to be loosely dependent on technology scaling, at least down to 130nm [11]. Based on these models, several approaches to multi-V_{DD} / multi-T dynamic tests (including BIST capabilities) have been proposed [12]-[14]. In particular, multi-V_{DD} BIST can take advantage of the infrastructure for Dynamic Voltage Scaling (DVS) [15] currently available in many microprocessor systems [16]-[19].

This paper addresses the definition of dynamic multi-V_{DD} / multi-T tests, in the sense of determining the values of (ΔV_{DD}, ΔT) which allow a given abnormal behavior to be detected. A simple semi-empirical model is presented, which can be used

to determine such values, taking into account: (1) the acceptability windows of process variations, (2) the magnitude of the target defects and (3) the magnitude of V_{DD} / T variations expected to occur during the operation of the CUT. Faults are unrestrictedly defined to describe the impact of physical defects, system operation, process variations, un-modeled layout-dependent parasitics, etc. on the timing response of the CUT. In the proposed model, such faults are represented by variations of the load capacitances of logic gates with respect to their nominal values.

The remainder of the paper is structured as follows. The basic concepts associated to multi-V_{DD}, multi-T dynamic tests are briefly described in Section II. The developed model and its application to dynamic test definition are the subject of Section III. Simulation results demonstrating the accuracy of the model and the capabilities of the proposed test strategy are presented in Section IV. Finally, Section V summarizes the conclusions of the work.

II. MULTI-V_{DD}, MULTI-T DYNAMIC TESTS

In this work, time slack is defined as the difference between the clock period (the time allowed for signal propagation) and the time interval associated with the response of the critical path (the slowest combinational module between registers).

Propagation delays in a logic circuit depend on local V_{DD} and T. In the design environment, logic simulation at nominal operating values, V_{DDnom} and T_{nom}, allows the logic and timing behavior of the circuit to be determined. The clock frequency is selected to guarantee a minimum time slack in worst-case conditions, taking into account that:

1) As V_{DD} and T may change, the impact of their variations on circuit's timing response must be characterized.

2) For nanometer technologies, very significant process variations must be expected to occur.

Typically, time slack values are conservatively defined to accommodate process variations for the maximum operating temperature, 90% of V_{DDnom} and *slow* MOS transistor models. As a result, the acceptable, fault-free, operating windows of the circuit can be determined.

In nanometer technologies, many hard-to-detect defects do not cause logic errors, but induce performance ones. Many physical defects inducing delay faults behave as parametric faults. For instance, the value of the resistance of a resistive short, or the way an interconnection node is split in two, in the presence of an open via, can induce different fault magnitudes (abnormal delay values). Parametric changes in the operating frequency, V_{DD} and T can be used to uncover physical defects causing abnormal delays, or distortions in the patterns of timing responses [12].

It has been shown that it is possible to back-annotate from electrical to logic level the impact of these parametric variations [20]. Models to compute the dependence of propagation delay variations (Δt_{pd}) of logic gates on V_{DD} variations (ΔV_{DD}) [8], T variations (ΔT) [9] and both of them [10] have been previously developed by the authors. In the Cadence design environment, the behavior of a long inverter chain can be simulated to compute, at electrical level, Δt_{pd} (ΔV_{DD}), Δt_{pd} (ΔT) or Δt_{pd} (ΔV_{DD}, ΔT) dependences. For each technology, model parameters are extracted once and reused to modulate the Δt_{pd} of library cells, whenever they are instantiated in the CUT netlist. Once Δt_{pd} is computed, the necessary variation of the maximum operating frequency (Δf_{max}), can be evaluated through the sum of individual delays in critical paths (ΔT_{pd}), which can be different from the ones at nominal operating conditions, in the case of local variations of V_{DD} or T. An industrial design, XTRAN (a fleet management system from Tecmic [21]), a combinational block with 13 inputs and 11 outputs, was used to validate the models through electrical simulation Experiments have also been conducted with level-sensitive latches and edge-triggered flip-flops.

Typical simulation results for a 130 nm technology are shown in Fig. 1. An IC has been fabricated in 0.6 µm technology to validate the models on a real platform.The comparison between measured values and those predicted by the $\Delta t_{pd}(\Delta V_{DD})$ model for a long inverter chain are depicted in Fig. 2. It can be clearly noticed that the model provides very accurate results, even for large V_{DD} depletion. Note that Fig. 2 illustrates that the model also accurately describes the behavior of I/O pads.

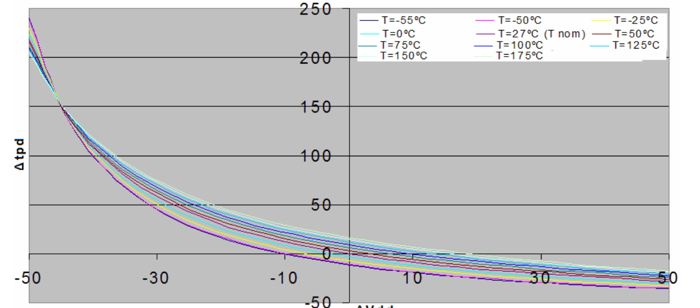

Fig. 1: Dependence of Δt_{pd} (%) on ΔV_{DD} (%) and ΔT for 130nm technology

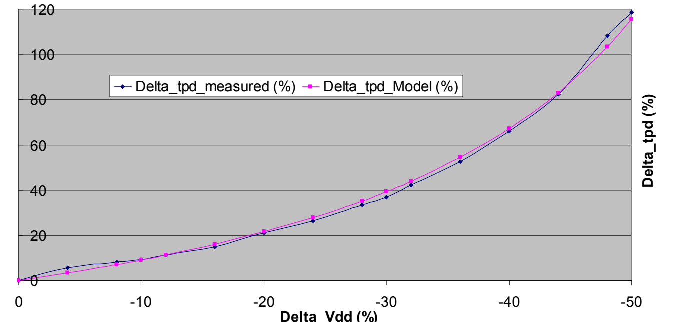

Fig. 2. Measurements vs. predicted behavior for a 76-inverter chain.

Interestingly, the models highlight the fact that the same value of Δt_{pd} can result from specific values of either ΔV_{DD} or ΔT. Fig. 3 shows the pairs (ΔV_{DDj}, ΔT_j) which produce the same Δt_{pd} value for the above mentioned 130 nm technology.

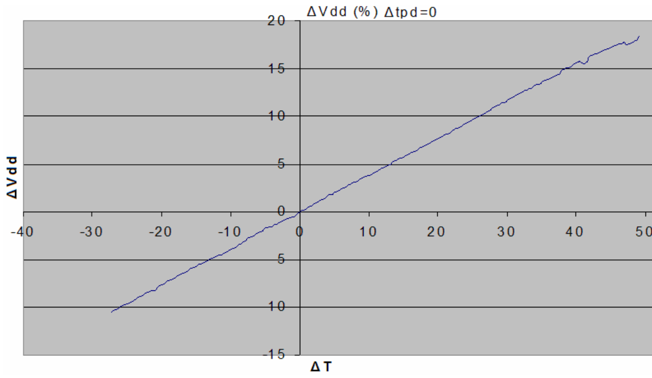

Fig. 3: Identical Δt_{pd} produced by either ΔV_{DD} (%) or ΔT (%) values

When V_{DD} decreases or T increases, the time slack is eroded, and performance errors may start to occur. The impact on the timing response of a physical defect causing a delay fault is amplified by decreasing V_{DD}, or increasing T, while keeping the clock frequency constant. A similar effect can be obtained for nominal values of V_{DD} and T by increasing clock frequency [22]. Advantage can be taken of this duality of effects for the development of efficient test strategies in the design phase as well as in the production floor or for lifetime test. In the design environment, multi-clock fault simulation can be a low-cost process (provided that a limited subset of discrete values of the clock frequency is used). However, at production or lifetime test, multi-clock test may require prohibitive costs. Alternatively, multi-V_{DD} self-test can become a rewarding technique, especially if multiple V_{DD} values are available on-chip (which is the case for products supporting DVS).

The advantages of using multi-clock and/or multi-V_{DD} test schemes for fault detection and diagnosis have been addressed in [12][14]. In [12], a histogram of the number of failing vectors, at each clock frequency, has been used. Failing vectors are the input vector pairs that trigger a switching behavior in the MOS network that induces performance errors at the observable outputs. With this technique, the ability to uncover delay faults (especially associated with defects outside the critical paths) and the diagnostic resolution were limited. In [14], advantage is taken of on-chip multi-V_{DD} and classic BIST hardware to perform signature-based multi-V_{DD} self-test and detect physical defects, with emphasis on resistive open and bridging defects, not only in critical paths but also in short paths (small-delay defects). Small-delay defects represent a significant reliability problem [23] as they are not detected by any of the two delay fault models widely used in industry, namely transition and path delay.

A relevant question to be considered for nanometer circuits is the accuracy of the results obtained through simulation. Using only nominal (typical) parameters is not enough, as process variations are quite large in these technologies. Monte Carlo simulations may be needed to validate the results, which can be a hard work.

Another important issue is to develop fault models which allow the easy and accurate derivation of the values of V_{DD} and T to be applied for a given defect to be detected in a real circuit.

In next Section, a new approach to define multi-V_{DD}, multi-T tests is presented, based on an extension of the previously developed models. It allows not only defects, but also process variations, as well as power supply noise and temperature variations to be integrated in the definition of the tests.

III. Analytical Definition of Multi-V_{DD} / Multi-T Tests

A. Modeling of delay faults and process variations

Physical defects, device operation or inaccurate parasitic modelling may induce dynamic faults on a nanometer SoC. System operation may induce power supply voltage and temperature variations. Variable V_{DD} may disturb the efficiency of the clock distribution network, thus influencing the on-chip clock frequency. Hence, the word "fault" is used throughout this work in a broad sense. It describes not only the impact of physical defects on circuit performance, but also the impact of system operation, process variations, un-modeled layout-dependent parasitics, etc. on timing behavior.

Like in previous works, the transient response of static CMOS gates is analyzed as the response of an equivalent inverter [24][25]. Hence, any input transition that toggles the output, activates a pull-up or pull-down path, corresponding to the activation of an equivalent PMOS or NMOS transistor. Static V_{DD} values are assumed during the equivalent inverter's switching. The remaining simplifying assumptions below have also been used for the development of the former models, with excellent results, as Fig. 2 demonstrates.

The average propagation delay of a balanced inverter, t_{pd}, under an instantaneous input voltage transition (step) can be computed as follows. Let us assume that the switching transistor operates with a constant drain current (saturation region), charging (or discharging) the load capacitance, C_L. The approximate equation for t_{pd} is given by

$$t_{pd} = \frac{C_L V_{DD}}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})^2} \quad (1)$$

where symbols retain their usual meanings. V_{th} and μ are the average values of the threshold voltage (V_{thp} and V_{thn}) and of the majority carrier mobility (μ_p and μ_n) of the PMOS and NMOS transistors, respectively.

As models are defined for relative variations, i.e.,

$$\Delta X = \frac{X - X_{nom}}{X_{nom}} \quad (2)$$

it is clear that the Δt_{pd} (ΔV_{DD}, ΔT) model is independent of C_L, providing C_L is kept constant, which is approximately the case for a fault free circuit. It is well known that the parasitic capacitances of MOS transistors depend on the bias conditions

(and, hence, on V_{DD}) and on T. However, it has been demonstrated in [8]-[10] that this dependence can be accommodated by the parameters of the models.

In current nanometer CMOS technologies, resistive defects are among the most common ones. Their effect combined with the various parasitic capacitances of the circuit can be modeled as a variation of the time constant R·C of the path affected by the defect, leading to delay faults. Even if resistive in nature, from a modeling point of view the same results can be obtained by keeping R constant and modifying C. It is important to note that the effects of process variations causing a modification of the propagation delays of the CUT can be also modeled as capacitance variations with respect to nominal (or other reference) conditions. In the following, the joint effect of process variations and defects is encapsulated in the term ΔC_L, i.e., they are easily modeled as a variation of the load capacitance of the equivalent inverter.

Once C_L is no longer assumed to be constant, the effect of its variations has to be included in the Δt_{pd} (ΔV_{DD}, ΔT) model. Let us first derive the Δt_{pd} (ΔC_L) model. From Eq. (1), and for constant V_{DD} and T, it follows:

$$\Delta t_{pd}(\Delta C_L) = \frac{\lambda \cdot C_L - \lambda \cdot C_{Lnom}}{\lambda \cdot C_{Lnom}} = \frac{C_L - C_{Lnom}}{C_{Lnom}} = \Delta C_L \quad (3)$$

where

$$\lambda = \frac{V_{DD}}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})^2}$$

Results in Section IV demonstrate that Eq. (3) is a good approximation but, taking advantage of its simplicity, its accuracy can be improved by including a correction parameter ζ, in the form:

$$\Delta t_{pd}(\Delta C_L) = (\Delta C_L)^{\zeta} \quad (4)$$

where ζ (ΔV_{DD}, ΔT) is empirically found to be very close to unity, as discussed in next Section.

The full model can be also derived from Eq. (1):

$$\Delta t_{pd}(\Delta V_{DD}, \Delta T, \Delta C_L) = \frac{\lambda \cdot C_L - \lambda_{nom} \cdot C_{Lnom}}{\lambda_{nom} \cdot C_{Lnom}} = \frac{\lambda}{\lambda_{nom}} \cdot \frac{C_L}{C_{Lnom}} - 1 \quad (5)$$

where $C_L / C_{Lnom} = 1 + \Delta C_L$.

Using the model proposed in [10] and taking into account Eq. (4), it yields:

$$\Delta t_{pd}(\Delta V_{DD}, \Delta T, \Delta C_L) = \frac{1 + (\Delta C_L)^{\zeta}}{1 + \Delta\mu(\Delta V_{DD}, \Delta T)} \cdot \frac{(1 + \Delta V_{DD})(1 - \alpha)^2}{(1 + \Delta V_{DD} - \alpha)^2} - 1 \quad (6)$$

where $\alpha = V_{th}/V_{DDnom}$ is a technology-dependent parameter, whereas $\Delta\mu$(ΔV_{DD}, ΔT) and ζ(ΔV_{DD}, ΔT) are empirically obtained during the setup of the model for a given technology.

B. Test strategy

As stated above, in this work a fault is unrestrictedly defined to describe the impact of physical defects, system operation, process variations, un-modeled layout-dependent parasitics, etc. on the timing response of the CUT. Faults are modeled with values of $\Delta C_L > 0$.

From Eq. (6), the fault-free behavior of the CUT is defined by Δt_{pd} (ΔV_{DD}, ΔT, 0). For a fault of a given equivalent magnitude ΔC_{Lf}, the faulty behavior in nominal operating conditions (V_{DDnom}, T_{nom}) can be computed as Δt_{pd} (0, 0, ΔC_{Lf}). In some cases, the result will be the increased delay exceeding the time slack and, therefore, these faults could be uncovered by a test performed at (V_{DDnom}, T_{nom}). For the remaining cases, Eq. (6) allows to determine whether or not there exists a 3-tuple (ΔV_{DD}, ΔT, ΔC_{Lf}) which makes the fault detectable. The underlying idea is that, in the presence of any cause inducing a delay fault, performance degradation (due to lower V_{DD} or higher T) is sufficiently different from the one observed in fault-free operation as for fault detection to be possible. This, of course, depends on the magnitude of the fault.

The applicability limit of this test strategy is the need for large negative ΔV_{DD} values that would cause functional collapse and / or large positive ΔT values that would damage the CUT. This relates to the minimum magnitude of the fault that can be detected but, very interestingly, do not limit the application to faults occurring in critical paths only, which makes detection of small-delay defects possible.

Of course, suitable test vectors must be found that sensitize the paths in which the fault is located, but test pattern generation for delay faults is out of the scope of this work.

This approach can be used at nominal operating frequency, in order for the cost of production or lifetime test to be reduced. Detection could be further improved by using several testing frequencies, as they could be fitted to accommodate the magnitude of the fault and the corresponding Δt_{pd}.

A practical limitation that could (but in fact does not, as explained below) affect the proposed solution is the existence of situations in which, as V_{DD} and / or T are modified during the test, they take the values (ΔV_{DD1}, ΔT_1) before reaching the target ones (ΔV_{DD2}, ΔT_2), and $\Delta t_{pd}(\Delta V_{DD1}, \Delta T_1, 0) \geq \Delta t_{pd}(\Delta V_{DD2}, \Delta T_2, \Delta C_{Lf})$. This means that in some circumstances the fault-free (ΔC_L=0) delay would be larger than the faulty one and, therefore, it would be possible to incorrectly flag a fault-free circuit as faulty. However, as ΔC_L>0 causes delay to increase, incorrect detection could only occur if $V_{DD1}<V_{DD2}<V_{DDnom}$ or $T_1>T_2>T_{nom}$. By making V_{DD} (T) evolve from nominal to lower (higher) values during the test, incorrect detection will never occur, as the taget test points will be reached before those causing the problem.

IV. Simulation Results

In order for the new model to be validated, extensive electrical simulations have been conducted for several combinational circuits in 0.35 μm technology, using the Cadence design environment.

For the sake of simplicity, the results presented here have been obtained for a short 5-inverter chain. Fig. 4 shows simulation results for the third inverter in the chain, C_{Lnom} being the input capacitance of the next inverter.

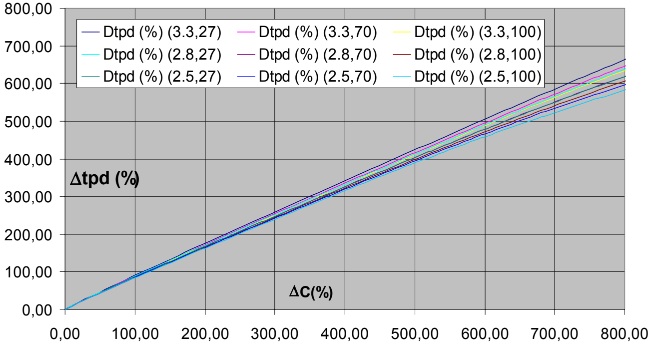

Fig. 4. Simulated Δt_{pd} (ΔC_L) behavior for a 0.35 μm technology, third on a 5-inverter chain.

All curves in Fig. 4 are quite close to the unity slope straight line defined by Eq. (3). This is an important result, which demonstrates that the dependence of the Δt_{pd} (ΔC_L) model on V_{DD} and T is not very strong, providing they are kept constant while ΔC_L changes. This is similar to what happens with the Δt_{pd} (ΔV_{DD}, ΔT) model for constant C_L, as stated in Section III-A.

Although the maximum error of the basic model is about 15%, it should be noted that it happens for $\Delta C_L \approx 800\%$, a very high value for which functional breakdown occurs, as the inverter is not sized to manage such load and the waveforms are totally distorted. For ΔC_L=300%, the maximum error is about 6%.

In order to use the model defined by Eq. (4), the correction parameter ζ has to be empirically determined. Fig. 5 shows the values of ζ for a wide range of (ΔV_{DD}, ΔT). The average and maximum errors of this modified model are 1.4% and 4.3%, respectively. It is important to note that the values of ζ are nearly constant and close to unity. If the model is simplified by considering a constant value of ζ=0.9635, the average and maximum errors are 2.7% and 7.3%, respectively.

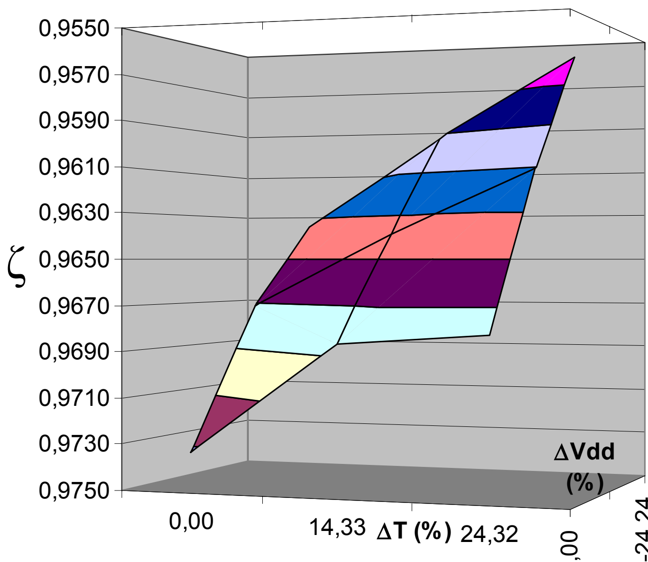

Fig. 5. Correction parameter ζ (ΔV_{DD}, ΔT) for a 0.35 μm technology

In order to illustrate the feasibility of the proposed test strategy, Fig. 6 depicts simulation results at room temperature for both the fault-free and a sample (ΔC_L=33%) faulty condition. It can be clearly noticed that the difference in propagation delays is large enough as to allow both situations to be differentiated. Assuming a 10% time slack and the fault occurring in a path with propagation delay 20% shorter than the critical path, the fault will be detected at nominal frequency by decreasing the power supply voltage to ΔV_{DD}=-5% (while, of course, sensitizing the path). Detection will take place even if the test vectors sensitize also the critical path, because the increase of its propagation delay would still be lesser than the time slack.

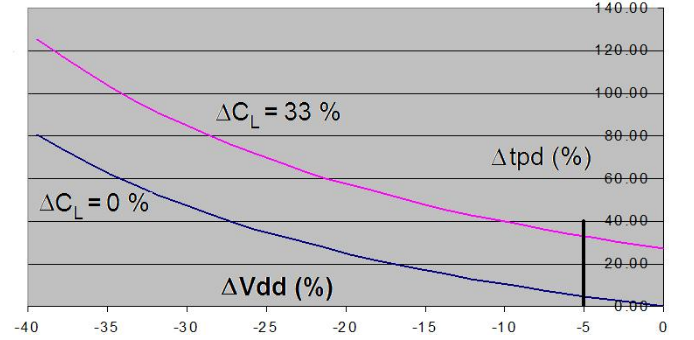

Fig.6. Simulated Δt_{pd} (%) vs. ΔV_{DD} (%) for ΔT = 0 (T = 27ºC), under fault-free (bottom plot) and faulty (upper plot, ΔC_L = 33%) conditions, third on a 5-inverter chain, 0.35 μm technology.

Very interestingly, even for this sample fault of relatively low magnitude (taking into account that it encapsulates physical defects, process variations, etc.), Δt_{pd} is much higher than the maximum error of the developed model, which could therefore be used, as intended, to specify the conditions (i.e., the values of V_{DD} and T) of the parametric tests.

V. CONCLUSION

Multi-V_{DD}, multi-T tests can be rewardingly applied to production and lifetime test of digital nanometer circuits. In order for these tests to be efficiently carried out, it is necessary to develop fault models which allow the easy and accurate derivation of the values of V_{DD} and T to be applied for a given defect to be detected in a real circuit.

A simple yet accurate semi-empirical model has been derived, as an extension of previously developed ones (whose capabilities have already been demonstrated in a real circuit for which results have been presented), to formulate the dependence of propagation delay time variations of logic elements, Δt_{pd}, on the variations of power supply voltage (ΔV_{DD}), temperature (ΔT) and load capacitance (ΔC_L). This latter parameter allows faults to be modeled for unrestrictedly describing the impact of physical defects, system operation, process variations, un-modeled layout-dependent parasitics, etc. on the timing response of the CUT.

Detectable delay faults are those whose magnitude, at a given testing frequency (only the nominal one if test cost is to be minimized), exceeds the time slack of the path they affect, therefore causing a system timing failure. Hence, the effectiveness in uncovering a path delay fault strongly depends on the path's propagation delay and the defect size. In a multi-V_{DD}, multi-T test scenario, the developed model allows to compute the values of V_{DD} and T that would make a fault detectable.

Simulation results supporting the claimed contributions of this work have been presented. An important practical advantage of the proposed test strategy is that it makes the detection of small-delay defects feasible, as it can be applied to faults affecting any path of the CUT, critical or not.

This approach can be combined with other novel testing techniques developed by the authors, as the signature-based multi-V_{DD} self-test taking advantage of DVS infrastructures.

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REFERENCES

[1] K.-T. Cheng, S. Devadas, K. Keutzer, "Delay Fault Test Generation and Synthesis for Testability under a Standard Scan Design Methodology", *IEEE Trans. on CAD of Int. Circs. and Systems*, vol. 12, nº. 8, pp. 1217-1231, August 1993.

[2] A. Krstic, L.-C. Wang, K.-T. Cheng, J.-J. Liou, T. M. Mak, "Enhancing diagnosis resolution for delay defects based upon statistical timing and statistical fault models", *Proc. of the 40th. Design Automation Conf. (DAC)*, pp. 668 – 673, 2003.

[3] H. Hao, E.J. McCluskey, "Very-Low-Voltage Testing for Weak CMOS Logic ICs", *Proc. Int. Test Conf.*, pp. 275-284, 1993.

[4] Jonathan T.-Y. Chang and E. J. McCluskey, "Detecting Delay Flaws By Very-Low-Voltage Testing", *Proc. Int. Test Conf.*, 1996.

[5] Y. Liao and D. M. H. Walker, "Fault Coverage Analysis of Physically-Based Bridging Faults at Different Power Supply Voltages", *Proc. Int. Test Conf.*, 1996.

[6] P. Franco and E.J. McCluskey, "Delay Testing of Digital Circuits by Output Waveform Analysis", *Proc. Int. Test Conf.*, pp. 798-807, 1991.

[7] J.-J. Liou, L.-C. Wang, K.-T. Cheng, J. Dworak, M.R. Mercer, R. Kapur, T.W. Williams, "Enhancing Test Efficiency for Delay Fault Testing Using Multiple-Clocked Schemes", *Proc. of 39th. Design Automation Conference (DAC)*, pp. 371-374, June 2002.

[8] M. Rodriguez-Irago, J.J. Rodríguez-Andina, D. Barros Júnior, F. Vargas, M. B. Santos, I.C Teixeira and J. P. Teixeira, "Using Multiple Clock Schemes and Multi-V_{DD} Test for Dynamic Fault Detection in Digital Systems", *Proc. IEEE Latin American Test Workshop (LATW)*, 2005.

[9] M. Rodríguez-Irago, J.J. Rodríguez-Andina, F. Vargas, I.C. Teixeira, J.P. Teixeira, "Using Multiple-Clock Schemes and Multi-T Test for Dynamic Fault Detection in Digital Systems", *Proc. IEEE Latin American Test Workshop (LATW)*, 2006.

[10] M. Rodríguez-Irago, J.J. Rodríguez-Andina, F. Vargas, I.C. Teixeira, J.P. Teixeira, "On the Use of Multi-Clock, Multi-V_{DD} and Multi-Temperature Schemes to Improve Dynamic Fault Detection in Digital Systems", *Proc. IEEE European Test Symposium (ETS)*, Informal Digests, May 2006.

[11] M. Rodríguez-Irago, J.J. Rodríguez-Andina, F. Vargas, M.B. Santos, I.C. Teixeira, J.P. Teixeira, "Multiple-Clock and Multi-V_{DD} Schemes for Dynamic Fault Detection in Nanometer Digital Circuits", *Proc. Conf. Design of Circuits and Integrated Systems (DCIS)*, 2005.

[12] M. Rodriguez-Irago, J.J. Rodriguez-Andina, F. Vargas, M.B. Santos, I.M. Teixeira and J. P. Teixeira, "Dynamic Fault Test and Diagnosis in Digital Systems using Multiple Clock Schemes and Multi-V_{DD} Test", *Proc. 11th IEEE Int. On-Line Test Symp. (IOLTS)*, pp. 281-286, 2005.

[13] M. Rodríguez-Irago, J.J. Rodríguez-Andina, F. Vargas, J. Semião, I.C. Teixeira, J.P. Teixeira, "Dynamic Fault Detection in Digital Systems Using Dynamic Voltage Scaling and Multi-Temperature Schemes", *Proc.12th IEEE Int. On-Line Test Symp. (IOLTS)*, July, 2006.

[14] J. Semião, M. Rodriguez-Irago, J.J. Rodriguez-Andina, F. Vargas, M.B. Santos, I.M. Teixeira and J. P. Teixeira, "Resistive Open and Bridging Defects Detection in Digital Systems Using Multi-V_{DD} Self-Test", *Proc. Conf. Design of Circuits and Integrated Systems (DCIS)*, 2006.

[15] T. Pering, T. Burd, and R. Brodersen, "The Simulation and Evaluation of Dynamic Voltage Scaling Algorithms." *Proc. of Int'l Symposium on Low Power Electronics and Design (ISLPED)*, pp. 76-81, June 1998.

[16] ARM / IEM, http://www.arm.com/products/esd/iem_home.html

[17] IBM PowerPC, http://www.chips.ibm.com/products/powerpc/

[18] Intel XScale. http://www.intel.com/design/intelxscale/

[19] Transmeta Crusoe. http://www.transmeta.com/technology/index.html

[20] D. Barros Júnior, F. Vargas, M.B. Santos, I.C. Teixeira, J.P. Teixeira. "Modelling of Power Supply Transients for EMI Compliance in Digital Systems". *Proc. 10th IEEE Int. On-Line Test Symp. (IOLTS)*, pp. 5-9, 2004.

[21] Tecmic, http://www.tecmic.pt/eng/index.html

[22] D. Barros Júnior, M. Rodríguez-Irago, M.B. Santos, I.C. Teixeira, F. Vargas, J.P. Teixeira. "Fault Modelling and Simulation of Power Supply Voltage Transients in Digital Systems on a Chip". *JETTA*, vol. 21, pp. 349-364, 2004.

[23] N. Ahmed, M. Tehranipoor, V. Jayaram, "Timing-Based Delay Test for Screening Small Delay Defects", *Proc. Design Automation Conf (DAC)*, pp. 320-325, 2006.

[24] M. Bafleur, J. Buxo, J.P. Teixeira, I.C. Teixeira, "Physical Macromodeling of the Dynamic Behaviour of CMOS VLSI Circuits", *Microelectronics Journal*, vol. 23, no. 8, pp. 599-623, 1992.

[25] C. Metra, S. Di Francescantonio, T.M. Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing", *IEEE Transactions on Computers*, vol. 53, no. 5, pp. 531-546, May 2004.