Impact of NBTI on FPGAs *

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Abstract

Device scaling such as reduced oxide thickness and high electric field has given rise to various reliability concerns. One such growing issue of concern is the degradation of PMOS devices due to Negative Bias Temperature Instability (NBTI). NBTI has detrimental effects on the threshold voltage of the PMOS transistor thereby leading to lower performance and noise degradation over time in digital systems. The degradation is measured as reduction in Static Noise Margin (SNM) of SRAM cells in memories and as timing impact in digital circuits. In this work, we provide a comprehensive analysis of the impact of NBTI on different components for current and future generation FPGAs. We provide solutions based on the reversible nature of this phenomenon and the static probabilities at the gate of the PMOS devices in any system.We recover an average of 53.2% of the lost SNM and improve the FIT rate by 2.48% for a X4VFX40 device by using our proposed method.

1 Introduction

Field Programmable Gate Arrays (FPGAs) have been aggressive with their scaling trends primarily due to tremendous advantages provided by them in the form of low NRI costs and symmetric designs. However, the limitations due to the basic physical nature of devices have become quite evident with aggressive scaling of technology [1]. Consequently, apart from the well researched issues of power,performance and process variations,the biggest threat with minuscule feature sizes is their reliability concerns. Reliability issues such as Electromigration(EM), Hot Carrier Effects(HCE), Time Dependent Dielectric Breakdown (TDDB) and Negative Bias Temperature Instability(NBTI) tend to pose serious problems as technology scales. In particular, there has been recent increasing interest on the impact of NBTI on PMOS transistors [2] [3]. In this paper, we analyze the impact of NBTI on various components of a FPGA and provide solutions to subsidize the effect.

Negative Bias Temperature Instability (NBTI) is an important phenomenon which leads to slow degradation of PMOS transistors in the design. NBTI occurs under negative bias conditions (V_{gs}=-V_{dd}) at high temperatures. Interface traps are generated due to disintegration of Silicon-Hydrogen (Si-H) bonds under these conditions which result in increase in the threshold voltage ($|V_{th}|$) and reduction in on-current(I_{on}) of the PMOS device. This phenomenon aggravates as the oxide thickness scales further due to its strong dependence on the electric field across the gate oxide. The increased thresholds of the devices however can be reduced during the recovery phase when the PMOS is not conducting (V_{gs} = 0). There has been quite a bit of recent analysis of NBTI both on the front of model development and impact analysis on circuits. The impact is separately analyzed in memory elements and logic circuits separately. Such analyses focuses on both the performance and the stability of the circuits.

FPGAs typically use memory elements in the form of 6T SRAM cells to store the configuration bits encoding the hardware. Such memory elements storing the configuration bits, once configured for some designs usually reside in the same state for long periods of time. Although the read/write delays of such cells are of no consequence in FPGAs, their stability is of prime concern due to the criticality of such configuration cells. The continuous stressing of the PMOS device in a memory cell decreases the stability of the cells gradually. Such instability is quantified in terms of reduced Static Noise Margins (SNM) of the cell. Reduced stability increases the vulnerability of the SRAM to noise and transient errors like soft errors, which is a prime concern in such devices. Apart from the stability of the device, the increased threshold voltage can lead to increased delays of the individual circuits, thereby affecting the timing constraints of the design implemented in them. These critical problems have been analyzed comprehensively and addressed with some novel solutions in this work.

The contributions of this paper include, (a) Analyzing the impact of NBTI on different components of FPGAs over time (b) Observing the performance and stability of the device and applications mapped on the devices (c) Solutions to counter such problems by effective interleaving of stress and recovery cycles.

The rest of the paper is as follows. Section 2 talks about the related work.The modeling of NBTI is done in section 3. The impact of NBTI on FPGA has been explained in section 4. Section 5 focusses on the novel mitigation techniques to reduce the effect of NBTI and it's results. Section 6 concludes the paper.

2 Related Work

Technological trends and various reliability problems are been discussed in [1]. Some of the prime reliability problems attributed to aging and permanent damage and their trends with scaling of technology are presented in [4]. The phenomenon of NBTI has been discussed along with the Reaction-Diffusion model in [5]. This impact of NBTI on the stability a[illegible]

*This work is supported in part by NSF Career Award 0093085, NSF grants 0454123,0202007 & MARCO GSRC

formance of memories was presented in [6]. The work demonstrated significant impact of NBTI on the stability of the SRAM cells in the form of SNM degradation. However, not much impact was observed in the read/write delays of the memory cell. The performance degradation of circuits due to NBTI has been discussed in [7], where the delay of logical circuits at a higher technology node is shown to degrade by 9% over a period of 10 years. FPGAs have been analyzed for permanent faults in [8], however the impact of NBTI has not been studied. So, to the best of authors' knowledge,this is the first work that studies the impact of NBTI on FPGAs. Our work provides a stability analysis and the performance impact of NBTI on different components of FPGAs. Degradation in SNM of configuration bits of the FPGAs may impact the susceptibility of the FPGAs to transient errors. The criticality of FPGAs in space applications has always called for guarding the configuration bits to radiation impacts [9]. Consequently, such an analysis and solutions proposed by us in this work are of prime importance.

3 NBTI Modeling

Till date, research on NBTI has been active in the fields of device and reliability physics. There have been different models worked upon in [10] [11]. The most commonly employed stress model is the Reaction Diffusion (R-D) model [5] with fine modifications for technologies. We use the stress and the recovery equation as shown in equations from [12] for estimating the change in threshold voltage ΔV_{th} after a period of time.

At Stress,

$$\Delta V_{th} = \sqrt{K_v^2.(t-t_0)^{0.5} + \Delta V_{th1}^2} + \delta_v \quad (1)$$

At Recovery,

$$\Delta V_{th} = (\Delta V_{th2} - \delta_v).\Big(1 - \sqrt{\eta(t-t_0)/t}\Big) \quad (2)$$

where

$$K_v = A.T_{ox}.\sqrt{C_{ox}(V_{gs}-V_{th})}.exp\Big(\frac{E_{ox}}{E_o}\Big).$$
$$\left(1 - \frac{V_{ds}}{\alpha(V_{gs}-V_{th})}\right).exp\Big(-\frac{E_a}{kT}\Big) \quad (3)$$

where E_{ox}=$(V_{gs}-V_{th})/T_{ox}$ and k the Boltzmann constant. The value of the coefficients are E_o=2.0 MV/cm, Ea=0.12 eV, A=1.8 mV/nm/$C^{0.5}$, $\eta = 0.35$ and δ_v=5mV. δ_v is a constant added to include the impact of oxide traps and other charge residues. Note that during the continuous operation of the circuit however, the device is under both stress and recovery based on the gate inputs' static probability or the duty cycle. The change in threshold voltage for long term degradation after 'n' cycles of stress and recovery is obtained from equation 4. These equations are used in conjunction with the PTM 90, 65 and 45 nm technologies [13] and all the simulations were performed at 100 °C.

$$\Delta V_{th} = K_v.\beta^{0.25}.T^{0.25}.$$
$$\left(\frac{1-(1-\sqrt{\eta(1-\beta)/n})^{2n}}{1-(1-\sqrt{\eta(1-\beta)/n})^2}\right) + \delta_v \quad (4)$$

where β is the duty cycle(ratio of time of stress to stress+recovery) and T is the clock period. Figure 1 shows the results obtained using the equation 1 for different technology nodes at 100 °C. It could be observed from the figure that the threshold voltage rise of the PMOS transistor is close to 10% for the period of 10^8 seconds (∼3 yrs), which clearly indicates the severity of the problem.

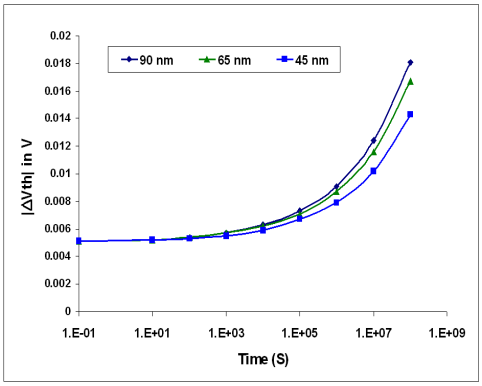

Figure 1. ΔV_{th} Variation of different technology nodes with age

Another important observation is the strong dependence of ΔV_{th} on the electric field, T_{ox} and temperature, which however are absent in the recovery equation. Such a bias significantly impacts the aging due to NBTI with technological fluctuations or process variations. Figure 1 shows the degradation in threshold of the PMOS (for V_g=V_{dd} as in table 1)after a period of ∼3yrs for three different technology nodes (Note that ΔV_{th} starts with 5mV due to δ_v). It is important to note that the change in threshold ΔV_{th} decreases as technology scales. This is due to the fact that the electric field across the gate oxide decreases for future technologies (since $(V_{gs}-V_{th})$ scales down faster compared to T_{ox} as shown in table 1) [13].

4 NBTI Analysis in FPGAs

FPGAs have many distinct features which require the analysis of each of its components separately with respect to the NBTI problem. The prime components under analysis in this paper are the configuration SRAMs, level restorers, buffers,flip flops and latches. The analysis is specifically targeted at current and future FPGA technologies, i.e, 65 nm and 45nm gate length devices. Each of the components affect the FPGAs in a different manner and is studied in detail in the following sections. The components used in our studies typically resemble the design used commonly by most FPGA vendors.

Table 1. Technology Parameters [13]

Technology Node(nm)	180	130	90	65	45	32
V_{dd} (V)	1.5	1.3	1.2	1.1	1.0	0.9
V_{th} (V)	0.22	0.2	0.2	0.2	0.2	0.2
T_{ox} (nm)	3.0	2.25	2.05	1.85	1.75	

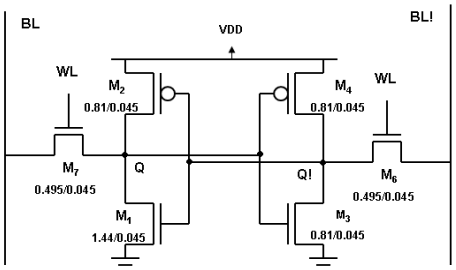

Figure 2. Nominal 6T SRAM Cell

4.1 Configuration Bits

Most FPGAs store their configuration bits in 6T SRAM cells as shown in the figure 2.Such configuration SRAM cells are used to store both the logic in the form of Look Up Table(LUTs) and the routing information for controlling the routing switches. Since the configuration of the device stays the same once programmed, the SRAM cells hold a value for long periods of time up until the FPGA is re-configured. Such a scenario leads to stressing of one of the PMOS transistors in the SRAM cell without recovery. Since the configuration SRAM cells are not in the critical path their timing degradation does not impact the performance of the application but it does affect the overall stability of the SRAM cell. Using the equation 1, we obtain the V_{th} degradation of a PMOS device while the value stored by the SRAM cell does not change. The severity of the problem in configuration bits is however subsidized a little due to the usage of medium-oxide (one of the triple-oxide thickness) [14] gates to reduce leakage ower in FPGAs. We performed our experiments on such SRAM cells to obtain the degradation in the device's SNM, read and write delays.

The performance degradation of a 45 nm degraded SRAM was studied. It was observed that the read delay is almost unaffected while the write delay improves slightly and is in consonance with [6]. Figure 3 demonstrates a graph of SNM degradation of SRAM cells for three technology nodes. It also shows the degradation for three different oxide thicknesses (for triple-oxide thicknesses of Xilinx) for a 45nm technology node over a period of 10^8 seconds ($\sim$3 yrs). Note that even in the thickest of gate oxides, the SNM degrades by 2% which is quite significant with respect to the read stability of the SRAM cell [6]. Increasing manufacturing uncertainty leading to variable oxide thicknesses may have a significant impact on the time to failure of different devices and impact the reliability yield of the chips.

Moreover, the degradation in the SNM values not only decreases the stability of the SRAM cell, but also increases the vulnerability of transient errors like soft errors, crosstalk etc. Therefore, it is imperative to analyze the soft error susceptibility of the affected SRAM cells. Critical charge Q_c is defined as the minimum charge that should be generated by the strike to cause an upset. Table 2 analyzes the impact of NBTI on the susceptibility of the SRAM cell to soft errors. It is observed that the critical charge (Q_c) decreases as the PMOS transistor gets degraded over time. Critical Charge (Q_c) for flipping a bit Q from 1→0 is lesser than 0→1 due to wider N^+ diffusion of the NMOS as shown in the figure 2.The Q_c for 0→1 is nearly unaffected since the strike occurs at Q! and the affected PMOS lies in the regenerative side in this case. We observe that Q_c for the bit flip from 1→0 decreases as the PMOS device gets affected due to NBTI. This arises due to the asymmetry in the affected cell. The affected PMOS transistor with its degraded current drive fails to bring back the node to 1 easily than the unaffected device. We also calculate the FIT rate (FIT is 1 failure in 10^9 hours of operation) of the degraded device using the model presented in [15]. A conventional SRAM's FIT rate is assumed to be 1000 FIT/MBit. Q_s which is the slope transformation factor is derived from [15] to be 4fC. The new FIT/MBit calculated of degraded SRAM is higher showing lesser resilience to errors.

Table 2. Critical Charge (Q_c) and FIT/MBit of Nominal and NBTI affected 45 nm SRAM Cell after 1 Year

	Bit	Flip	Nominal SRAM	Degraded SRAM
Q_{crit}	Q=1	0→1	11.244 fC	11.245 fC
	!Q=0	1→0	9.5366 fC	9.3896 fC
FIT /Mbit			1000	1037.5

4.2 Level Restorers and Buffers

Buffers and level restorers are commonly used in the FPGA interconnect circuitry. The interconnect circuitry comprise of multiplexers whose switches are stored in the configuration SRAM cells. FPGA interconnect multiplexers typically comprise of pass transistors, which need a level restorer and buffers to retain the signal high as shown in figure 4. Such components are in the critical path of the applications and hence may impact the timing of the applications implemented on the FPGA. An analysis of the delay increase in a level restorer with the increase in the V_{th} of the PMOS gates, is presented in figure 5. However, estimating the delay increase in an application requires us to know the static probabilities at the different gates of level restorers and buffers in the device for a given application followed by obtaining the degradation of PMOS devices. Then the delay impact is calculated using the obtained ΔV_{th}s. The different ΔV_{th} for all the transistors are calculated for different duty cycles varying from 0.1 to 0.9 (Note that the duty cycle of of M_2 is β and of M_r and M_4 is (1-β) in figure 4) and the corresponding delays after one year of operation at the frequency of 100 MHz. The different duty cycles capture the effect of different static probabilities at the input of the level restorer and buffer.

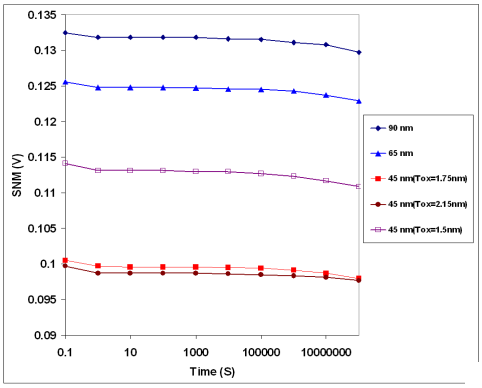

Figure 3. Variation of SNM with Age

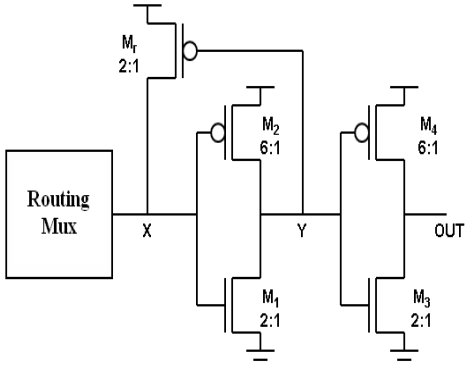

Figure 4. Level Restorer and Buffer

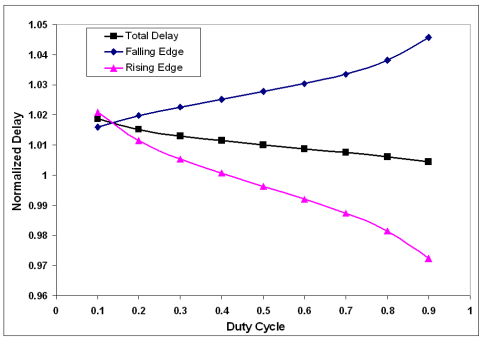

Figure 5. Impact of Duty cycle on Delay of Level Restorer and Buffer

Figure 5 shows the delays for rising edge, falling edge and the total delay. We observe that the level restorer plays a critical role in determining the speed of the circuit. The rising edge and falling edge shows different trends due to different ΔV_{th}s for varying values of β and also the effect of level restorer in pulling up node X to '1' with increased thresholds. The total delay decreases as β increases from 0.1 to 0.9 (Note that this delay is still higher than the normal delay).

To analyze such an impact of NBTI on the performance of the circuits we use a set of 9 MCNC benchmarks. Based on the static probabilities of different routing elements and the level restorer degradation results presented in figure 5, we compute the degradation in the speed of the routers. The new delays are employed to obtain the performance degradation of the applications mapped on to the device over a period of time. We use the open source Versatile Place and Route (VPR) tool [16] to perform our experimentation. The critical path delay is computed after a period of 1 year for different benchmarks and plotted in figure 6 with the original delays annotated at the top. It is evident that all the benchmarks have an average increase in the critical path delay by 6.63%.

4.3 Flip Flops and Latches

Flip Flops and latches are predominantly used in I/O Blocks and Combinational Logic Blocks (CLBs). The register elements used in these blocks are edge-triggered D flip flops or level sensitive D latches. We implemented Transmission gate based D flip-flop and D latches. The static probabilities of each internal node was calculated to be 0.5 and the corresponding ΔV_{th} for each of the PMOS at the end of one year is estimated using equation 4 at f=100MHz. The total delays after one, two and three years of operation for the flip-flops and latches are estimated using HSPICE and are shown in figure 7.

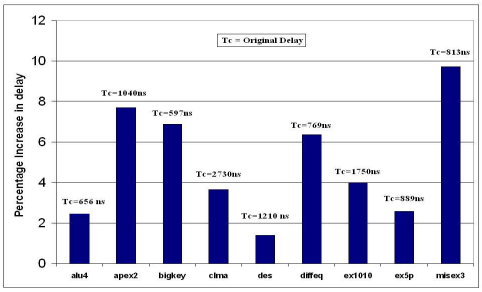

Figure 6. Performance Degradation due to Level Restorers and Buffers

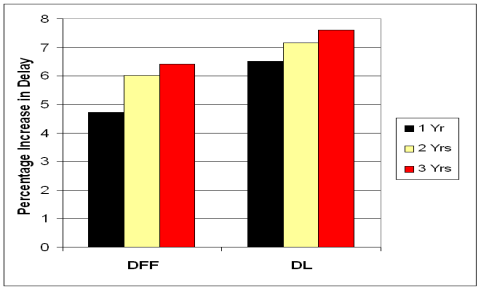

Figure 7. Change in delays of D flip flops and D latches

5 Mitigating NBTI effects

The impact of NBTI in a device can easily be inverted by flipping the gate inputs. In case of the configuration bits it requires us to flip the value stored in the configuration SRAM cells to restore the SNM. To recover from the increased delays of the level restorers and the buffers we need to invert the inputs driving the buffers. We present a methodology to achieve both, based on some existing as well as novel schemes. The existing schemes are derived from the power aware schemes which work on Input Vector Control (IVC) based strategies. Note that not all the configuration bits can be inverted all together to relax the FPGAs, since such a reversal may lead to damaging of devices. One such example of shorting the circuit by flipping the routing multiplexer bits is shown in figure 8. It is therefore evident that the configuration bits governing different circuitries of the FPGAs require different schemes. In this work we demonstrate how an existing flipping policy of LUTs may increase the age of the device and also present a methodology to flip the configuration of the routers.

5.1 Flipping configuration bits

The flipping of configuration bits may be performed by loading a new bitstream which has to be provided and stored in any external memory in the FPGAs. This bitstream whic

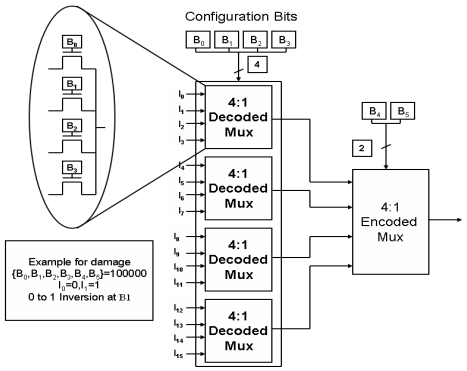

Figure 8. Routing Mux Architecture

be termed as a *Relaxing Bitstream* (RBIT), may be loaded over a period of time onto the device to relax the various devices while continuing to perform the required application implementation. Such RBIT(s) may be generated in a orderly manner. The configuration bits mainly store the LUT logic and the routing information. A technique similar to the SER aware technique presented in [17] may be employed to flip the bits used for configuring the LUTs. Figure 10 demonstrates the flipping operation which does not impact the LUT logic at all. All the LUT bits are flipped and shuffled appropriately to maintain the functionality of the application. However, performing both the shuffling and flipping together prevents inversion of all the configuration bits, since some of the bits retain their original values.The flipping algorithm is implemented by directly operating on the configuration bits of the FPGA using the opensource Java APIs provided by JBits(ver 3.0) [18] FPGAs.

The flipping of the configuration bits storing the routing information requires us to delve into the different types of routers in FPGAs. The routing multiplexers in FPGAs may be classified into four prime types as shown in table 3. Such a classification is important with respect to the strategies used for flipping the configuration SRAM cells of the multiplexers. Assuming a multi level multiplexer design as shown earlier in figure 8 we present different strategies to solve the bit inversion problem. Note that if any two inputs of opposite polarities are driving the multiplexer inputs, inverting the bits may turn on a 1-0 path and lead to shorting of the device as shown in figure 8. We therefore tackle such a shorting problem carefully for different multiplexers.

Table 3. Characterizing FPGA routing multiplexers

Router Type	Output State	Inputs State
Dead	Unused	All Undriven
Inactive	Unused	Some Driven
Active	Used	Some Driven
Fully-Used	Used	All Driven

(a) Dead Muxes: Such multiplexers comprise of nearly 60% of the total FPGA multiplexers even in the most used case. Since,all the inputs are undriven and the output is also unused, all the configuration bits may be conveniently inverted. The inputs and the outputs of the multiplexer may also be controlled appropriately to prevent the shorting, using the input vector control based strategies presented in [19].

(b) Inactive Muxes: These multiplexers have some of the inputs driven, but the output is unused. Consequently, they face the problem of shorting when the configuration bits are inverted. As demonstrated in the algorithm shown in figure 9, the bits of such routers may be flipped one at a time in a round robin manner.It is done for a time frame controlled using the variable *i* in the algorithm determined by the user. Note that this strategy requires either a processor support which is common in modern FPGAs or may be achieved by storing multiple frames of such configurations that may be loaded dynamically onto the FPGA.

(c) Active and Used multiplexers: Such multiplexers may not be inverted at all since their outputs impact the functionality. These routers however as demonstrated in the algorithm may be selectively rested by selecting alternate paths. Such a alternate path may be obtained at a bitstream level by using bitstream modulating tool JRoute [20]. Similar strategies for aging have been demonstrated for Electromigration aware design in [8].

```
i=0
x=0
Max_X_Coord = Maximum X coordinate of the device
MAX_ROUTE_INPUTS = Maximum inputs to any router
Invert_Route_Conf(Bitstream)
{
 Obtain the input and output information of the routers.
 for each( R in Routers )
   INPUTS = total inputs to the router R
   if(R's output is undriven)
    if(All inputs are undriven))
     Flip all the inputs/outputs/conf-SRAM-switches
      to same value
    if(Some or all inputs are driven))
      Drive (i mod INPUTS)^th config bit to 1
   else if(R's output is driven)
    if(R's location's X == x)
      Reroute the connection using JRoute
   if(i < MAX_ROUTE_INPUTS) i=i+1 else i=0
   if(x < Max_X_Coord_FPGA) x=x+1 else x=0
}
```

Figure 9. Algorithm for flipping the configuration bits of the routers in an orderly manner

5.2 Relaxing the Level Restorers and Buffers

The inputs to level restorers and buffers come from the routing muxes as shown in the figure 4. The migration of the routing to alternate routers has a direct impact on the resting of the level restorers. Such re-routing helps the overall reliability of the used routers significantly, not only due to NBTI based degradation but also other aging phenomena. The resting of LRs and buffers also helps gaining back the performance significantly.

5.3 Experimental Results

The experimental results obtained from the proposed algorithms are explained in this section. From figure 3, we observed that the SNM degraded by 2% at the end of 2 years for a 45nm medium oxide SRAM cell.So, we chose 2 years as the total

time frame for observation. Bit flipping was performed after 1 year on 10 Xilinx reference designs implemented on a Virtex-II device and we present the average SNM regained and FIT improvement of the devices. At an average, it was observed that 75.3% of the LUT Bits were flipped from its original configuration at the end of 1 year. The SNM at the start time of operation was 0.1005 V and the SNM of all benchmarks without cell flipping at the end of 2 years was 0.09828 V. The regained SNM results for the benchmarks (with bits flipped at the end of first year) at the end of second year are shown in table 4. Also, the FIT rate of the inverted cell also improved from 1038.5 FIT/MBit (for 2 years)to 1012.3 FIT/MBit (Bit flipped cell with maximum stress period of 1 year due to flipping) with higher critical charge. An estimated 2.5% decrease in FIT for cells inverted in X4VFX40 device was obtained for cell flipped designs with higher critical charge.

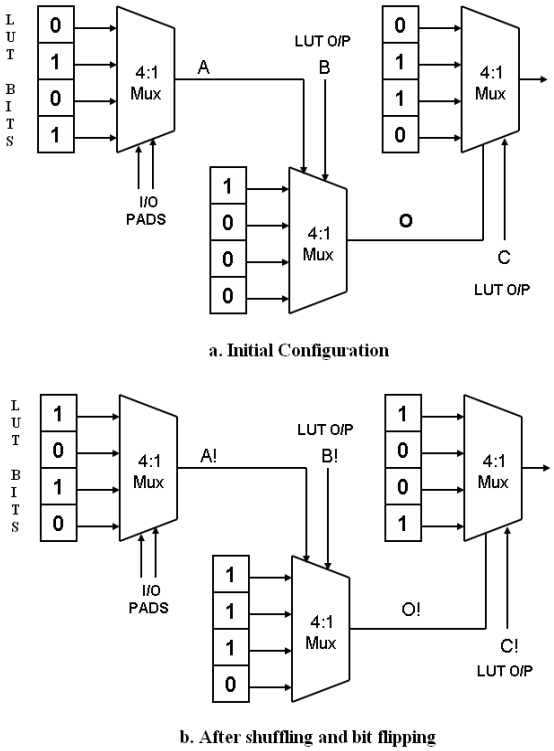

Figure 10. Bit Inversion to mitigate NBTI

6 Conclusion

In this paper we have provided a comprehensive analysis of the impact of NBTI on different components of FPGAs. The prime impact is observed in the form of stability of the FPGAs due to the constant stressing of the SRAM cells storing the configuration bits. An average performance degradation of 6.63% was observed when degraded level restorers and buffers were used. We proposed a novel, Relaxing Bitstream Technique to invert the gate inputs of the stressed devices appropriately for gaining back the lost stability and performance. Our experimental results for this method show a 53.26% improvement in the lost SNM and the FIT rate of device decreases by 2.48% for a X4VFX40 device.

Table 4. SNM Improvement for Benchmark Designs at the end of 2 years

Benchmark	Average SNM after Bit Flip(V)	% of SNM regained
xapp248	0.09913	38.71
xapp288	0.09975	66.46
xapp289	0.09957	58.34
xapp298	0.09936	48.88
xapp299	0.09953	56.39
xapp610	0.09917	40.47
xapp615	0.09958	58.58
xapp621	0.09959	59.34
xapp625	0.09927	44.94
xapp645	0.09962	60.43
Average		53.26

References

[1] International Technology Roadmap for Semiconductors,2005

[2] N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai,T. Horiuchi, "The Impact of Bias Temperature Instability on Digital Circuit Reliability for Direct-Tunneling Ultra-thin Gate Oxide on MOSFET Scaling" In *VLSI Symp. on Tech*, pp 73-74,1999.

[3] V. Reddy, A. T. Krishnan, A. Marshall, J. Rodriguez, S. Natarajan, T. Rost,S. Krishnan, S "Impact of Negative Bias Temperature Instability on Digital Circuit Reliability" In *Proceedings of International Reliability Physics Symposium(IRPS)*, 2002.

[4] J. Srinivasan, S. V. Adve, P. Bose and J. A. Rivers, "The Impact of Technology Scaling on Lifetime Reliability" In *Proceedings of International Conference on Dependable Systems and Networks(DSN)*, 2004.

[5] M. A. Alam and S. Mahapatra, "A Comprehensive Model of PMOS NBTI Degradation" In *Microelectronics Reliability*, vol 45,pp 71-81,2005.

[6] S. V. Kumar, C. H. Kim and S. S. Sapatnekar, "Impact of NBTI on SRAM Read Stability and Design for Reliability" In *Proceedings of International Conference on Quality Electronics Design(ISQED)*, 2006.

[7] B. C. Paul, K. Kang, H. Kufluoglu, M. A. Alam and K. Roy, "Impact of NBTI on Temporal Performance Degradation of Digital Circuits" *Electron Device Letters*,vol. 26,pp. 560-562,2003.

[8] S. Srinivasan, P. Mangalagiri, K. Sarpatwari, Y. Xie and N. Vijaykrishnan "FLAW:FPGA Lifetime Awareness" In *Proceedings of Design Automation Conference (DAC)*, 2006.

[9] P. K. Samudrala, J. Ramos and S. Katkoori "Selective Triple Modular Redundancy for SEU Mitigation in FPGAs" In *Proceedings of Military and Aerospace Applications of Programmable Logic and Devices (MAPLD)*, 2003.

[10] D. K. Schroder and J. F. Babcock, "Negative Bias Temperature Instability:Road to Cross in Deep Sub-Micron Silicon Semiconductor Manufacturing" *Journal of Applied Physics*,94:1-18,2003.

[11] J. G. Massey "NBTI: What we know and What we need to know - a tutorial addresssing the current understanding and challenges for the future" In *International Integrated Reliability Workshop Fianl Report*,Pages 199-211,2004.

[12] R. Vattikonda, W. Wang and Y. Cao "Modeling and Minimization of PMOS NBTI Effect for Robust naometer Design" In *Proceedings of Design Automation Conference (DAC)*, 2006.

[13] W. Zhao and Y. Cao "New Generation of Predictive Technology Model for sub-45nm Design Exploration" In *Proceedings of International Conference on Quality Electronics Design(ISQED)*, 2006.

[14] " http://www.xilinx.co.jp/bvdocs/whitepapers/wp246.pdf" Power Consumption in 65nm FPGAs,White Paper:Virtex-5 Family of FPGAs,May 11,2006.

[15] P. Hazucha and C. Svensson, "Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate" In *IEEE Trans. on Nuclear Science*, vol 47,No. 6,pp 2586-2594,2000.

[16] V. Betz and J. Rose "VPR: A new packing, placement and routing tool for FPGA research" In *Proceedings of the 7th International Workshop on Field-Programmable Logic and Applications*, 1997.

[17] S. Srinivasan, A. Gayasen, N. Vijaykrishnan, M. Kandemir, Y. Xie and M. J. Irwin "Improving Soft-Error Tolerance of FPGA Configuration Bits" In *Proceedings of International Conference on Computer-Aided Design (ICCAD)*, 2004.

[18] " www.xilinx.com" Xilinx product datasheet and application tools for Virtex-II.

[19] S. Srinivasan, A. Gayasen, N. VijayKrishnan and T. Tuan "Leakage control in FPGA routing fabric" In *Proceedings of Asia-South Pacific Design Automation Conference (ASPDAC)* , 2005.

[20] E. Keller "JRoute: A Run-Time Routing API for FPGA Hardware" In *Proceedings of Seventh Reconfigurable Architectures Workshop (RAW)* , 2000.