# Mixer Topology Selection for a Multi-Standard High Image-Reject Front-End

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*Abstract*— **In this paper, a mixer topology selection for a multi-standard high image-reject front-end is presented. The receiver is intended to work for Digital Enhanced Cordless Telephone (DECT) systems (at 1.9 GHz and 2.4 GHz) and for Bluetooth (at 2.4 GHz). It will be implemented in** $0.18\ \mu m$ **CMOS technology. A double-quadrature low-IF architecture is employed because it can provide a high image rejection and flexibility for different standards. Building block specifications are optimized in order to achieve high image rejection and high sensitivity. Since the downconverter is the core of the front-end, it is necessary to select a high performance mixer topology that can provide low noise figure, high voltage gain, low power consumption and moderate linearity. Instead of simply using standard Gilbert cell and focus on its optimization, as it is quite often done in the literature, three mixer topologies, are examined. The evaluation is done analytically and by simulations with SpectreRF. A novel folded switching mixer topology achieves the best performance. With this topology the following simulation results are achieved: noise figure (NF)** 14 dB**, voltage gain (**$G$**)** 17 dB**, linearity (**$IIP_3$**)** $-1$ dBm **with a power consumption of** 4.5 mW **at the operating frequency of** 2.5 GHz**. Good matching between expected and simulated results is observed. A low voltage operation, which implies robustness for technology scaling, is also considered. At the end the final results are reported and the most promising topology is selected.**

*Keywords*— **Multi-Standard Receiver, CMOS Mixer, Low voltage operation**

## I. INTRODUCTION

The wireless market is changing very rapidly. For set-makers it is very useful to have cost effective front-end solutions that can be applied in communication systems for different standards. From an application point of view, a non-concurrent front-end that can be used for the DECT system at 1.9 GHz and for systems in the ISM band (like Bluetooth or DECT at 2.4 GHz) is very attractive. In [1], it was shown that such a multi-standard receiver is feasible.

The front-end employs a double-quadrature low-IF architecture (see Fig. 1). Building block specifications (e.g. $NF$, gain ($G$), input $IP_3$ ($IIP_3$)) are calculated such, that the front-end satisfies the system specifications for both standards. The target mixer specifications are: $NF$ lower than 14 dB, $G$ higher than 15 dB, $IIP_3$ higher than $-1$ dBm at the maximum operating frequency of 2.5 GHz. A high mixer voltage gain is important, since it reduces the noise coming from the stages after the mixer and a low mixer $NF$ is necessary in order to relax LNA specifications and to mitigate the corruption of the overall front-end $NF$ by the RF polyphase filter.

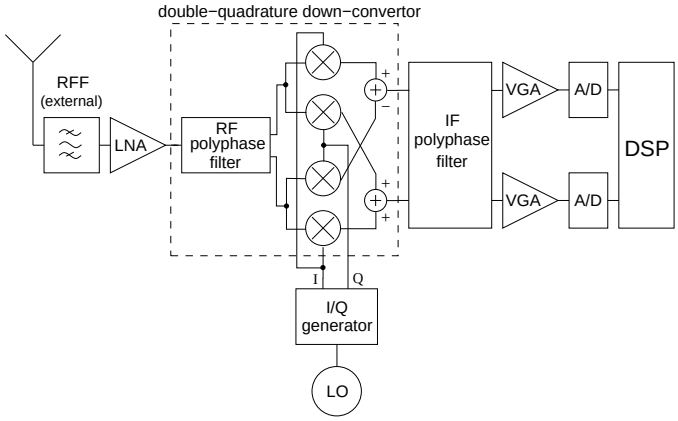


Fig. 1. The double-quadrature low-IF architecture

There are three fundamental ways to realize mixing operation in CMOS circuits. The first possibility is to realize a switching mixer. A well known example is the double-balanced switching mixer (Gilbert cell), which is described in section 2 with special attention to its operation at low supply voltages. In order to avoid some drawbacks of the Gilbert cell, a new folded switching mixer is discussed in section 3. The second possibility is to exploit the square law characteristic of a MOS transistor [2]. The disadvantage of this mixer is a low gain (around 2 dB). The third possibility is using a MOS transistor in the linear

region. In this way, a passive linear mixer is obtained [3]. This mixer has a very high linearity ($IIP3$ around 40 dBm) but the $NF$ is very high (around 30 dB). Such a $NF$ will lower the front-end sensitivity too much. In section 4, a modified mixer that uses MOS transistors in the linear region, with an improved $NF$, is represented. In section 5, the presented mixer topologies are compared and the most promising mixer topology is selected.

## II. DOUBLE BALANCED MIXER

The double balanced switching mixer (Gilbert cell) is the most commonly used switching mixer (see Fig. 2). In this article special attention is paid on the optimization

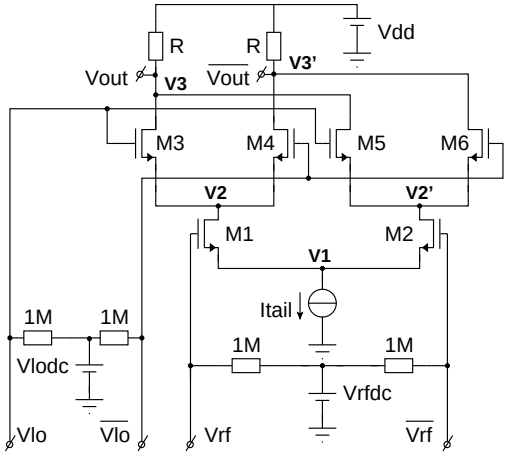


Fig. 2. Double balanced switching mixer

in CMOS 0.18 $\mu$m technology and on low voltage operation. The following design procedure has been followed. First it is necessary to adjust the biasing ($V_{rfdc}$, $V_{lodc}$), the $W/L$ ratio of the transistors and the resistor value ($R$) such that all the transistors work in the saturation. This is especially important when a low supply voltage is applied. Low voltage design requires a good insight into the circuit operation.

For a given $I_{tail}$ current, voltage $V_1$ is determined by $V_{rfdc}$ and by the $W/L$ ratio of the transistors $M_1$ and $M_2$. In order to keep $V_1$ sufficiently high, the $W/L$ ratio of the transistors $M_1$ and $M_2$ must be large. This increases parasitics, which can corrupt the high frequency mixer operation. From a positive perspective, the transconductance ($g_m$) of the transistors $M_1$ and $M_2$ will be increased, which increases gain and reduces noise. Voltage $V_1$ can also be increased by increasing $V_{rfdc}$. By decreasing the $W/L$ ratio of the transistors $M_1$ and $M_2$, the overdrive voltage ($V_{gs}-V_t$) of $M_1$ and $M_2$ will be increased. This helps to obtained higher $IIP_3$ [5]. $V_2$ depends on the $W/L$ ratio of the switching transistors ($M_3$,$M_4$,$M_5$ and $M_6$) and $V_{lodc}$. For a given $I_{tail}$, it is appreciable to keep $V_2$ as high as possible. This can be done by increasing the $W/L$ ratio of the switching transistors or by increasing $V_{lodc}$. The first action can have a negative influence on the high frequency mixer operation. If the $W/L$ ratio of the switching transistors is not high then it is necessary to apply a high $V_{lo}$ voltage in order to perform the complete commutation. $V_3$ is determined by $V_{dd}$ and $R$ for a constant $I_{tail}$. If $V_1$, $V_2$ and $V_3$ are low and if all the other parameters are constant, they can be increased by decreasing $I_{tail}$. This will reduce $g_m$ and increase $NF$.

The next step is to optimize the mixer for a low $NF$, specified voltage gain and linearity. The $NF$ of the Gilbert cell, under the assumption that local oscillator (LO) voltage is an ideal square wave and taking into account a noise folding from the frequency $f_{RF}+f_{lo}$, is approximated by:

$$NF = 10\log(2+\frac{4\gamma_n}{g_m R_s}+\frac{\pi^2}{2g_m^2 R R_s}) \qquad (1)$$

$R_s$ is the impedance of the signal source, which drives the mixer RF port, The coefficient $\gamma_n$ is equal to $2/3$ for long channel transistors and need to be replaced with a larger value for submicron MOSFETs [4]. The voltage gain can be approximated by:

$$G = 20\log(\frac{2}{\pi}g_m R) \qquad (2)$$

A more detailed noise analysis can be found in [6]. In this article, the most important design measures for noise reduction and voltage gain improvement will be mentioned. Higher $I_{tail}$ improves $g_m$, reduces $NF$ and increases gain and power consumption. $g_m$ can be improved by increasing the $W/L$ ratio of $M_1$ and $M_2$ transistors, but this will introduce more parasitics and increase the chip area, or by reducing the overdrive voltage, which will reduce $IIP_3$. A large LO drive reduces the $NF$ and increases gain because complete commutation is performed. When complete commutation is achieved, increase of the LO drive does not help anymore. Finally it is important to check the achieved mixer linearity by simulating the $IIP_3$. Mixer $IIP_3$ can be approximated by [5]:

$$IIP_3 = 4\sqrt{\frac{2}{3}}(V_{gs}-V_t) \qquad (3)$$

$V_{gs}$ is the gate-source voltage and $V_t$ is the threshold voltage of transistors $M_1$ and $M_2$. From (3) it is clear that a better linearity (higher $IIP_3$) can be obtained by increasing the overdrive voltage ($V_{gs}-V_t$).

Using the circuit simulator SpectreRF and applying the presented approach for Gilbert cell optimization in CMOS 0.18 $\mu$m technology, the simulation results shown in Table I are obtained.

TABLE I

SIMULATION RESULTS FOR GILBERT CELL AT 2.5 GHZ

| $V_{dd}$ (V) | $NF$ (dB) | $G$ (dB) | $IIP_3$ (dBm) | $P$ (mW) |
|---|---|---|---|---|
| 1.8 | 10.13 | 8.9 | 2.2 | 5.22 |
| 1.5 | 10.67 | 7.2 | 2.68 | 4.35 |
| 1 | 13.84 | 3.5 | $-1$ | 1.4 |

The mixer operating frequency is set to 2.5 GHz and LO frequency is 2.498 GHz because, if the mixer satisfies the specifications at 2.5 GHz then it will certainly satisfies the same specifications at 1.9 GHz. At the lower supply voltages ($V_{dd} = 1.5$ V and $V_{dd} = 1$ V), $I_{tail}$ must be reduced in order to provide proper operation of the mixer. This causes the reduction of $g_m$ of the transistors $M_1$ and $M_2$ and as a consequence the mixer $NF$ and voltage gain $G$ get worse. The reduction of the overdrive voltage $(V_{gs} - V_t)$of $M_1$ and $M_2$ is the reason for slightly lower $IIP_3$ of the mixer. The disadvantage of this mixer topology is the low voltage gain. A higher voltage gain can be obtained by increasing $R$ or by increasing $g_m$. The resulting higher voltage swing at the output can also be problematic because it corrupts the normal operation of the switching transistors.

## III. FOLDED SWITCHING MIXER

In order to overcome the relatively low voltage gain of the previous mixer topology, a folded switching mixer with PMOS transistors as loads is investigated. This mixer topology is shown in Fig. 3.

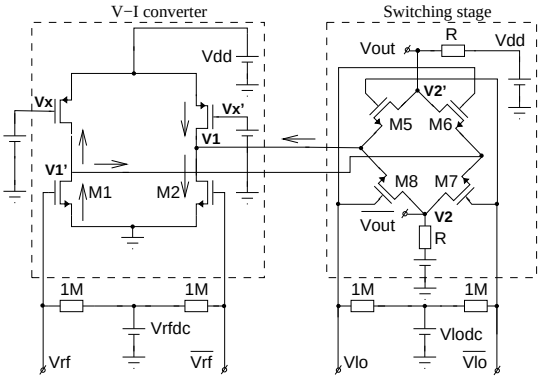


Fig. 3. Folded switching mixer

The voltage gain of the mixer in Fig. 3 can be approximated by:

$$G = 20\log(\frac{2}{\pi}\frac{g_{mn}R}{1+\frac{1}{R_o(g_{ms}+g_{msb})}}) \qquad (4)$$

where $g_{mn}$ is the transconductance of the transistors $M_1$ and $M_2$, $g_{ms}$ is the transconductance of the switching transistors, $g_{mbs}$ is the transconductance from the bulk of the switching transistors and $R_o$ is the output impedance of the transistors $M_1$ and $M_2$. The bulk and the source of the switching transistors are not at the same potential (the bulk is grounded) and the bulk behaves as a second gate. The AC current flow is depicted in Fig. 3. A part of the AC current flows through the transistors $M_3$ and $M_4$ and this is the reason why the gain is lower than $\frac{2}{\pi}g_mR$, as it is in the case of the Gilbert cell (see (2)). In order to have a higher voltage gain it is necessary to have $R_o$ as large as possible. This also follows from (4). In this way the AC current that flows through the transistors $M_3$ and $M_4$ is reduced.

The $NF$ of this mixer can be approximated by:

$$\begin{aligned} NF &= 10\log(2+\frac{4\gamma_n}{g_{mn}R_s}+\frac{\pi^2(1+\frac{1}{R_o(g_{ms}+g_{mbs})})^2}{2g_{mn}^2RR_s} \\ &+ \frac{4\gamma_p g_{mp}}{g_{mn}^2R_s}+\frac{2\gamma_n g_{ms}}{R_s g_{mn}^2 R_o^2(g_{ms}+g_{mbs})^2}) \end{aligned} \qquad (5)$$

The $NF$ is increased in comparison with the $NF$ of the Gilbert cell. The noise from transistors $M_3$ and $M_4$ contributes to the $NF$ (the fourth term in (5)) and the noise from the switching transistors contribute more than in the case of the Gilbert cell (the fifth term in (5)). Even in the case of perfect switching when a square wave LO signal is applied, the noise current from the conducting switching transistor can flow through the output impedance ($R_o$) of the transistors $M_3$ and $M_4$ and contributes in this way to the total $NF$.

Using the circuit simulator SpectreRF, the simulation results, given in Table II, are obtained. The main advantage of this mixer topology is a relatively high voltage gain (higher compared to the Gilbert cell ) at very low supply voltages and moderate linearity. So this mixer topology is very robust to the technology scaling. The disadvantage is increased $NF$. At the lower supply voltages ($V_{dd} = 1.5$ V and $V_{dd} = 1$ V), the overdrive voltage $(V_{gs} - V_t)$ of $M_1$ and $M_2$ gets lower and this is the reason for lower performance.

TABLE II

SIMULATION RESULTS FOR FOLDED SWITCHING MIXER AT 2.5 GHZ

| $V_{dd}$ (V) | $NF$ (dB) | $G$ (dB) | $IIP_3$ (dBm) | $P$ (mW) |
|---|---|---|---|---|
| 1.8 | 11 | 20 | $-4$ | 12 |
| 1.5 | 14 | 17 | $-1$ | 4.5 |
| 1 | 15 | 13 | $-2$ | 3.3 |

## IV. MIXER WITH MOS TRANSISTORS IN THE LINEAR REGION

Very linear down-conversion mixer with MOS transistors in the linear region is presented in [3]. The $IIP_3$ of this

mixer is very high, but the disadvantage is a very high NF (around 30 dB). Such a high NF corrupts too much the receiver sensitivity and can not be used for a non-concurrent multi-standard receiver for the DECT system and Bluetooth. A possibility is to modify this mixer topology in order to reduce the NF. The NF can be reduced by adding a gain stage in front of a stage with MOS transistors in the linear region (linear stage) that performs frequency conversion. The gain stage can be a simple differential pair. The new, modified mixer topology is represented in Fig. 4.

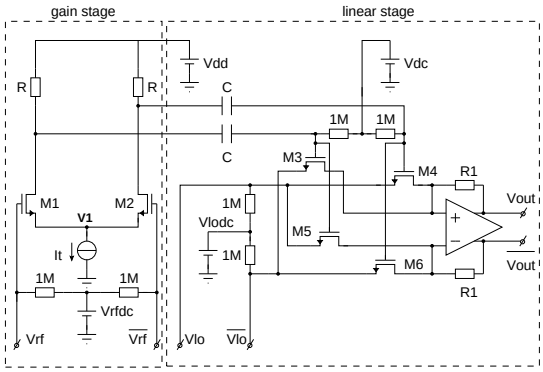


Fig. 4. Mixer with MOS transistors in the linear region

The total mixer noise figure ($NF$) can be calculated as:

$$NF = NF_g + \frac{NF_l}{G_g} \tag{6}$$

where $NF_l$ is the $NF$ of the linear stage, $NF_{dif}$ and $G_g$ are the $NF$ and the voltage gain of the gain stage. $NF_g$ can be calculated by:

$$NF_g = 10\log(1 + \frac{2\gamma_n}{g_m R_s} + \frac{2}{g_m^2 R R_s}) \tag{7}$$

where $g_m$ is the transconductance of the transistors $M_1$ and $M_2$. $G_g$ can be calculated by:

$$G_g = 20\log(g_m R) \tag{8}$$

The noise figure $NF_l$ of the linear stage is extensively discussed in [3] and this part of the mixer is designed such that a minimal $NF_l$ is obtained. In addition to a low $NF$, linearity is of importance. The mixer $IIP_3$ can be calculated by:

$$\frac{1}{IIP_3^2} = \frac{1}{IIP_{3g}^2} + \frac{G_g^2}{IIP_{3l}} \tag{9}$$

where $IIP_{3g}$ and $IIP_{3l}$ describe the linearity of the gain stage and linear stage respectively. In order to achieve a low $NF$ and a good linearity, it is necessary to have insight into circuit operation. First the linear stage is simulated. The mixer is designed in a 0.18 $\mu$m CMOS technology and simulated in SpectreRF circuit simulator. The following results are obtained: $NF_l = 36dB$, $IIP_{3l} = 21dBm$ and $G_l = -3dB$. $G_l$ is the gain of the linear stage. From (6) it is clear that for a low $NF$ it is necessary to provide high voltage gain of the gain stage ($G_g$) and a low $NF_g$. A high $G_g$ can make problems in achieving good linearity. First it increases the contribution of nonlinearities from the linear stage (see 9) and second a high voltage swing at the output of the gain stage, that is the result of a high gain, can corrupt the normal operation of the transistors M1 and M2 ( they work partly in linear region). As a consequence $IIP_{3g}$ is reduced, that reduces the $IIP_3$. The design goal is to find an optimal value for $G_g$ in order to obtain a low $NF$ and satisfactory linearity. The $G_g$ can be increased in the following ways: increasing the ratio $W/L$ of the transistors $M_1$ and $M_2$, increasing $I_t$ and increasing $R$. The first possibility is not convenient because the overdrive voltage ($V_{gs} - V_t$) of the transistors $M_1$ and $M_2$ is reduced, that reduces $IIP_{3g}$ [5] and also due to the increased parasitics the mixer high frequency operation is corrupted. Increasing $I_t$ increases $g_m$, that reduces $NF_g$ and improves linearity because the overdrive voltage $V_{gs} - V_t$) of the transistors $M_1$ and $M_2$ is increased. The disadvantage is that the power consumption is increased and also the voltage drop over resistor $R$ is increased. Increasing $R$ increases $G_g$, but the voltage drop over this resistor is also increased. The second and third option for $G_g$ increasing are used with special attention on voltage drop over resistor $R$, that must be sufficiently low to keep the transistors $M_1$ and $M_2$ in saturation.

Using the circuit simulator SpectreRF and applying the presented insight, the simulation results, shown in Table III, are obtained. The simulated $IIP_3$ for the gain stage (using the data from the second row in Table III) is 1 dBm. From (9) it is clear that the nonlinearity of the gain stage is dominant and there only is a small contribution from the linear stage. This is the reason for increasing $IIP_3$ with in-

TABLE III
SIMULATION RESULTS FOR MIXER WITH MOS TRANSISTORS IN THE LINEAR REGION AT 2.5 GHz

| Row No. | $R$ ($\Omega$) | $I_t$ (mA) | $NF$ (dB) | $G$) (dB) | $IIP_3$ (dBm) | $P$ (mW) |
|---|---|---|---|---|---|---|
| 1 | 1k | 1.5 | 20 | 14 | $-1.8$ | 2.7 |
| 2 | 500 | 2 | 21 | 12 | $-1.5$ | 3.6 |
| 3 | 1k | 2 | 19 | 15 | $-1.2$ | 3.6 |
| 4 | 1k | 2.5 | 18 | 16.5 | $-3$ | 4.5 |
| 5 | 500 | 2.5 | 20 | 13.6 | $-1$ | 4.5 |

creasing $I_t$. Only in the fourth row in Table III the linearity is somewhat degraded because the voltage drop over resistor R was to high and the transistors $M_1$ and $M_2$ operate partly in the linear region. When $R$ is reduced to 500 $\Omega$, then the $IIP_3$ was improved (the fifth row in Table III). Increasing $I_t$ and keeping $R$ the same, $G_g$ is increased and $NF$ is reduced. When $I_t$ is increased and $R$ reduced, then $NF_g$ is reduced but $NF$ is increased because $G_g$ is reduced and the noise from the linear stage is dominant. This explains the results in the third row in Table III. The main disadvantage of this mixer topology is that it can not work at low voltages because of high voltage drop over resistor $R$ and the relatively high $NF$.

## V. MIXER TOPOLOGY SELECTION

Comparing the obtained simulations results given in the Table I, II and III, it can be seen that the folded switching mixer is the only topology that satisfies the target specifications mentioned in section 1. The Gilbert cell is convenient for the applications where a low mixer $NF$ is required. It can also operate at very low supply voltages (up to 1V). When low $NF$ is not the dominant issue, but high voltage gain, then the folded switching mixer should be selected. The performance of the mixer with MOS transistors in the linear region are lower in comparison with the other two topologies.

## VI. CONCLUSIONS

Three mixer topologies are presented and evaluated. Full insight into the operation of the presented mixers is given. As a result of this insight approximated expressions for voltage gain, $NF$ and $IIP_3$ for the topologies are given and the fundamental differences between the presented topologies are discussed.

It was shown that the novel folded switching mixer satisfies the target specifications resulting from the chosen double-quadrature low-IF architecture. With this mixer topology it is possible to achieve a high voltage gain, moderate $NF$ and moderate linearity with low power consumption. Mixer operation at very low supply voltages is considered. The complete design procedure for the Gilbert cell is given. Applying such a design approach, it was shown that Gilbert cell can operate at supply voltage of $1V$ achieving moderate $NF$. An alternative is the folded switching mixer that can achieve high gain at low supply voltages.


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