Characterization of Pulsed Laser Deposited Al_2O_3 Gate Dielectric

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Abstract— **The demands of future CMOS devices require a new gate dielectric material with higher dielectric constant than SiO_2. Aluminum oxide is one of the high-k materials and an interesting candidate.**

Thin Al_2O_3 layers have been deposited by pulsed laser deposition (PLD) from a mono-crystalline sapphire target. This deposition technique was chosen because of its flexibility and availability. Aluminum oxide is known for its decent interface properties with silicon and is expected to be part of the future gate dielectric.

The probability and effects of interface intermixing during PLD have been estimated by (thermodynamic) calculations. The results showed that the exchange of aluminum and silicon atoms at the interface is thermodynamically favourable. AFM and XPS analysis of PLD Al_2O_3 layers showed a difference in density and interface between samples deposited in Ar and O_2. The films deposited in an Ar ambient appear to have a higher density and sharper Al_2O_3/Si interface.

Test structures with PLD dielectric, thermal oxidation and jet vapor deposition (JVD) of SiO_2 will be used to make a comparison between the layers and their interface properties. Electrical characterization will have to confirm the expected interface mixing, reduction in minority carrier mobility and effects of PLD deposition.

Keywords— **high-k; gate dielectric; aluminum oxide (Al_2O_3); pulsed laser deposition (PLD)**

I. Introduction

The process of downscaling transistors was started since their first use in the early 1960s and continued at a dramatic rate until reaching fundamental limits. Solutions now have to be found to overcome these barriers and enable future progress in semiconductor technology. For decades thermally grown silicon dioxide has been used as the gate dielectric material in standard CMOS technology. Downscaling has reduced the thickness of this layer, resulting in unacceptably high leakage currents through the MOS stack. The solution to this problem for MOSFETs is replacing the SiO_2 gate dielectric by a new material with increased dielectric constant. A high-k material will replace the traditional SiO_2 gate dielectric and thermal oxidation will be replaced by a deposition technique. The new material allows a thick layer with lower leakage current, without a reduction of the gate capacitance:

$$C_{ox} = \frac{\epsilon_0 \cdot \kappa_{ox} \cdot A}{t_{ox}} \quad (1)$$

Aluminum oxide was reported to have the highest electron bandgap (E_G = 8.7 eV) and conduction band offset to silicon (ΔE_C = 2.8 eV) of all high-k materials [1]. Although Al_2O_3 has a relatively low dielectric constant (κ = 7. . . 9) compared to other high-k materials, these advantages will probably make Al_2O_3 part of a future MOS gate stack.

With the change from thermal oxidation to deposition, heteroepitaxial growth of a dielectric material on silicon becomes of interest. An epitaxial interface between gate dielectric and silicon substrate will improve the interface trap density and channel mobility. Epitaxial growth of γ-Al_2O_3(100) films on Si(100) by ionized beam deposition has been reported in literature [2].

Until now, the most promising technique to deposit high-k materials is atomic layer chemical vapor deposition (ALCVD). Although ALCVD has many advantages above the other known deposition techniques, initial growth behaviour, uniformity and interfacial oxide are not yet fully understood. During the construction of a custum designed ALCVD reactor, experiments on high-k dielectrics by pulsed laser deposition were started. Pulsed laser deposition was chosen for its flexibility in materials and reported ability to deposit epitaxial layers.

II. Calculations

The stability of the Al_2O_3/Si interface can be estimated by a thermodynamic approach using bond-enthalpies. The ideal interface between substrate and Al_2O_3 consists of

oxygen atoms fully bonding the silicon lattice to the dielectric lattice, without an intermixed or interfacial oxide (SiO_2) layer.

Intermixing of the interface starts when Si and Al atoms exchange positions. The Al atom is negatively charged (acceptor) in the silicon lattice and has accepted an electron from the Si atom in the dielectric, which becomes a positive oxide charge. The negative Al ions in the channel reduce the mobility of electrons and holes. Once the Al atom diffuses one atomic layer deeper into the substrate, it is considered a normal acceptor at 67 meV above the valence band.

Thermodynamics defines two criterea for spontaneous change at constant temperature:

$$\Delta A = \Delta U - T \cdot \Delta S \leq 0 \quad (2)$$

$$\Delta G = \Delta H - T \cdot \Delta S \leq 0 \quad (3)$$

The change in entropy ΔS for this process is positive since the degree of disorder increases when the Al and Si atoms change position. Due to a constant internal energy (ΔU = 0) equation 2 is valid. The change in enthalpy ΔH is estimated using mean bond enthalpies. Table I lists the bond enthalpies of interest.

bond type	bond energy (kJ/mol)	bond energy (eV)
Al : Al	133 ± 6	1.4
Al : O	511 ± 3	5.3
Al : Si	229.3 ± 30.1	2.4
Si : O	799.6 ± 13.4	8.3
Si : Si	325 ± 7	3.4

TABLE I
BOND ENTHALPIES AT 298 K.

The change of enthalpy for the reaction in which the two atoms exchange position at the interface can now be calculated:

$$\begin{aligned} \Delta H &= 3 \times (Al:O) + 3 \times (Si:Si) + 1 \times (Si:O) - \\ &\quad (3 \times (Si:O) + 3 \times (Al:Si) + 1 \times (Al:O)) \\ &= 15.9 + 10.2 + 8.3 - (24.9 + 7.2 + 5.3) \\ &= 34.4 - 37.4 = -3.0\ eV \end{aligned} \quad (4)$$

The net ionization energy for Si^+ and Al^- is assumed to be negligible ($\ll 1$ eV).

The results show that the exchange reaction is thermodynamically favourable. However, the actual reaction depends on the kinetics, which is determined by temperature and the energy of the arriving particles. In PLD the typical energy of arriving particles is about 40 eV [3], so sufficient energy is available for the reaction and diffusion of the aluminum atoms.

The contribution by diffusion is defined by $\sqrt{Dt}$ and the maximum solid solubility. For aluminum it is estimated (by extrapolation from high temperature values [4]) to be $\sqrt{D} = 10^{-5}$ µm/hr$^{1/2}$ at 800 K. This means $\sqrt{Dt} = 10^{-5}$ µm for 1 hr deposition at 800 K which is much less than one mono-layer. So the temperature contribution to the disturbance of the interface is negligible.

The thermal energy is sufficient to disturb several Si-Si bonds and enhance the diffusion in the surface over a range of a few mono-layers. It is questionable whether the maximum solid solubility of Al in Si is of any importance because the process takes place far from equilibrium. If equilibrium is assumed then the maximum solid solubility is estimated to be $5{\cdot}10^{18}$ cm^{-3} at 800 K [4]. In a layer of 2 mono-layers thick there will be about $2.7{\cdot}10^{11}$ cm^{-2} Al atoms incorporated in the Si surface. The resulting shift in flatband voltage is calculated (with substitution of eq. 1):

$$\Delta V_{\text{fb}} \sim \frac{q \cdot \Delta N_{\text{ss}}}{C_{\text{ox}}} = \frac{q \cdot \Delta N_{\text{ss}} \cdot t_{\text{ox}}}{\epsilon_0 \cdot \kappa_{\text{ox}} \cdot A} \quad (5)$$

Assuming an equivalent oxide thickness of 2 nm, the flatband voltage will only shift by +25 mV. However, the reduction of minority carrier mobility is estimated (using equation 6 [5]) to be $300 \ldots 500$ cm^{2}V^{-1}s^{-1}. This amount of mobility degradation is not acceptable.

$$\Delta E_{\text{eff}} = \frac{\epsilon_{\text{ox}}}{2 \cdot \epsilon_{\text{s}}} \cdot \frac{\Delta V_{\text{fb}}}{t_{\text{ox}}} \quad (6)$$

It is expected that due to the disturbance of every new layer, Si may diffuse (enhanced by the high thermal energy of deposition) up to the surface of the dielectric and create a lot of traps in the film.

Taking these considerations into account it is expected that a deposition by low energy particles, like CVD or thermal PVD would yield less disturbed interfaces. Due to the higher bond energy of a Si:O bond, a 2 mono-layer thick SiO_2 interface layer could also prevent intermixing of Al_2O_3 and the substrate. However, the absence of an interfacial SiO_2 or intermixed layer after the epitaxial growth above 850 °C, was explained by the difference in formation enthalpies between Al_2O_3 (-1676 kJ/mol) and SiO_2 (-908 kJ/mol) [2]. The formation of Al_2O_3 would be more effective and dominant to the formation of SiO_2.

III. EXPERIMENTAL

A semiconductor process was developed to make test structures (capacitors, MOSFETs, etc.) on 100 mm p-type

Si(100) substrates. The wafers were chemically cleaned with 100% fuming HNO_3 and 69% boiling HNO_3 for 10 minutes each, followed by 1% HF dipping to remove native oxide. After patterning the active areas by LOCOS oxidation, source/drain areas were implanted through a 3.5 µm resist mask. A 100 nm TEOS layer was deposited to reduce the parasitic capacitance of interconnect and probe pads. After opening the gate area by etching in 1:6 HF/NH_4F, the wafers were cut to 15 × 15 mm^2 pieces to fit in the PLD reactor. Before pulsed laser deposition of the Al_2O_3 gate dielectric, native oxide was removed by dipping in a 1% HF solution.

Single crystalline $(11\bar{2}0)$ α-Al_2O_3 (sapphire) was used as target material to minimize the impurity concentration in the deposited film. A KrF excimer laser (Lambda Physic Compex, λ = 248 nm) was pulsed at a low rate with a 20 ns pulse length. The homogeneous part of the laser beam was selected by a mask and projected on the target at 45° incidence by means of a focusing lens. The resulting energy density and size of the laser spot on the target have been optimalized by SEM analysis of the target surface, after ablation at different energy densities. To minimize oxidation of and intermixing with the silicon, the substrate temperature was kept at room temperature. The deposition ambient was 0.1 mbar Ar or O_2, with purities > 99.99 % and > 99.995 % respectively, while the background pressure was kept below 10^{-7} mbar.

After deposition of the gate dielectric, a 200 nm aluminum layer was immediately deposited by sputtering, to complete the MOS stack and protect the gate dielectric. The test structures were finished by etching a gate cover pattern in the aluminum layer, etching of contact holes and making an aluminum interconnect pattern.

Besides test structures with pulsed laser deposited dielectric, thermal oxidation and jet vapor deposition (JVD) of SiO_2 will be used to make a comparison between the dielectric layers and their influence on interface properties. On a fourth sample the PLD Al_2O_3 will be etched off after deposition and replaced by JVD SiO_2. This last sample will be used to determine the effects of the PLD technique (plasma damage, interface intermixing, etc.) on the silicon/dielectric interface.

IV. Results and discussion

A. Atomic force microscopy

The surface morphology of the deposited Al_2O_3 films was studied by tapping mode AFM. Table II shows the measured roughness (average and rms) on the 1 × 1 μm^2 area and the thickness of the film as determined by ellipsometry.

laser pulses	ambient 0.1 mbar	thickness (nm)	R_{avg} (nm)	R_{rms} (nm)
100	Ar	4.0	0.106	0.133
500	Ar	18.8	0.359	0.453
1000	Ar	37.4	0.545	0.688
5000	Ar	161.2	1.187	1.477
100	O_2	8.5	0.436	0.629
500	O_2	49.5	1.380	1.753
1000	O_2	103.6	2.747	3.437
5000	O_2	550.8	6.773	8.439

TABLE II
Surface roughness and film thickness.

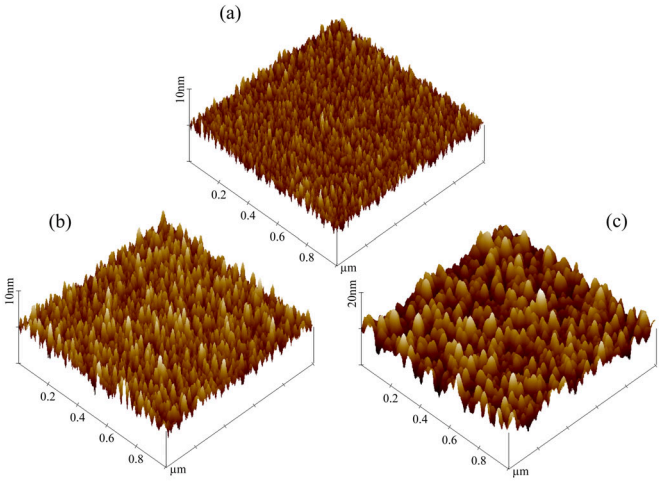

Fig. 1
AFM images of the Al_2O_3 film deposited in Ar ambient after (a) 500, (b) 1000 and (c) 5000 pulses.

The AFM images in figures 1 and 2 show the increase in film roughness with the number of laser pulses. The difference in film thickness between the layers deposited in Ar and O_2, shows the reactivity of the plasma with oxygen. Including the measured thicknesses, the film deposited in O_2 is expected to either contain a higher oxygen concentration or have a lower density. Although the size of particles arriving at the surface is unknown, island growth mode becomes visible after 1000 pulses.

B. X-ray photoelectron spectroscopy

A depth profile of the Al_2O_3 films was measuremed after deposition of 5000 pulses in an Ar or O_2 ambient. The graphs in figures 3 and 4 show the atomic concentrations of O, Si, and Al after every 4 minutes of 1 keV Ar^+ sputter etching. Although the etch rate was measured as

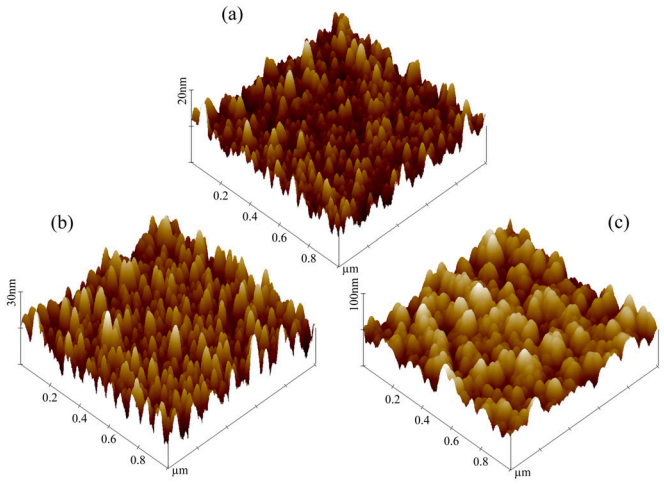

Fig. 2
AFM IMAGES OF THE AL_2O_3 FILM DEPOSITED IN O_2 AMBIENT AFTER (A) 500, (B) 1000 AND (C) 5000 PULSES.

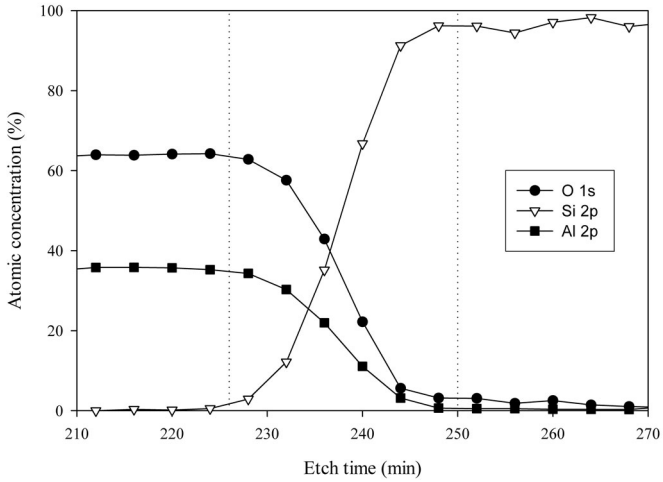

Fig. 4
DEPTH PROFILE OF AL_2O_3 DEPOSITED IN O_2.

2.5 nm/min on a SiO_2/Si reference, calculations on the required time to reach the Al_2O_3/Si interface results in about 1.8 nm/min and 2.3 nm/min for figures 3 and 4, respectively. This result could also indicate a difference in density between to two films.

Comparing the two depth profiles, the sample deposited in Ar appears to have a sharper interface. Silicon was only found near the Al_2O_3/Si interface and the small amounts of Al and O in the substrate area are caused by re-deposition of sputtered particles.

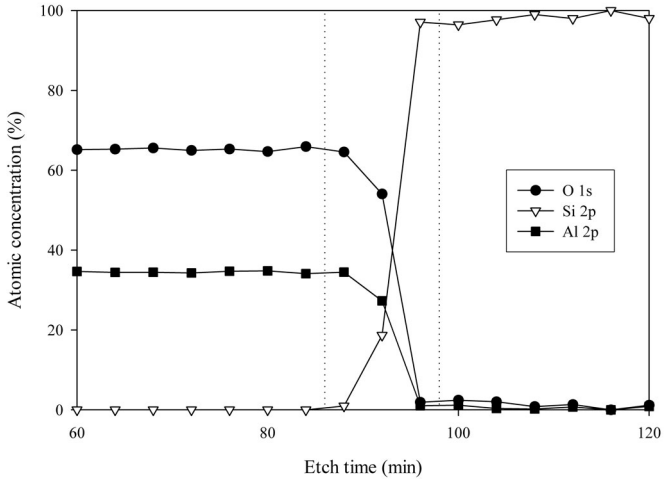

Fig. 3
DEPTH PROFILE OF AL_2O_3 DEPOSITED IN AR.

C. Electrical characterization

Results from electrical characterization will be presented on the poster.

V. CONCLUSION

Thermodynamic calculations have been used to estimate the interface effects during the pulsed laser deposition of Al_2O_3. The results showed that aluminum atoms can exchange positions with a silicon atom from the substrate. Surface scans by AFM and XPS depth profiles showed the significant difference between deposition in Ar and O_2. The films deposited in an Ar ambient appear to have a higher density and sharper Al_2O_3/Si interface. Electrical characterization of test structures with PLD gate dielectric will have to confirm interface mixing, a reduction in minority carrier mobility and effects of PLD deposition.

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