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A parallel architecture for implementation of filters based on order statistics

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Abstract

A new approach for implementing filters based on order statistics is proposed in this letter. As an illustration realisations of range, α-trimmed mean and WMMR filters are presented.

Keywords: Non-linear filters; Order statistics; Computer vision

1. Introduction

In recent years, significant advances have been made in the development of non-linear image processing methods, since these provide effective solutions to problems where linear techniques are not adequate (Pitas and Venetsanopoulos, 1990). One major category of non-linear filters consist of those based on order statistics (David, 1981). In this category belong the median, rank-order, range, α-trimmed mean, weighed majority with minimum range (WMMR), and other popular filters. Filters based on order statistics exhibit excellent robustness properties. For example, they can suppress high frequency and impulse noise, avoiding at the same time extensive blurring of the image. They have found numerous applications in digital image analysis, speech processing, coding, etc.

Non-linear filters based on order statistics have been hardware implemented in the past using the threshold decomposition (TD) technique (Fitch et al., 1985; Razi and Chu, 1995) and a bit-serial technique based on Positive Boolean Functions (PBF) (Chen, 1989). These architectures are fixed for a certain type of filter. Also, they can be realised through a sorting network (SN) with compare and swap elements (Pitas and Venetsanopoulos, 1990). A single and efficient structure for any rank order filter realisation based on the majority gate (MG) has been presented by Gasteratos et al. (1997). A comparative study for median filter implementation using 3×3 pixel image data of 8-bit resolution is shown in Table 1. In this letter a new real-time parallel architecture for implementing filters based on order statistics is presented. The proposed architecture is recon-

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Table 1
Hardware comparison of existing architectures for median computation using 3×3-pixel data of 8-bit resolution

	TD	PBF	SN	MG
NOT	–	8×18	36×24	8×52
AND2[a]	–	8×36	36×17	8×68
OR2	–	8×9	–	8×17
XNOR2	–	8×9	–	8×17
NOR2	–	–	36×8	–
NAND2	–	–	36×24	–
AND3	–	–	36×1	–
AND4	–	–	36×1	–
AND5	256×126	8×126	36×1	–
AND6	–	–	36×1	–
AND7	–	–	36×1	–
AND8	–	–	36×1	–
OR8	–	–	36×1	–
OR126	256×1	8×1	–	–
Decoder of 1 grey-level image to 256 binary images	1	–	–	–
Adder of 256 1-bit inputs	1	–	–	–

[a] The number denotes the inputs: e.g. AND5 is a five input AND gate.

figurable and realisations of range, α-trimmed mean and WMMR filters are presented.

2. Filters based on order statistics

The input of rank order filters is a data window with an odd number of elements. These elements are sorted in ascending order and the output of the rank order filter with rank r is the r-th element (r-th order statistic). Special cases of rank order filters are median, min and max filters.

Range filters are an extension of rank order filters (Bailey and Hodgson, 1985). Let $x_{(1)}, x_{(2)}, \ldots, x_{(N)}$ be the order statistics of the input data window. The output of this filter is

$$y = x_{(i)} - x_{(j)}, \tag{1}$$

where $1 \le j < i \le N$.

α-trimmed mean filters are a class of filters with properties varying between two extremes: the running average and the median filter (Razi and Chu (1995)). The output of this filter is

$$y = \frac{1}{N - 2[\alpha N]} \sum_{i=[\alpha N]+1}^{N-[\alpha N]} x_{(i)}, \tag{2}$$

where $[\alpha N]$ is the integer part of αN and $0 \le \alpha \le 1/2$.

When α is 0, the sum includes all inputs and, therefore, the output is the running average. On the contrary, when α is close or equal to $1/2$, the output of the filter is the median.

WMMR filters exhibit the same properties in impulse noise rejection and in edge preservation as do the other order statistics filters. Additionally, WMMR filters optimally enhance non-perfect edges (Longbotham and Eberly, 1993). Consider the weights $b_1, b_2, \ldots, b_{(N+1)/2}$, such that $b_j \ge 0$ and $\sum_{j=1}^{(N+1)/2} b_j = 1$. The ranges $x_{(j+(N-1)/2)} - x_{(j)}$, $j = 1, \ldots, (N+1)/2$, are calculated and let the minimum be obtained for $j = I_1, I_2, \ldots, I_l$, where $1 \le l \le (N+1)/2$. The output of this filter is

$$y = \frac{1}{l}\left[\sum_{j=1}^{(N+1)/2} b_j x_{(I_1+j-1)} + \sum_{j=1}^{(N+1/2)} b_j x_{(I_2+j-1)} + \cdots + \sum_{j=1}^{(N+1/2)} b_j x_{(I_l+j-1)} \right]. \tag{3}$$

3. Implementation of filters based on order statistics

A generalised computing hardware structure of a filter based on order statistics is shown in Fig. 1. The first stage of this structure consists of N order statistic modules (OSM) (Gasteratos et al., 1997), of

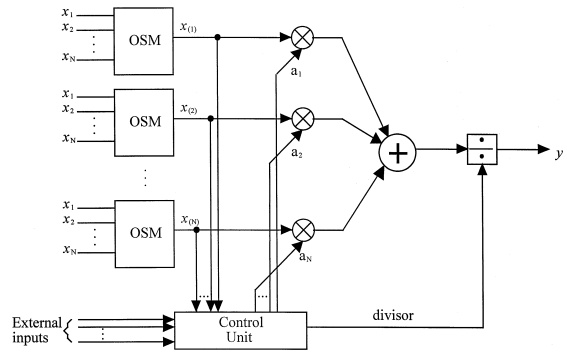

Fig. 1. Generalised computing hardware structure of a filter based on order statistics.

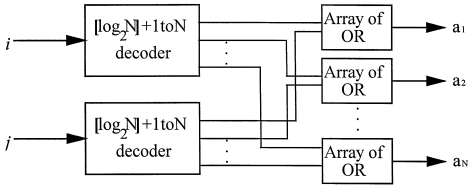

Fig. 2. Control unit for range filtering.

N inputs $(x_1, x_2, \ldots, x_N)$ each. A different order statistic $x_{(1)}, x_{(2)}, \ldots, x_{(N)}$ is provided by each of these modules. The control unit is associated with the type of the order statistic filter. The inputs to this unit are external inputs (the ranges and factor α in range and α-trimmed mean filters, respectively), or the order statistics (WMMR filters). The output of this unit are the divisor and coefficients $a_1, a_2, \ldots, a_N$, which are either 0 or 1 in most types of filters. These coefficients are multiplied with the corresponding $x_{(i)}$. In the case of WMMR coefficients, a_i are deduced from b_j, according to Eq. (3). Usually b_j are 0.5, 0.25, 0.125 or 0 (Longbotham and Eberly, 1993). Multiplication can be performed through shift registers and adders. The shift registers shift right $x_{(i)}$ one place, two places, three places or n places, respectively, where n is the resolution of $x_{(i)}$. Thus, products $b_j \cdot x_{(i)}$ are formed and are used as inputs to adders, in order to calculate products $a_i \cdot x_{(i)}$. The final stage of the proposed hardware structure is a divider.

The control unit for range filters is shown in Fig. 2. The external inputs to this unit are numbers i and j, which correspond to the order statistics that are subtracted, according to Eq. (1). These numbers are the inputs to two $[\log_2 N] + 1$ to N decoders. The output of the upper decoder is 1 at position i, and 0 elsewhere. The output of the other decoder is -1 at position j, and 0 elsewhere. The outputs of the two decoders, combined one-by-one through N arrays of OR gates, produce coefficients a_i.

The control unit for α-trimmed mean filters is a decoder having external input number α and outputs coefficients a_i. Table 2 contains the truth table of such a decoder for a 9-input data window. The intervals of the values of α, the coded values of α, which are the inputs to the decoder and coefficients a_i are shown in columns one, two and three, respectively. The divisor deduced from factor α is shown in the last column. For a relatively small image data window and pixel resolution, the required division can be efficiently performed through a Look Up Table (LUT). For example, in the usual case of Table 2 and with 8-bit resolution numbers, a LUT of $2304 = 9 \times 2^8$ memory locations is required.

The control unit for WMMR filters is shown in Fig. 3. The ranges $x_{(j+(N-1)/2)} - x_{(j)}$ are computed by means of $(N+1)/2$ subtractors. The minimum range is calculated through an $(N+1)/2$ input OSM. In order to trace the positions $(I_1, I_2, \ldots, I_l)$ of the minimum range, the ranges and the minimum range are used as inputs to arrays of XOR gates. These produce 0 everywhere, except at the positions of the minimum range, where the outputs are 1. The outputs of each array of XOR gates are then fed into an OR gate, to produce a single bit output, which determines the positions of the minimum range. The outputs of the latter gates are connected to a combinational circuit with $(N+1)/2$ inputs and N outputs, corresponding to coefficients a_i. The outputs of the OR gates are also used as inputs to an adder, which produces the divisor l. An illustrative truth table of such a combinational circuit for $N = 5$ and $\{b_1, b_2, b_3\} = \{0.25, 0.5, 0.25\}$ is shown in Table 3.

Table 2
Functional table for realisation of α-trimmed mean filters

α	Coded α	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8	a_9	$N - 2[\alpha N]$
$0 \le \alpha < 1/9$	000	1	1	1	1	1	1	1	1	1	9
$1/9 \le \alpha < 2/9$	001	0	1	1	1	1	1	1	1	0	7
$2/9 \le \alpha < 3/9$	010	0	0	1	1	1	1	1	0	0	5
$3/9 \le \alpha < 4/9$	011	0	0	0	1	1	1	0	0	0	3
$4/9 \le \alpha < 1/2$	100	0	0	0	0	1	0	0	0	0	1

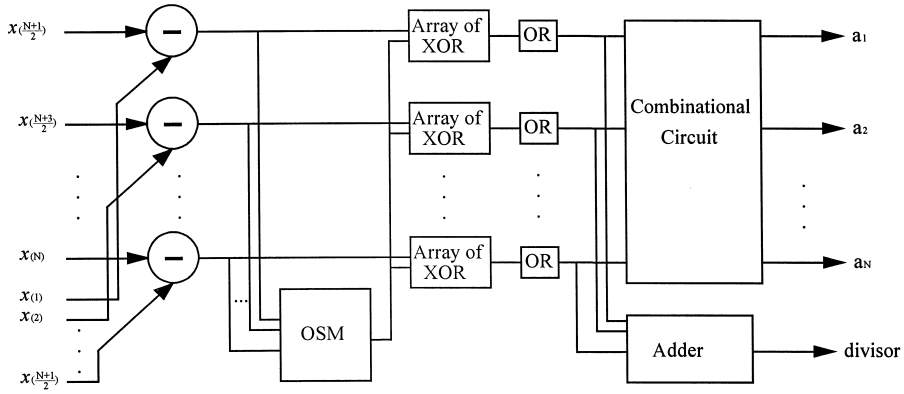

Fig. 3. Control unit for WMMR filtering.

The first three columns are all the possible OR gates outputs, which correspond to the positions of the minimum range. The next five columns are coefficients a_i, which are computed from coefficients b_1, b_2 and b_3, according to Eq. (3).

Range and α-trimmed mean filters can be realised through an SN with compare and swap elements, the TD and the PBF techniques. Table 4 presents an illustrative example for the hardware requirements of the proposed architecture, TD, PBF and SN techniques, for a 5-pixel window and 8-bit pixel resolution. Table 5 shows the number of transistors required for each standard cell mentioned in Table 4. From both Tables 4 and 5 it is obvious that the proposed architecture is superior in terms of silicon area, when compared with the TD technique. Furthermore, in the MG technique, hardware complexity grows linearly both in terms of the number of inputs and resolution of pixels, whereas in the TD technique, it grows exponentially. In the presented example, the PBF and MG techniques are comparable in terms of hardware complexity. However, in the PBF technique, hardware grows as a function of $N!$; for example, in the median filter this function is $N!/([N/2]![1+N/2]!)$ (Lee and Jen, 1992). Thus, even for the typical 3×3-pixel window, the MG technique becomes advantageous. Both techniques can attain very high operation speeds, the MG technique being slightly faster, due to the presence of an extra multi-input gate level in the PBF implementation. Also, in the presented case, the SN requires less silicon area than that of the MG technique. Here, hardware complexity is proportional to a factor $N[N/2]$ (Lee and Jen, 1992). Therefore, for larger size input windows, the MG technique becomes more attractive than the SN technique. Additionally, the SN is rather slow when compared with the MG technique. This is due to the fact that the processing element of the MG technique consists of only three levels of gates (Gasteratos et al., 1997), whilst each compare and swap element consists of eight levels of gates (includes a comparator and a multiplexer).

Table 3
An example truth table for the combinational circuit of Fig. 3 ($N=5$ and $\{b_1, b_2, b_3\}=\{0.25, 0.5, 0.25\}$)

$x_{(3)}-x_{(1)}$	$x_{(4)}-x_{(2)}$	$x_{(5)}-x_{(3)}$	a_1	a_2	a_3	a_4	a_5	Divisor
0	0	1	0	0	0.25	0.5	0.25	1
0	1	0	0	0.25	0.5	0.25	0	1
0	1	1	0	0.25	0.75	0.75	0.25	2
1	0	0	0.25	0.5	0.25	0	0	1
1	0	1	0.25	0.5	0.5	0.5	0.25	2
1	1	0	0.25	0.75	0.75	0.25	0	2
1	1	1	0.25	0.75	1	0.75	0.25	3

Table 4
An illustrative example for the hardware requirements of the TD, PBF, SN and MG techniques, for a 5-pixel window and 8-bit pixel resolution

TD	256 binary max filters	256 binary 4th largest filters	256 binary median filters	256 binary 2nd largest filters	256 binary min filters	1 decoder of 1 grey-level image window to 256 binary image windows	1 adder of 256 1-bit inputs (128 half adders + 64 2-bit adders + 32 3-bit adders + 16 4-bit adders + 8 5-bit adders + 4 6-bit adders + 2 7-bit adders + 1 8-bit adder)
	256×1 OR5	256×(1 AND5 + 5 5 OR4)	256×(1 OR10 + 10 AND3)	256×(1 OR5 + 5 AND4)	256×1 AND5	5 ROMs (256×256) bits	128 AND2 + 502 XOR2 + 748 NAND2 + 374 XNOR2 + 247 NAND3 + 127 NOR2 + 127 NOR3 + 63 NOR4 + 31 NOR5 + 15 NOR6 + 7 NOR7 + 3 NOR8 + 1 NOR9
PBF	1 max filter	1 4th largest filter	1 median filter	1 2nd largest filter	1 min filter		
	8×(10 NOT + 20 AND2 + 5 OR2 + 5 XNOR2) + 8×(1 OR5)	8×(10 NOT + 20 AND2 + 5 OR2 + 5 XNOR2) + 8×(1 AND5 + 5 OR4)	8×(10 NOT + 20 AND2 + 5 OR2 + 5 XNOR2) + 8×(1 OR10 + 10 AND3)	8×(10 NOT + 20 AND2 + 5 OR2 + 5 XNOR2) + 8×(1 OR5 + 5 AND4)	8×(10 NOT + 20 AND2 + 5 OR2 + 5 XNOR2) + 8×(1 AND5)		
SN	10 Compare and Swap circuits						
	10 Comparators					10×(8 multiplexers 2×1)	
	10×(16 NOT + 17 AND2 + 8 NOR2 + 1 AND3 + 1 AND4 + 1 AND5 + 1 AND6 + 1 AND7 + 1 AND8 + 1 OR8)					10×(8×(1 NOT + 3 NAND2))	
MG	5 OSMs						
	5×(8×(28 NOT + 36 AND2 + 9 OR2 + 9 XNOR2))						

Table 5
Hardware requirements, in terms of transistors (CMOS technology), for each standard cell of Table 4

Number of transistors	Standard cell
2	NOT
4	NAND2, NOR2
6	AND2, OR2, NAND3, NOR3
8	AND3, NOR4
10	AND4, OR4, NOR5
11	XOR2, XNOR2
12	AND5, OR5, NOR6
14	AND6, NOR7
16	AND7, NOR8
18	AND8, OR8, NOR9
22	OR10

Hardware structures for WMMR filters have not been reported in the literature yet.

4. Conclusions

A parallel architecture for implementing filters based on order statistics has been presented in this letter. Different filters based on order statistics are obtained, by altering the *Control Unit*. Efficient realisations of range, α-trimmed mean and WMMR filters have been illustrated.

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