

Multi-Channel Data Acquisition for a Free-Towed Synthetic Aperture Sonar

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Abstract: This paper describes the data acquisition system developed for the KiwiSAS-III Synthetic Aperture Sonar (SAS), developed by the Acoustics Research Group at the University of Canterbury. This sonar system is designed to provide high resolution imagery of the seafloor in a shallow water environment. The data-acquisition system is based around a custom rack of electronics interfaced to a standard PC for data storage and display. A central design feature is the fully synchronous nature of all real-time components to ensure coherent image processing techniques can be applied to the data.

Keywords: Data-acquisition, Digital Down Converter, FPGA

1. INTRODUCTION

The KiwiSAS-III is a free-towed, side scanning sonar system being developed by the Acoustics Research Group at the University of Canterbury. The system is designed as a completely coherent system allowing post-processing signal processing to be applied to the data. In particular, research is being performed on Synthetic Aperture Sonar (SAS) algorithms and bathymetric terrain mapping.

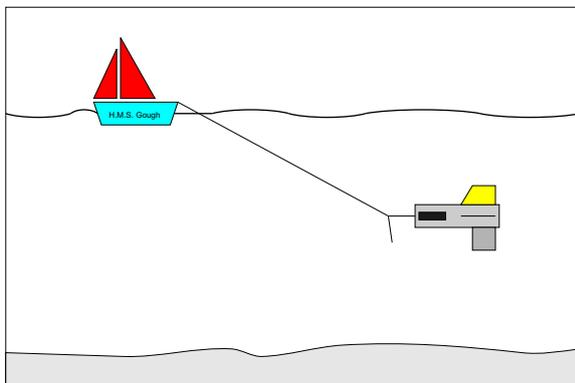


Figure 1: KiwiSAS system in operation.

There are two major components to the system; the free-towed towfish, and the towboat hardware as outlined in Figures (1, 2). The towfish is a nose towed,

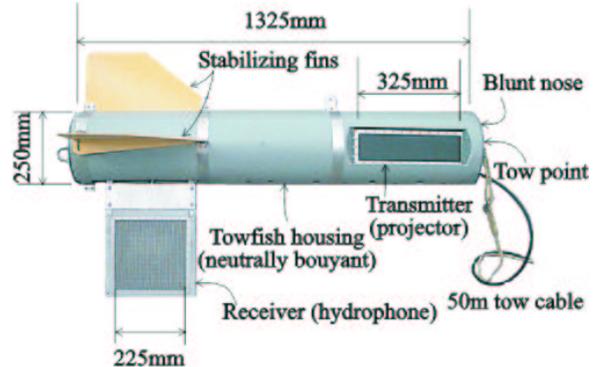


Figure 2: KiwiSAS-III towfish.

blunt nose design with stabilizing fins at the rear. These features are intended to make the towfish more stable when towed reducing blurring of the resulting imagery. The towfish is connected to the towboat via a 50 m multi-core towcable. To minimise the complexity and cost of the water sealed towfish the data acquisition hardware is located on the towboat, with all data signals to and from the towfish in an analogue form. The system is designed to operate in a continuous data acquisition mode and due to the coherent nature of the data processing, all real-time parts of the system must operate synchronously. The data acquisition hardware is mounted in a standard 19" Eurocard rack, connected to a standard PC via a custom PCI card.

2. TOWFISH ELECTRONICS

The towfish can be considered to have three separate sub-systems. These consist of the transmitter, receiver, and instrumentation as shown in Figure (3). Each of these three sub-systems are independent except for a common power supply.

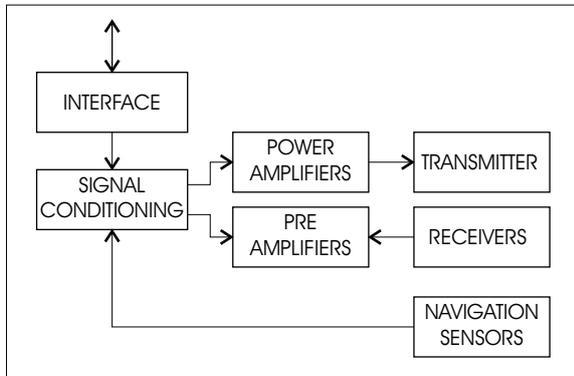


Figure 3: Block diagram of towfish electronics.

The transmitter consists of 12 power amplifiers, each amplifier driving three Tonpilz[1] projectors. All amplifiers are driven with the same signal, so no electrical beam steering is available. The power amplifiers are powered directly off the ± 12 V lines of the towcable. Power decoupling is provided via two capacitor banks of 42000 μ F each within the towfish. These capacitor banks ensure the supply voltage does not droop during the period of transmission.

The receiver hydrophone consists of nine 75×75 mm PVDF tiles arranged in a 3×3 grid. Each row of three are wired in parallel and connected to a 40dB pre-amplifier. These three signals are sent to the towboat via the towcable using differential line transmitters (EL2140C).

In order to estimate the orientation of the towfish an instrumentation package is included in the rear can of the towfish. This device contains an inclinometer, magnetometers, and accelerometers. These sensors are interfaced using an 8-bit microcontroller, and the resulting digital data stream sent to the towboat using NMEA type sentences via an RS-232 link[2].

3. TOWBOAT ELECTRONICS

Since this sonar system is designed to be operated from a variety of small vessels the system must be simple, self contained and easy to transport. On board the boat all equipment is housed in small, sturdy containers with large transportation handles. The overall towboat setup is outlined in Figure (4).

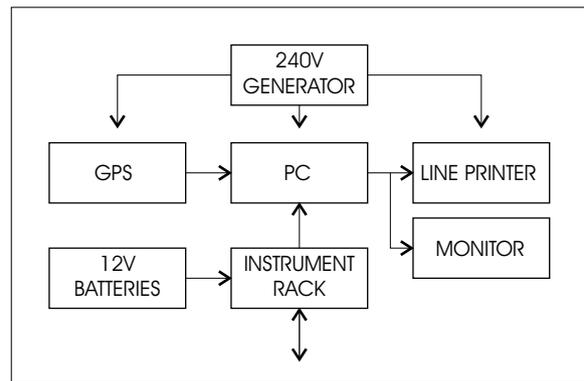


Figure 4: Block diagram of towboat electronics.

3.1 Central Computer

The central computer is an off the shelf dual-processor Pentium III system running the Linux operating system. This computer is mounted in a sturdy metal box with large handles to ease transportation. This central computer primarily records the incoming data from the instrument rack of Section 3.3 via a custom built PCI interface card[3]. This data is recorded onto a standard IDE hard-disk in raw form to allow post processing to be performed.

During data collection some form of feedback to the boat crew is required to ensure correct operation of the system. To do this, the data is pulse-compressed (correlated with the transmitted signal) and displayed on a flat screen monitor in real time. This display stream is user configurable providing valuable information to the boat crew. The data is also recorded in a hard form using a thermal line printer. This provides a longer term history of the sonar operation. The software application running on the computer consists of two main programs. The background task provides the real time data acquisition and storage of the incoming data streams. The second task provides the visual display of this recorded data, and also any real-time processing as required. Only the raw data stream is recorded to the disk, all other processing is only used for visual display.

3.2 Auxiliary Systems

A standard 12 channel GPS receiver on the boat provides a basic navigation recording. This positioning information is transferred to the central computer as NMEA type sentences via a serial RS-232 connection. These sentences are then tagged to synchronise the data streams from the towfish and recorded onto the disk. This positioning information is of limited use for the development of synthetic aperture algorithms since the GPS receiver must be located on the towboat and not the towfish.

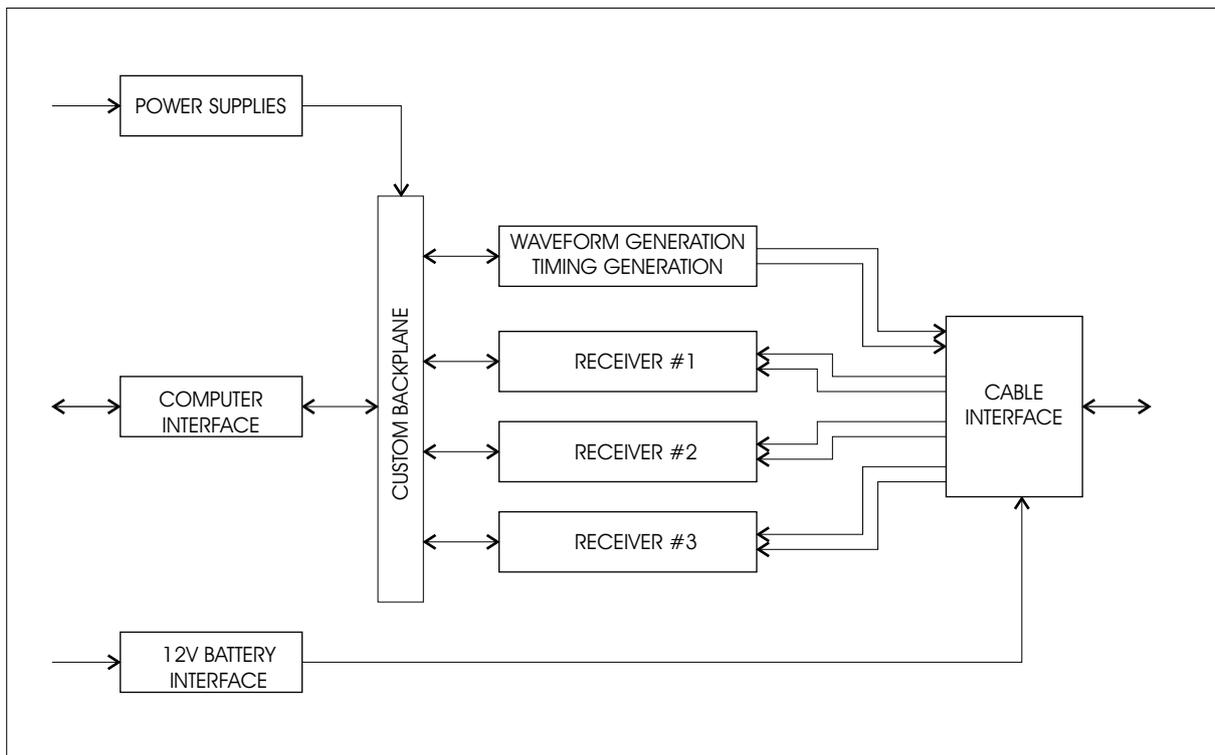


Figure 5: Block diagram of towboat instrumentation rack electronics.

Power for all the systems on the boat is generated by a portable petrol 240 V generator. The towfish is powered separately from two large capacity, deep cycle 12 V lead-acid batteries. These batteries help reduce electrical switching noise in the towfish electronics by separating the power supplies of the towfish and the towboat.

3.3 Instrument Rack

The rack of electronics on board the boat provides the heart of the real-time sonar system. This rack provides all the interfacing between the computer and the towcable, as outlined in Figure (5). It is housed in a 19" Eurocard rack, utilising a custom backplane for communication between the cards. Each card in the rack is allocated a unique four-bit card number by jumpers on each card. This then allows the cards to be individually addressed from the central computer.

3.3.1 Backplane. The backplane is the only communication channel between the various cards within the rack. Connections to each card are provided via 16 64-pin DIN connectors spaced at a distance of 4HP (1HP=5.08mm). It is an entirely passive device with three main groups of signals. The top 32 pins of each connector are connected in a parallel bus, used for digital communication between the cards. The next 14 pins are used for DC power supplies to each of the cards as outlined in Section 3.3.2. The bottom 18 pins

of each connector are divided into six groups of three providing analog connections to each card. Rather than being connected to all cards as a bus, these connections are to connectors on the back of the backplane. This then allows a point-to-point connection of these signals to be made as required.

3.3.2 Power Supplies. The entire electronics rack is designed to run from a single 240 V AC power source. From this several raw DC power supplies are derived using a single transformer with multiple secondary windings. These raw supplies are ± 8 V used for analog supplies, +8 V for digital supplies, and ± 15 V for auxiliary supplies. Each of these raw supplies is routed along the backplane to all cards, each of which linearly regulate the supplies as required. Typically the 8 V lines are regulated to 5 V and the 15 V lines are regulated to 12 V. By separating the analog and digital supplies at the power transformer noise is minimised. Each of the supplies has separate ground returns, and are completely isolated from each other. In order to ensure common ground potential between the analog and digital supplies, these grounds are connected by 0Ω resistors under the AD converter on each of the receiver cards.

3.3.3 Computer Interface. This is a simple card providing buffering and termination of the high speed serial link to the computer and the backplane. It also contains a phase locked loop (PLL) chip (MC88915)

to provide the main 40 MHz clock for the entire system. Buffering between the computer and backplane is achieved using HCT family buffers.

3.3.4 Timing/Waveform Generation Card. This card has two primary functions. The first is to generate all the timing signals to control the other parts of the system. The second is to generate the arbitrary analog waveforms used as the acoustical transmitted signal. Central to this card is an FPGA (XILINX XC4003E), booted from an onboard serial PROM chip (XC17108E). This FPGA device is configured with several internal registers addressable via the backplane.

The overall timing of the system is controlled via two internal registers of the FPGA. These registers control the length of the transmitted waveform and the overall repetition period of the waveform. These timing signals are transmitted to the other cards in the system via the digital portion of the backplane. They are also buffered and routed to BNC test connectors on the front panel.

The arbitrary signals used by the sonar are downloaded into a field memory device from the central computer, via the FPGA. These waveforms are then converted to an analog signal using a dual-channel, 12-bit, digital to analog converter (DAC7801).

The outputs of the DAC are then buffered and passed out to the backplane via differential transmitters (EL2140C). The single ended signal is also routed to a BNC test point on the front panel via a dedicated buffer. This allows an oscilloscope to be connected to monitor the transmitted signal. There is no gain control over any of the transmitted signals, other than varying the maximum digital code stored in the Field Memory. This is because the transmitter of the sonar is always operated at maximum signal levels to maximize acoustic response.

3.3.5 Receiver Card. The primary role of the receiver cards is to take the incoming differential signals from the towfish and convert them into a suitable digital format for storage on the computer harddisk. Each card has two independent, identical receiver channels. To provide synchronicity between all the receiver channels, all devices are controlled from the same clock and timing signals from the waveform card. Each receiver channel consists of an analog shaping stage, the digital conversion, and then digital down conversion to lower the data rate.

Each channel is initially sampled as 12-bits 40 MSps, and then down-converted to 16-bit real, 16-bit imaginary samples at approximately 30 kSps. The data is sampled at a much higher than Nyquist rate and

down-sampled to a lower rate, allowing low order anti-aliasing filters to be used. This simplifies the filter design, reducing the phase effects within the resulting signal spectrum.

The incoming differential signal from the towfish are terminated and converted to a single ended signal using a differential receiver (EL2142C); the matched receiver to the transmitter in the towfish. The input of the receiver may also be switched via a relay to an auxiliary test input from the backplane. This allows a known test signal to be used as the input for any of the receivers to test their operation. This relay is under software control from the PC. The single ended signal then passed through a gain stage (AD603), variable from -10 dB to +30 dB, again under software control. This allows the maximum signal to be applied to the ADC without overloading it. From the output of the variable gain stage the signal is low pass filtered using a LCL filter module (P3LP-300) with a cutoff frequency of 300 kHz. This filtered signal is then applied to the input of the ADC (CLC952) via a center-tapped transformer, driven by a unity gain buffer. The transformer is necessary to level shift the signal from a bipolar signal to a unipolar signal suitable for the input of the ADC. The ADC input is also routed to the front panel for monitoring via a dedicated buffer.

The AD converters are operating at the full 40 MHz clock frequency, performing 12-bit signal conversions. This digital data is bussed to a Digital Down Converter (DDC) (HSP50016) chip performing a frequency shift and decimation of the data stream. The operation of the DDC is under complete software control, allowing tuning of the internal circuitry to the desired spectrum portion of interest.

This card is digitally controlled from a Complex Programmable Logic Device (CPLD) (XC95108). This device also time division multiplexes (TDM) the serial data streams from the two DDC devices. Each DDC produces a 33-bit data word, consisting of a frame pulse followed by 32 data bits. The data streams from each of the three receiver cards are then combined into one serial TDM stream, transmitted to the PC via the custom PCI card, as shown in Figure (6).

Data from the three receiver cards is time division multiplexed together to form one data stream for transmission to the PC. This is achieved by allocating each card a unique slot number within the data stream. Each card then holds the serial lines in a tri-state condition until their time slot is reached. The card then drives the serial lines with the data from the two DDCs, then returns to a tri-state condition to allow another card to take control of the bus. This time slot allocation is achieved by setting a register within the receiver card CPLD.

The power supplies for the card are derived from the raw DC supplies of the backplane, linearly regulated

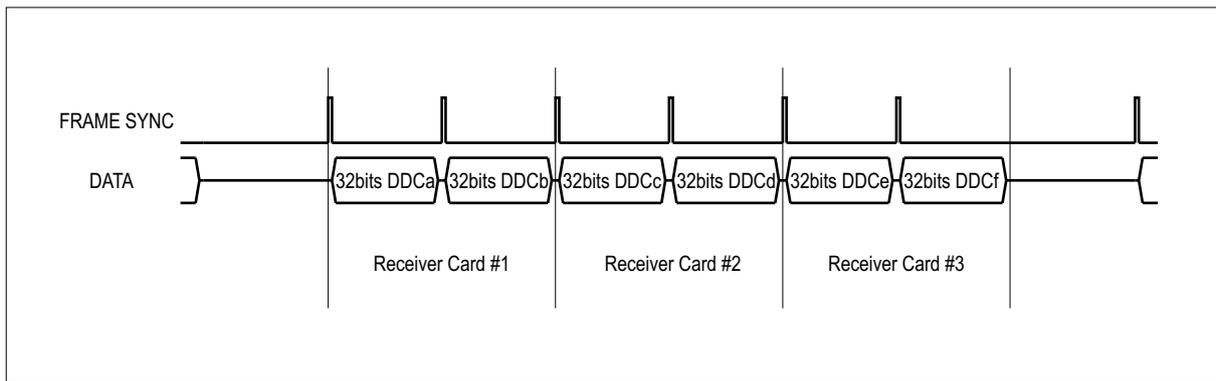


Figure 6: Time division multiplexed bus for data.

to $\pm 5V$ for the analog circuits and +5 V for the digital circuits. This separation of the power supplies is to reduce the interference from the digital switching into the analog signals.

4. EXAMPLE DATA

Results from a test site in Sydney Harbour, Australia are shown in Figure (7). This scene contains several man-made objects including several point reflectors, and a ladder-like structure. Also present is a natural bland background.

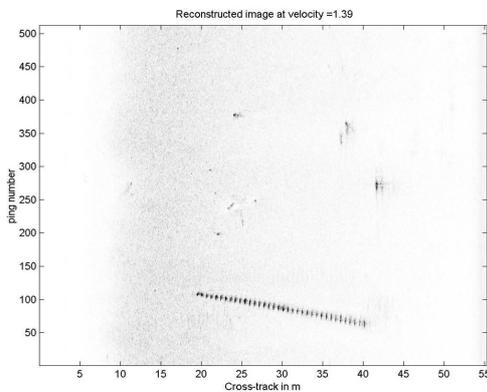


Figure 7: Sonar image from a test site in Sydney Harbour, Australia after synthetic aperture with autofocus processing has been applied.

5. KIWISAS-IV

The KiwiSAS system is currently under reconstruction to incorporate a new array of receiver elements, increasing the total number of receiver elements to 18. This will allow further work in the autofocus field to be performed. This will also allow faster towboat operation or an increase in imaging range. The transmitter is also being redesigned to allow the individual elements to be driven with independent signals. This will

allow the transmitted beam to be steered in azimuth. This increase in both transmitter and receiver channels has necessitated the inclusion of a computer system within the towfish housing and the development of a new multi-channel data acquisition system[3]. This new system will also incorporate a new navigation system to precisely position the towfish while imaging. This system will use fixed transponders placed on the seafloor in a long baseline configuration [4, 5].

6. CONCLUSION

The KiwiSAS-III system has been used to collect sonar data on several occasions in various locations. This data has allowed algorithms to be developed for a number of image processing stages, including synthetic aperture reconstruction, direct autofocus[6], statistical autofocus[7] and bathymetry[8, 9]. The hardware described here is an essential part of the data collection process, shown to be reliable under a range of trying conditions.

7. ACKNOWLEDGEMENTS

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Imagery in Section (4.) collected on sea-trials of the KiwiSAS system for the Australia Defense Science Technology Organisation (DSTO).

8. APPENDIX

- XILINX www.xilinx.com
XC95108 In-System Programmable CPLD
XC4003 Field Programmable Gate Array
XC17108 Serial Configuration PROM

- Analog Devices www.analog.com
CLC952 12-bit, 41 MSPS Monolithic A/D Converter
AD603 Low Noise, 90 MHz Variable-Gain Amplifier
- Burr-Brown (Texas Instruments) analog.ti.com
DAC7801 Dual Monolithic CMOS 12-bit Multiplying Digital to Analog Converters
- OKI Semiconductor www.okisemi.com
MSM518221 282,214-Word \times 8-bit Field Memory
- Motorola www.motorola.com
MC88915 Low Skew CMOS PLL Clock Driver
- Harris (Intersil) www.intersil.com
HSP50016 Digital Down Converter
- Elantec (Intersil) www.intersil.com
EL2140 Differential Twisted Pair Driver
EL2142 Differential Line Receiver
- Coilcraft www.coilcraft.com
P3LP Low Pass LC Filter Modules
WB2010 Wide Band RF Transformers

9. REFERENCES

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