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Single-electron and quantum SOI devices

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Abstract

This paper describes, from the viewpoint of device fabrication, single-electron and quantum devices using silicon-on-insulators (SOIs). We point out that control of the oxidation of Si is quite important and could be the key to their fabrication. We also introduce our technique for making single-electron transistors (SETs), which uses special phenomena that occur during the oxidation of SOIs, and show that the technique enables us to realize primary single-electron circuits as a result of its high controllability and high reproducibility.

Keywords: Silicon-on-insulator; Single-electron transistor; Quantum device; Oxidation

1. Introduction

According to the International Technology Roadmap for Semiconductors, the gate length of the MOSFETs in MPUs will reach 20–22 nm in 2014. At these sizes, quantum effects originating from single-electron charging and from low-dimensional subbands become effective. Quantum devices utilizing these effects will therefore become significant at that time or later. However, it will not be easy to merge quantum devices into MOS LSIs with already-high and ever-improving performance. In order to achieve this goal, it is crucial to establish a technology that makes it as easy to fabricate quantum devices with excellent controllability as it is to fabricate MOSFETs. In this paper, after briefly reviewing quantum devices that use silicon-on-insulators (SOIs), we will focus on their fabrication and point out that control of thermal oxidation of Si could be a key process. Then, as a clue for the mass-production of quantum SOI devices, we will introduce our technique for making single-electron transistors (SETs), which uses special phenomena that occur during the oxidation of SOIs.

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2. Quantum SOI devices and impact of thermal oxidation on their fabrication

Using Si for quantum devices is quite important because this enables us to combine them with MOSFETs, which is expected to enhance the advantages of each device, leading to higher-performance LSIs. SOIs are promising base materials for Si quantum device research because they provide a thin sheet of single-crystalline Si and allow the formation of lower-dimensional structures with the help of lithography. In addition, the large band-discontinuity of SiO_2/Si interfaces would be beneficial for the high-temperature operation of the quantum devices because of the strong confinement of electrons. Therefore, SOI quantum devices have been widely studied. Among them, single-electron devices are attracting the most attention. One [3] of the earliest observations of SET characteristics in Si [1–3] was actually done using SOIs. The first demonstration of the high-temperature operation of a SET was also achieved using SOIs [4]. Ever since these pioneering studies, single-electron tunneling has been observed by many groups [5–10] and a large variety of single-electron devices and primary circuits, including a single-charge transfer device with a unique operation principle [11] have been demonstrated [11–22]. There are also a lot of reports on the fabrication of one- and two-dimensional quantum structures using SOIs [23–35], and some have suggested, from photoemission spectra [35] and electrical characteristics [23,29–31], the formation of subbands originating from SiO_2 confinement barriers.

Despite such efforts, however, single-electron-device research still focuses mainly on one device, although quite a few groups are studying combined SETs. Whether the subband formation due to SiO_2 barriers occurs is still unclear, and resonant tunneling through one- or two-dimensional subbands, to the best of our knowledge, has not yet been demonstrated in SiO_2/Si system. This situation is mainly a result of a lack of technologies for fabricating quantum structures with good controllability for systematic investigation of the systems.

The difficulty in making quantum devices is obviously due to their small size. Control of nanometer-scaled thickness, area, and volume is not easy even when state of the art lithography and/or self-organization techniques are used. The solution to this problem could be control of the thermal oxidation of Si. Thermal oxidation converts Si to SiO_2 and consequently reduces the size of the Si, making it possible to produce structures that are much smaller than the critical dimensions of lithography. Furthermore, some unique features of oxidation of nanometer-scaled Si arising from oxidation-induced stress might be applicable to the formation of quantum structures and their size control. One is *pattern conversion* [31,36,43]. An example of this is shown in Fig. 1. These are transmission electron microscope (TEM) images of post-oxidation SOIs that had a flat Si layer before oxidation. Splitting of the Si layer occurs only when it was initially thin (Fig. 1c and d). This is because accumulation of stress around the edges of the wire suppresses oxidation there. (Oxidation-rate reduction similar to this occurs when narrow Si pillars [37] and dots [38] are oxidized, which is referred to as self-limiting oxidation [37].) Fig. 1 shows that the size of the resultant narrow wires is independent of the initially-defined wire width and indicates that we can make narrow quantum wires beyond critical dimension of lithography in a controlled way. Another feature is *band-profile modulation* [39]. Fig. 2 shows results of the first-principle calculations of the change in the bandgap of Si as a function of strain for a Si wire with valley direction as a parameter. The data indicate that we can modify the band profile of Si intentionally by introducing local strain at a desired area, which is achievable by using the oxidation-induced stress.

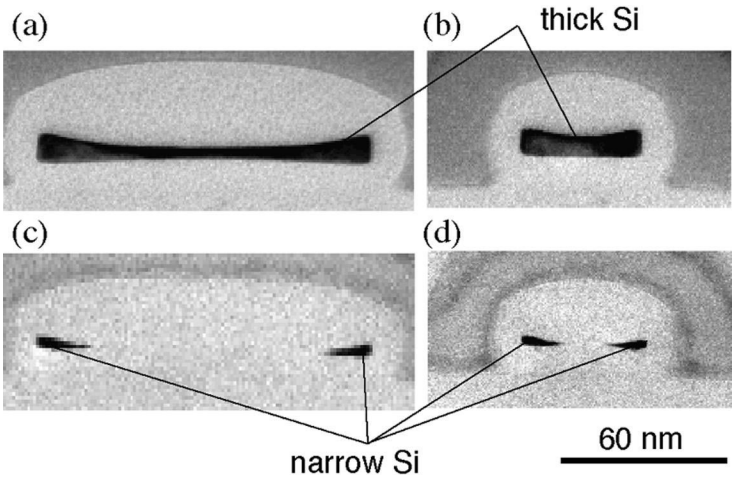

Fig. 1. Cross-sectional TEM images of Si wires after oxidation at 900°C. Initial thicknesses of Si were 22 nm for (a) and (b) and 14 nm for (c) and (d).

3. Pattern-dependent oxidation for fabricating single-electron transistors

We have developed a special method of fabricating SETs that exploits the above-mentioned properties of oxidation in a very sophisticated way. The method is called pattern-dependent oxidation or PADOX [4,40–42] because the shape of the pre-oxidation pattern of Si and the oxidation conditions determines the final physical and electrical structures of the devices. (We have actually fabricated some devices by changing the initial patterns [12,17].) Fig. 3 shows a version of PADOX, where the initial pattern is vertically modulated (hence this is called vertical PADOX or V-PADOX) [43]. In V-PADOX, the pattern conversion shown in Fig. 1 is employed, and a narrow and short wire is automatically formed at the edge of the thin region. Tunnel barriers (made of Si, not of SiO_2) are also

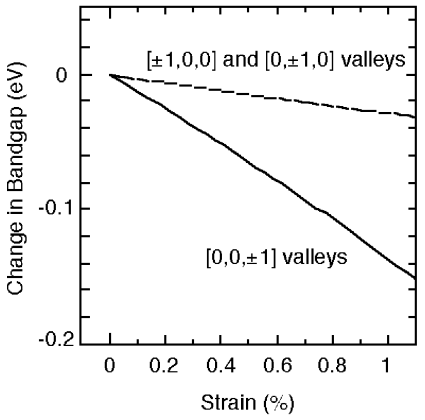

Fig. 2. Change in bandgap of Si as a function of strain for a Si wire with valley direction as a parameter.

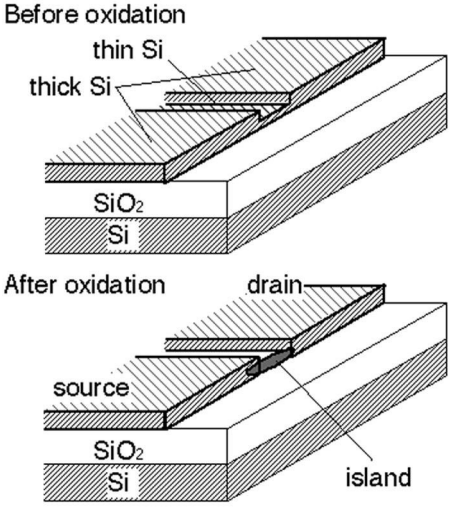

Fig. 3. Pattern conversion by V-PADOX.

formed around the boundaries between the resultant narrow wire and thick regions. We infer from theoretical considerations that this automatic tunnel-barrier-formation results from two competing effects on the band-profile modulation: a bandgap increase due to the quantum confinement effect and a bandgap decrease due to the above-mentioned strain effect. These two effects are expected to form a potential profile for the SET, i.e., two bumps for barriers and a well acting as an island [44].

One of the remarkable features of PADOX (including V-PADOX) is that it offers high controllability of the size of the island and electrical parameters of SETs. For example, the gate capacitance can be controlled by changing the structural parameters of pre-oxidation Si patterns [41,43]. In addition, especially in V-PADOX, automatic formation of narrow Si (Fig. 1) leads to better control of island size, and this has enabled us to demonstrate operations of some primary single-electron circuits, part of which will be shown in the next section.

Another feature of PADOX is that the SETs are definitely stable for thermal cycling. Fig. 4 shows

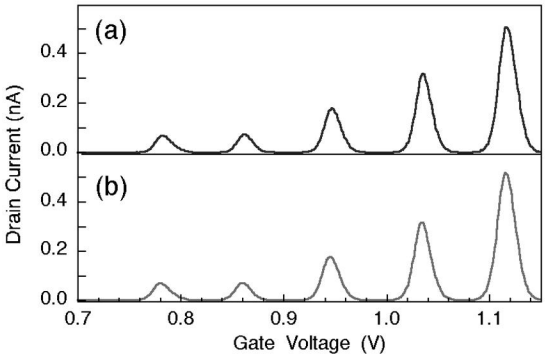

Fig. 4. Drain current vs. gate voltage characteristics of a SET, measured at 27 K with a source–drain voltage of 10 mV, on May 10, 1999 (a), and on April 13, 2001 (b).

the current characteristics of a SET fabricated using V-PADOX. The curve in Fig. 4a was obtained within a month after fabrication while that in (b) was obtained two years after the former measurements. Between the two measurements, the device temperature was cycled between ~30 K and room temperature several times. The curve does not change within the accuracy of the measurement system used, indicating that the SET is not influenced by random mobile charges, which in general fatally unstabilize the current characteristics of SETs. This is not surprising because the base material and fabrication process for our SETs are fundamentally the same as those for the MOSFETs, which is of course very stable. As for immobile random offset charges, although we have not yet obtained available data, we expect that control of the offset of the current characteristics would not be much more difficult than the threshold voltage control of MOSFETs, provided that the size of the island is precisely controlled.

4. Circuit operations by single-electron transistors

Since the potential of SETs for low-power dissipation can best be taken advantage of by using them for logic LSIs, we have so far tried to demonstrate, using SETs made with V-PADOX, logic and arithmetic operations [20,21]. The following describes 'half sum' and 'carry-out' operations for an adder based on a pass-transistor-logic scheme [21].

Fig. 5 shows structure of the circuit for half-sum and carry-out operations. (Half-sum calculates the lower-order bit from the addition of two 1-bit operands, while carry-out calculates the high-order bit.) The circuit consists of two SETs with individual input gates and common output terminal. The pattern before the input-gate formation (Fig. 5a and c) is a three-terminal Si wire containing a thin region.

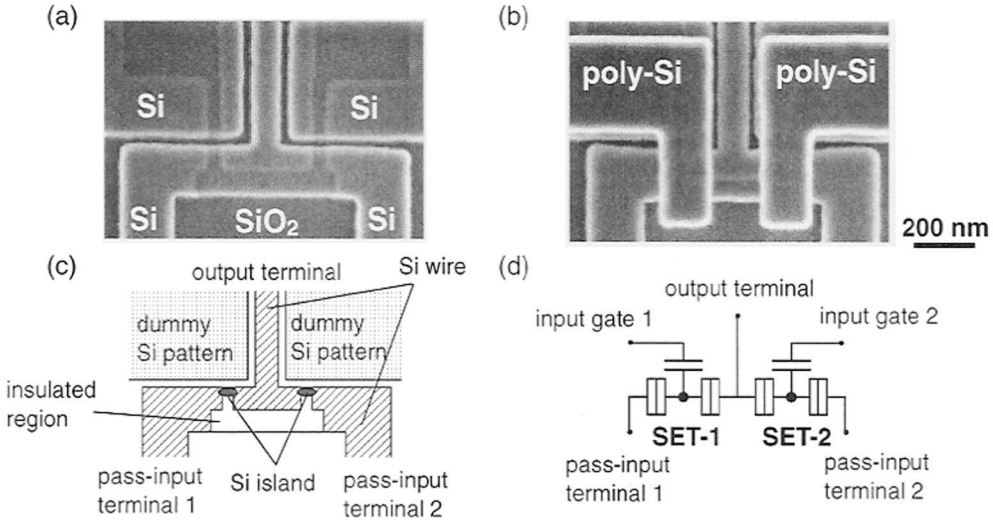

Fig. 5. Structure of the circuit. SEM images before (a) and after (b) input-gate formation, schematic view of the pattern before input-gate formation (c), and the equivalent circuit (d). In (c), the white area is the thin region that becomes insulated after oxidation.. The dummy Si patterns, positioned on both sides of the output node, were grounded throughout the electrical measurements (Figs. 6 and 7).

The thin region consists of a broad part and two narrow branches. After thermal oxidation, a SET island is formed at each end of the branches and the remaining part of the thin region becomes insulated [19]. Thus, we can automatically get two SETs with a common output terminal. In fabrication, we first formed a 15-nm-deep trench in a flat (about 40-nm-thick) SOI layer by using reactive ion etching to make a thin region of Si. The three-terminal Si wire was then defined in such a way that the wire overlaps the trench. Next, PADOX was carried out at 900°C for the island formation, which was followed by the poly-Si input-gate definition. We used EB lithography for the trench, wire, and input-gate formation steps. Finally, we again deposited poly-Si to form a top gate. The top gate covers the entire pattern shown in the scanning electron microscope (SEM) image of Fig. 5b, and was used to generate inversion channels in the Si wire, which work as leads for the SETs.

The measurements were done at 25 K with the top gate voltage kept at 2 V. We first measured the current vs. input gate voltage characteristics of the SETs. The results are shown in Fig. 6. The measurement configurations are also shown in the figure. For the measurements, one of the SETs was pinched off by applying a negative (−1 V) input gate voltage, and the current flowing from each pass-input terminal was measured with a source–drain voltage of 4 mV. It can be seen that the oscillation periods and phases are nearly the same for the two SETs. The gate capacitance and the total capacitance are respectively 2.7 and 7.0 aF for SET-1, and 2.6 and 7.5 aF for SET-2. Fig. 7 shows the experimental data for the half-sum and carry-out operations. The input voltage configurations are also shown in the figure. The first current peak near the input-gate voltage of 0 V was used for the circuit operation. Just like the original pass-transistor logic used in the MOS-LSI world, the gate inputs are routed in a complementary way. In the present case, they have a voltage amplitude of $V_{IN} = 24$ mV. The pass inputs are also routed in a complementary way for the half-sum, while one of the pass-input terminals was grounded for the carry-out. These pass inputs have a smaller voltage amplitude of $V_{dd} = 4$ mV. The use of the small voltage for the pass inputs is the main feature of the present circuit operations and gives us two merits. One is that we can enjoy the Coulomb blockade effects of the SETs, which is important for maintaining a good ON/OFF ratio of the current characteristics. The other is that a small (smaller than the width of the current peaks) pass-input voltage enables SETs to be ON throughout both the pull-up and pull-down actions, which prevents the signals from deviating from the logic levels, 0 and V_{dd}. As shown in Fig. 7, both half-sum and

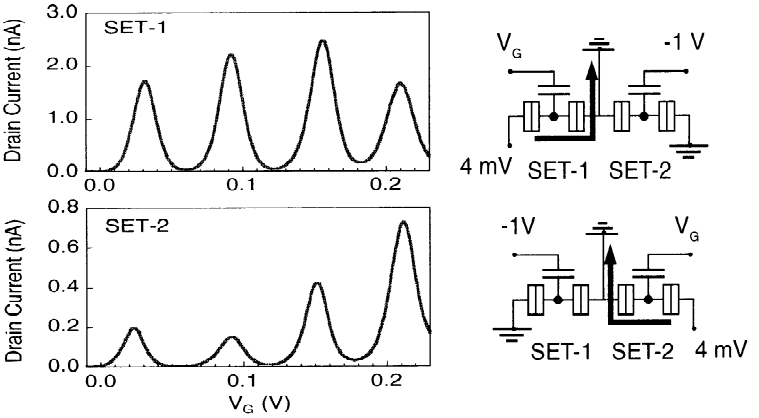

Fig. 6. Current vs. input-gate voltage characteristics of the SETs in the circuit. Each equivalent circuit shows the voltage conditions and the path of the current. Measurement temperature is 25 K.

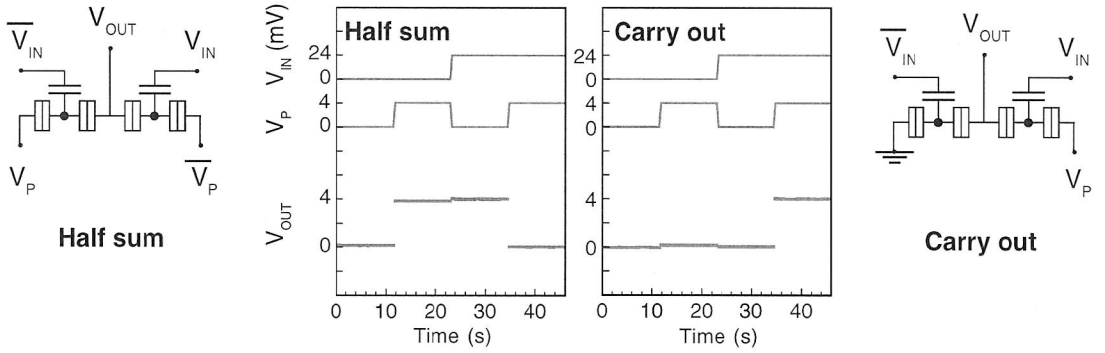

Fig. 7. Experimental demonstration of half-sum and carry-out. V_{IN} and V_P are the input-gate voltage and pass-input voltage, respectively, and V_{OUT} is the output voltage. $\overline{V}_{IN}$ and $\overline{V}_P$ are the inverse of V_{IN} and V_P. Measurement temperature is 25 K.

carry-out are performed with full logic swings. (Notice that although the switching is rather slow, this is not due to the circuit itself, but due to the large capacitance of the measurement system.)

It is obvious that good control of the electrical parameters of the SETs makes the present circuit operation possible. We have also realized a complementary single-electron inverter, in which voltage gain larger than unity was achieved [20].

5. Conclusions

For the fabrication of quantum SOI devices, we believe that control of the oxidation process of nanometer-scaled Si is important. Unique features that arise when it is oxidized, like pattern conversion and band-profile modulation, could lead to the formation of various types of quantum structures with good controllability. The idea has been embodied in a method of fabricating SETs called PADOX, which has made it possible to achieve single-electron circuit operations, including half-sum and carry-out for an adder.

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