Buried Cobalt Silicide Layers in Silicon Created by Wafer Bonding

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ABSTRACT

A buried conductive layer in silicon has been created using wafer bonding technique, with a cobalt interfacial layer. Co-coated silicon wafers were brought into contact with either similar or uncoated wafers at room temperature. $CoSi_2$ was then formed through a solid-phase reaction, during an anneal at 700 to 900°C. A 700 Å buried $CoSi_2$-layer, with a resistivity of approximately 21 μΩ cm, was achieved. Good adhesion, as measured by tensile strength testing, between the wafers was achieved. Transmission electron microscopic investigations (Co-coated wafer bonded to bare silicon) showed that the silicide has not grown into the opposite wafer, and that an amorphous layer exists between the silicide and the silicon surface. The presence of such a layer has been confirmed by electrical characterization.

The possibility of having a conductive layer buried in high quality silicon is of great interest for new device concepts, both in microelectronics and micromechanical applications. Buried layers made by growing $CoSi_2$ epitaxially on silicon has been shown to be useful in fabrication of high frequency devices like the permeable base transistor[1] and the metal base transistor.[2] It may also simplify the manufacturing of complicated ultralarge scale integrated (ULSI) circuits, since the electrical interconnects may be made from both sides of the devices.

With integrated circuit (IC) compatible standard deposition techniques today it is impossible to form a single-crystalline silicon overlay on top of an epitaxial silicide layer. An extensively used process in silicon IC technology is ion implantation, and high energy implantation of Co ions has been shown to be an alternative way of making buried $CoSi_2$-layers.[3,4] However, this technique also suffers from problems with the silicon overgrowth, as the silicon substrate becomes defect-rich, or even amorphized, during high energy implantation. An interesting way to form buried films in a single-crystalline silicon matrix, called allotaxy, recently has been presented by Mantl and Bay.[5] By coevaporation of cobalt and silicon, to varying rates, and a subsequent anneal step, an epitaxial $CoSi_2$ film is created inside the silicon film. However, this is a complicated method, performed in ultrahigh vacuum and demanding exceptionally good control of the deposition rates.

Silicon wafer bonding offers another possibility of creating buried conductive layers in high quality single-crystalline silicon through a relatively uncomplicated process. Bonding silicon wafers, or oxidized silicon wafers, with an intermediate coating of *e.g.*, Ti, Pt, Al, and Ge has been reported earlier.[6-8] Some metals react with silicon, and form a silicide during heat-treatment. In this work, a buried silicide layer has been formed, by bonding of silicon wafers coated with cobalt. During heat-treatment the metal layer and the silicon form cobalt disilicide, $CoSi_2$, through a solid-phase reaction.

Compared to other conductive silicides and metals, $CoSi_2$ has the advantages of both low thin-film resistivity and high thermal stability.[9] The latter is important if further IC processing of the wafers is to be done, *e.g.*, heat-treatments for diffusion or activation of dopants. $CoSi_2$ has been used commonly in the so-called self-aligned silicide (SALICIDE) process, in which the silicide can be used as a diffusion source (SADS).[4]

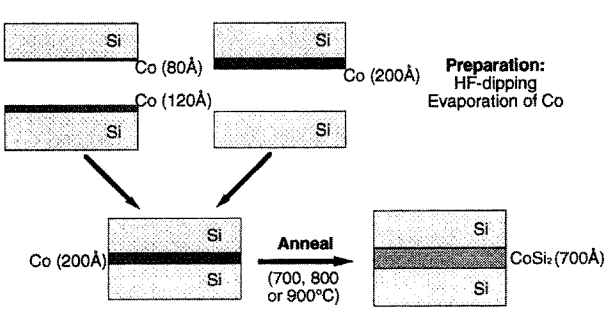

Fig. 1. Schematic diagram of the bonding process steps. Silicon (100) wafers were brought together after evaporation of Co on one or both wafers. The silicide was then formed through a solid-phase reaction by annealing at three different temperatures.

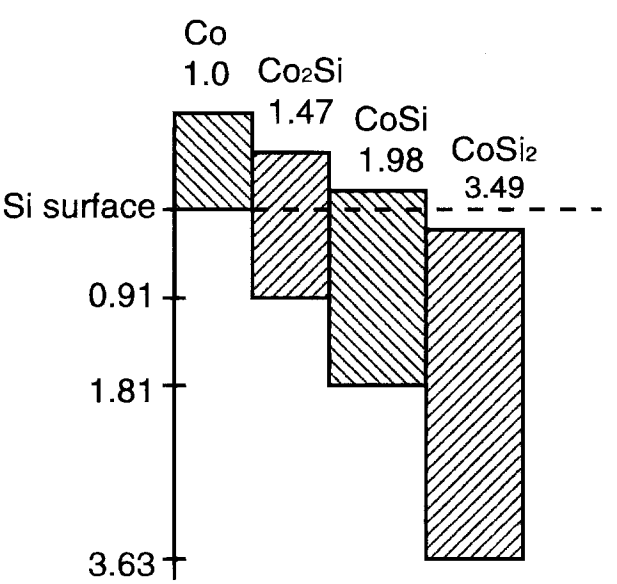

Fig. 2. Expected volumetric changes during the solid-state reaction that forms cobalt silicide from a metal layer, deposited on a silicon substrate. The depth scale, extending into the substrate, shows the amount of silicon consumed. The number given for each phase is the thickness of the formed silicide, as compared to the original metal layer.[4]

Experimental

The silicon used in all experiments were 3 in. wafers (Okmetic n[100], 1 to 10 Ω cm), with a thickness of 390 ± 25 μm. A cobalt film was evaporated on the bare silicon surface, since a native silicon oxide acts as a diffusion barrier for both silicon and cobalt.[4] Immediately before evaporation of Co, the Si wafers were dipped in dilute HF to remove the native oxide and keep the surface oxide-free in air for a reasonably long time. Cobalt was evaporated at a pressure of 5×10^{-8} mbar.

A 200 Å thick Co layer was deposited on surfaces to be bonded to bare silicon surfaces. For bonding of Co to Co, the thickness of the Co layers was 80 to 120 Å. Two Co-coated wafers were then combined to achieve a total thickness of 200 Å on each sample. Figure 1 shows a sketch of the bonding process steps. 200 Å Co, assuming a complete reaction with silicon, results in a 700 Å thick $CoSi_2$ layer. Figure 2 illustrates the expected volumetric changes during the reaction.[4] The solid-state reaction goes through three different silicide phases, as seen in the figure. The metal-rich silicide and the monosilicide begin to grow simultaneously at 350°C, with activation energies of 1.5 and 1.9 eV, respectively.[10] The disilicide begins to form at *ca.* 550°C.[11]

After the samples were brought together in air at room temperature, they were furnace annealed in N_2 ambient at 700, 800, and 900°C for 30 min. Wafers were bonded both with and without a load applied (100 g quartz plate) on the wafer pair during anneal.

Characterization

The following methods were used for characterization of the buried $CoSi_2$-layer.

1. To get an estimation of the bonded area related to the whole wafer area, the bonded wafers were cut into 1 × 1 cm pieces. Depending on the number of separated pieces, a qualitative evaluation of the bond process could be made.

2. Tensile strength testing was done to determine the fracture strength of the bonds. This kind of experiment has been discussed previously.[12] The 1 × 1 cm bonded pieces were glued to aluminum holders, to fit in the grips of the testing machine. A cyano acrylate glue with high fracture strength was used. The samples were then loaded perpendicularly until fracture.

3. Transmission electron microscope (TEM) studies were performed on a bonded sample made with one Co-coated silicon wafer and one bare silicon wafer annealed at 800°C. A cross-sectional sample was prepared using standard techniques.[13] The TEM studies revealed information about the homogeneity and thickness of the silicide layer, the average silicide grain size, the orientation of the silicide layer *vs.* the silicon wafers, and also about the character of the achieved bonding.

4. Samples were etched down to the buried silicide layer from one side, in KOH (40 g in 100 ml H_2O, 80°C). The sheet resistivity of the uncovered silicide layer was then measured using a four-point probe. With knowledge of the silicide layer thickness from the TEM studies, the resistivity could then be calculated.

5. Samples annealed and bonded at 800°C were prepared for electrical characterization of the current transport through the bonded interface. The back sides of the bonded 1 × 1 cm pieces were heavily phosphorus implanted, annealed, and covered with aluminum to get ohmic contact. To minimize leakage current at the edges, the pieces were patterned and etched to form mesa islands. A schematic view of the structure is shown in Fig. 3. Samples from both Co-Si bonded and Co-Co bonded wafers were prepared. The IV characterizations were carried out at room temperature. Ideally, it is expected that two opposite rectifying Schottky diodes are formed against each silicon surface. The IV characteristics should then be symmetrically plotted around the y-axis, showing the reverse leakage current for each diode. The leakage current is mainly determined by the Schottky barrier,[14] which thus can be estimated.

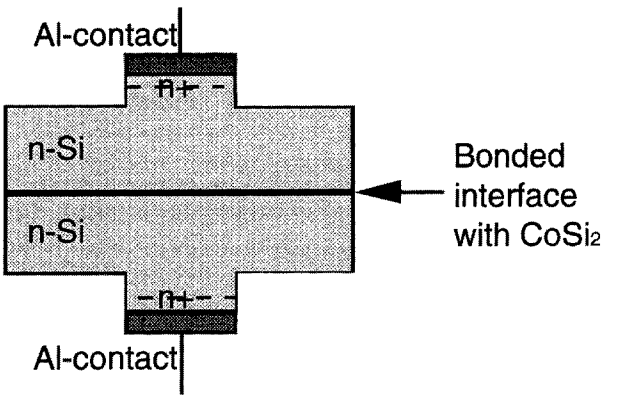

Fig. 3. Schematic view of the bonded structure used for IV characterization. The area of the sample is 1 cm², and the metallized area is 14 mm². Measurements were made for samples annealed at 800°C, with the bonded interface either between the silicide and silicon or inside the silicide layer.

Results

The wafers were found to stick together already at room temperature in a way similar to smooth silicon surfaces.[15,16] This facilitates further handling. However, the wafer pair also could easily be separated from each other again, without the surface being destroyed.

When a load was applied during heat-treatment, bonding was achieved over the whole wafer area. With no load applied during the anneal, only the center parts of the wafers were bonded. This is due to stresses in the film, resulting in a convex curvature of the Co-coated side. These stresses are probably caused by the volumetric changes as well as the differences in thermal expansion coefficients between the silicide phases and the silicon. Only wafers loaded during heat-treatment were characterized further.

A classification of the bonds achieved is summarized in Table I. Both the presence of unbonded areas, as estimated by cutting, and the tensile strength measurements have been parts of this estimation.

When the bonds were characterized, unbonded areas of various sizes were found. Large unbonded areas were detected by cutting the wafers in 1 × 1 cm pieces. Pieces separated to different degrees for all the samples, but in the best cases such poor adhesion was almost entirely located on the wafer periphery. This could be caused by a slight buckling of the wafers as described above, or contaminants from wafer holders, tweezers, etc.

The highest tensile strength was achieved for Co-Si bonded samples annealed at 800°C. Fracture occurred at the glued interface before the bond broke, while only a lower limit for the fracture stress, of 25 MPa, could be obtained. To be able to measure higher values, a reduction of the bond area must be made.[12] For all other samples the bonded interface, or the surrounding silicon, broke before the glue. Fracture strengths between 2.5 and 13 MPa were obtained for these samples.

The TEM studies showed that the silicide layer is continuous and has a relatively homogeneous thickness of 70 nm.

Table I. Classification of the bond quality *vs.* two process parameters, *i.e.*, the surfaces to be bonded (one or both the wafers covered by a Co film) and the annealing temperature.

Bonded surfaces	Anneal 700°C	Anneal 800°C	Anneal 900°C
Co-Si	+	++	+
Co-Co	+	=	=

++ Very successfully bonded, few voids.
+ Successfully bonded, some unbonded areas.
= Partially bonded.

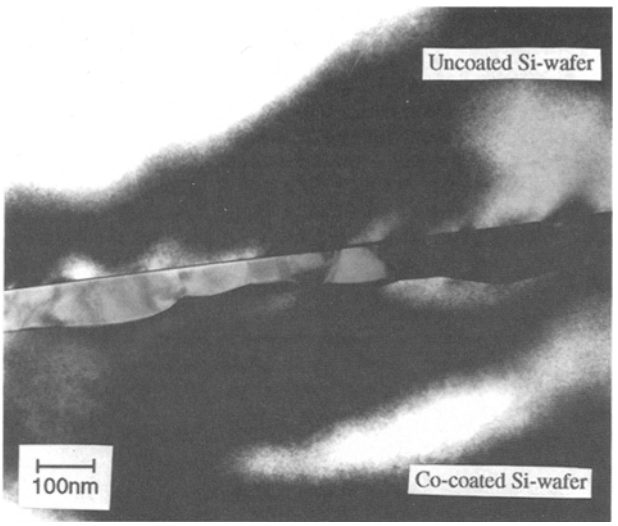

Fig. 4. Cross-sectional TEM image of the silicide layer formed after annealing in 800°C. Bonding of an uncoated wafer against a wafer with a Co film 200 Å thick.

The silicide has an average lateral grain size of 150 to 300 nm (Fig. 4). A few small voids (less than 1 μm) were observed in the silicide layer. These voids extended from the bare silicon wafer and at the most through the silicide layer. Small voids (typically on the order of 20 to 40 nm) were seen at some silicide grain boundaries. Nowhere along the thin region in the TEM sample (200 μm) had the cobalt reacted with the bare silicon wafer and created a bridge of $CoSi_2$. High resolution TEM (HRTEM) shows an amorphous layer which separates the silicide grain from the silicon (Fig. 5). This layer is approximately 30 to 40 Å thick. The morphological changes of the silicide grains has been hindered at the uncoated silicon wafer surface (probably by the amorphous layer) and all the silicon during the solid-phase reactions has been supplied from the coated wafer. This can be seen from the fact that the grains have very flat surfaces facing the bare silicon wafer. No epitaxial relationship was observed between the formed silicide layer and the substrate silicon or the opposite silicon wafer. In the TEM sample, separations (about 20 nm) of the silicide from the bare silicon wafer were seen and were considered to be unbonded areas. Possibly these areas have been weakly bonded before TEM specimen preparation, but released or induced stresses may have caused the separation.

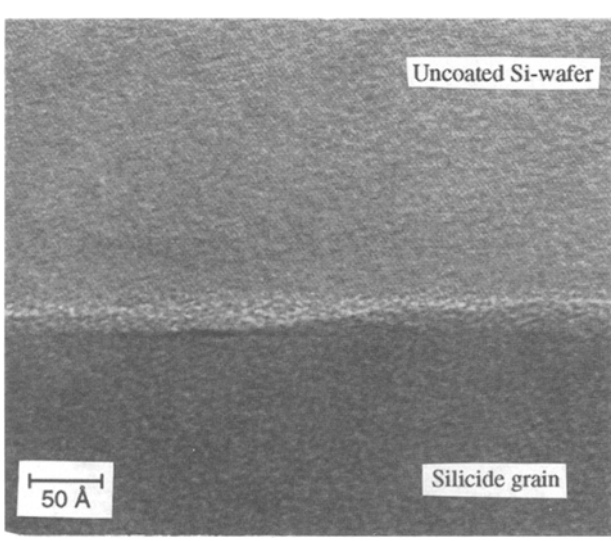

Fig. 5. Cross-sectional HRTEM image of the interface between a favorably oriented silicide grain and the uncoated silicon wafer after annealing at 800°C. An amorphous interfacial film *ca.* 30 to 40 Å can be identified.

For the samples where one of the wafers was etched away, the silicide layer had a sheet resistivity of *ca.* 2.8/sq, in good agreement with earlier reports.[9] With a 700 Å thick layer, according to the above, this corresponds to a resistivity of 21 μΩ cm.

The measured IV characteristics for Co-Co bonded samples are presented in Fig. 6a showing the behavior as expected from two rectifying diodes. Assuming constant current density over the sample area (1 cm^2), and that the leakage current at the edges can be neglected, the leakage corresponds to a barrier height of about 0.63 eV. This is in good agreement with earlier published values for the barrier of cobalt disilicide on n-type silicon.[17]

For Co-Si bonded samples, the IV characteristics have a different appearance. The diode corresponding to the bonded interface is no longer rectifying, as can be seen in Fig. 6b, in the forward direction. The series resistance of this IV curve can be estimated to *ca.* 14 Ω. It should be noted that the series resistance is too large to be explained only by resistance from the bulk silicon, but probably gets an appreciable contribution from the bonded interface. In the reverse direction, corresponding to the diode on the coated side, the characteristic look similar as in Fig. 6a.

Discussion

Silicon wafer bonding in general, and bonding of oxidized wafers to create a silicon-on-insulator (SOI) structure in particular, attracts increasing attention in microelectronics and micromechanics. Today, void-free bonded SOI wafers with high flexibility in silicon film thicknesses are commercial products.[18,19] Recently, it has been shown that nearly void-free silicon-silicon bonds, with high bond strengths, can be achieved.[15,16] In combination with the results of silicon-silicide bonding, this makes several new device applications feasible. Novel 3D devices, buried conducting layers, or new transistor concepts[1,2] are a few examples. Buried interconnects and methods for joining different materials are also interesting for fabrication of micromechanical complex systems, *e.g.*, in equipment, practice for opto- and microelectronics. The above results show that silicon-silicide bonding is one promising step on the way to reach the goal of a complete setup for bonding different materials: insulators, semiconductors, and conductors.

The main problem in the experiments described here is the presence of unbonded areas or voids. Explanations include trapped particles, contamination, or irregularities in the evaporated film. Film stresses causing wafer buckling which reduce the contact areas, may be an additional problem. In Table I, where the classification of the bond qualities of the different samples is given, a tendency can be seen that the bond quality of the Co-Co samples is lower than for the Co-Si samples. One explanation of this may be that in the first case two evaporated surfaces are involved, which should make problems such as roughness and particle contamination worse. Oxidation of the Co film is another problem that may cause lower adhesion, especially when Co is bonded to Co. The oxide probably prevents interaction between the two metal layers during the anneal, and so the bond strength is limited by the surface adhesion between the two oxide surfaces.

No reaction between the silicide on one wafer and the other silicon surface has been found in the TEM sample, but the strain contrast phenomena (submicrometer buckling) along the interface indicates that there is a continuous bonding in the interfacial layer. The amorphous interfacial layer, found in the TEM studies (Fig. 5), between the bare silicon wafer and the silicide layer is most likely an oxide. This suggests that bonding has occurred between this oxide and the opposite surface. An amorphous oxide acting as a diffusion barrier is consistent with the observation that there has been no reaction between the silicide and the uncoated silicon. An amorphous film possibly may be a specimen preparation artifact due to ion-beam thinning. A thin unbonded slit may be filled with sputtered material

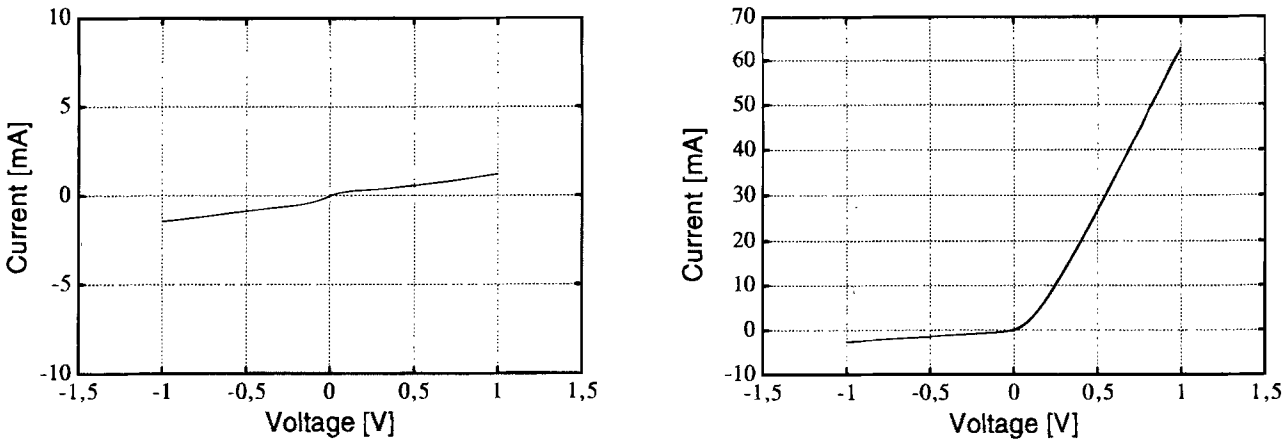

Fig. 6 (a, left) IV characteristics for a Co-Co bonded (800°C anneal) sample, *i.e.*, where the bonded interface is located inside the buried silicide layer. (b, right) IV characteristics for a Co-Si bonded (800°C anneal) sample, *i.e.*, where the bonded interface is located between the silicide layer and the opposite silicon surface.

during the thinning process. However, the same silicide morphology is observed at the thicker parts of the specimen; this strongly supports that the amorphous layer (diffusion barrier) existed between the silicide and silicon before the specimen preparation.

Cobalt almost immediately forms a thin protective oxide in air. Since the wafers must be brought together in air after evaporation, an oxide layer in the bonding interface is likely. For this system of Co, O, and Si, the thermodynamically most stable phase (up to at least 1000°C) is SiO_x. Hence, the Co oxide is probably transformed to SiO_x during the anneal, and could constitute an adhering film between the wafers. Co oxide normally crystallizes in an NaCl structure. This also supports that a transformation to SiO_x has occurred, since the observed intermediate film is amorphous.

The tensile strength tests show that the bonds are strong enough to ensure that the wafer package can be handled and processed further. It is difficult to get an accurate quantitative value, as there are many errors involved in the method. Besides problems with alignment in obtaining an ideal tensile test of a brittle material, the fracture stress values in these tests are determined by the geometry of the interface at the edges. Unbonded regions at edges strongly reduce the fracture strength. Nevertheless, the tests give valuable information about the quality of the bond for further processing. A fracture stress better than a high qualitative glue, 25 MPa, is sufficient for many applications. As a comparison, values between 25 and 50 MPa have been reported for bonding Si to Pyrex glass,[12] and 2 to 20 MPa for Si-SiO_2-bonding.[20]

The results from the IV characterization of different samples clearly show how the current is influenced by the bonded interface. For samples where Co was evaporated on both wafers, thereby placing the bonding interface inside the $CoSi_2$-layer, good Schottky diodes were created in both directions. From the leakage current, the barrier was estimated to 0.63 eV, which corresponds well with earlier values.[17] However, when the bonded interface was located between the silicide and the silicon, no such Schottky diode behavior in both directions was observed. Instead, the bonded junction is more like that of an ohmic contact between the silicon and the silicide. The total series resistance is also 3 to 5 times higher than the series resistance originating from the bulk silicon. This can be explained by the thin amorphous layer between the silicon and the silicide observed in the TEM investigation. Assuming that this layer consists of SiO_x, with poor insulating properties and high concentration of traps, an ohmic current transport can be permitted even if the work functions in the silicon and the silicide are different.[21] An estimation of the contribution from the bonded interface to the total resistance, is difficult to make for these samples, since there is a dependence on the amount of unbonded areas. Additional errors can be expected from the approximation of a constant current density.

Increasing the bond quality certainly should be possible, if the cobalt oxide is eliminated. In that case, a silicidation across the bonded interface may be achieved. To find ways of eliminating the oxide, or preventing its formation, as well as minimizing any other factors that may cause unbonded areas of voids, our our most important goals in future work on this project.

Conclusion

Buried conductive layers of $CoSi_2$ have been achieved in silicon by using wafer bonding technique with evaporated cobalt on one or both the silicon wafers as an intermediate layer between the silicon surfaces to be bonded. During the subsequent anneal a 700 to 900°C, metal and silicon form a stable silicide buried between the silicon wafers. The bond strength of the wafers were between 2.5 and 25 MPa, as measured by tensile strength testing Unbonded areas of various sizes reduce the mechanical strength and also affect the electrical properties of the bond. The bond strengths obtained however are believed sufficient for many applications.

TEM investigations of the silicide layer obtained at 800°C (Co bonded to Si) showed a uniform silicide film thickness of 70 nm and an average lateral grain size of 150 to 300 nm. As far as can be seen, the grains have not grown into the opposite wafer. In HRTEM a 30 to 40 Å amorphous layer, assumed to be SiO_x, was detected between the silicide and the silicon.

Electrical characterization of the silicide layer gave a resistivity of 21 $\mu\Omega$ cm for the buried silicide layer. IV characterization shows that in Co-Co bonded wafers the structure behaves as two opposite Schottky diodes. The Schottky barrier height was estimated to 0.63 eV. In Co-Si bonded wafers, the characteristic at the bonded interface shows an ohmic behavior, which can be referred to the thin amorphous layer observed in the TEM study.

Silicon wafer bonding is a promising technique for creating buried conductive layers in single-crystalline silicon due to its simplicity and the ability to keep the high quality bulk silicon. Many possibilities arise from this both in IC technology and micromechanics.

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