Standard Cell Library Design with Voltage Scaling and Transistor Sizing for Ultra-Low-Power Biomedical Applications

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***Abstract*—This paper reports the design and optimization of a standard cell library in 0.18μm CMOS, together with the analysis on voltage scaling and transistor sizing for ultra-low power biomedical applications. By simulating with a 8-bit 4-tap FIR filter at 0.6V clocked 100kHz, the design achieves 18.6× and 1.55× lower power consumption comparing to a commercial standard cell library working at nominal voltage 1.8V and re-characterized 0.6V.**

I. Introduction

Ultra-low power electronic is important especially for biomedical and portable applications for prolonging battery life. For lowering power consumption in digital circuits, designs can be migrated to advanced technologies to profit from technology scaling. In the algorithm and architecture level, designers can reduce the system computation workload and improve the architecture/microarchitecture for power optimization. In the circuit level, optimizing the standard cell library (SCL) can reduce the system power consumption. The SCL is a set of fundamental building blocks for digital VLSI, including the logic blocks (e.g. AND, OR, NOT), storage blocks (e.g. flip-flop) and physical assistances (e.g. buffer, Tie-High, Tie-Low, End-Cap), etc. Cell-based design flow can be adopted to automate the schematic and layout designs with SCL and VLSI Computer-Aided Design (CAD) tools [1], [2].

For power optimization of digital VLSI, this paper reports the optimization of a SCL, with the analysis on voltage scaling and transistor sizing for searching the power-efficient supply voltage and for tuning the driving capability and the input/parasitic capacitances, respectively. The linear timing model and logic effort methodology are adopted in standard cell power and timing optimization. The custom SCL ($V_{DD} = 0.6V$) is compared to a benchmark commercial SCL (nominal $V_{DD} = 1.8V$) with a FIR filter clocked at 100kHz, showing a 18.6× power reduction. After re-characterizing the commercial SCL to 0.6V, the custom SCL still shows a $1.55\times$ power reduction in the FIR filter.

II. Basic Principal and Analysis

A. Sources of Power Dissipation

The source of power dissipation consists of dynamic power and static power. Dynamic power is due to charging and discharging load capacitances as gate switches, and short-circuit current when both PMOS and NMOS stacks are partially ON. It consists mostly of the switching power, given in Eq.(2). The static power is due to leakage current through OFF transistors, gate leakage through dielectric, junction leakage from source/drain diffusions and contention current in ratioed circuits. The static power is modeled in Eq.(3)

$$P_{Total} = P_{Dynamic} + P_{Static} \tag{1}$$

$$P_{Dynamic} \approx P_{switching} = \alpha C V_{DD}^2 f \tag{2}$$

$$P_{Leak} = W_{eff} I_{leak} V_{DD} \tag{3}$$

So dynamic power $P_{Dynamic}$ is proportional to operating frequency f, total loading capacitances C, square of the supply voltage V_{DD}, activity factor α which is the percentage of switching in clock cycles. Static power is proportioinal to the supply voltage V_{DD}, the total width contributing to leakage current W_{eff}, the leakage current of a characteristic inverter I_{leak}.

B. Voltage Scaling

As shown in Eq.(2) and Eq.(3), the supply voltage is quadratically related to the dynamic power and linearly to the static power. Voltage scaling is a predominant way in lowering the total power of the digital VLSI.

As shown in Eq.(4), the drain current of a transistor in saturation region is proportional to the over-drive voltage $V_{GS} - V_{TH}$. In Eq.(5), the drain current of a transistor in subthreshold region is exponentially proportional to $V_{GS} - V_{TH}$. The drain current is for charging and discharging the load/parasitic capacitors for changing the voltage levels. Thus for digital VLSI, the supply voltage also impacts the circuit delay.

$$I_D = \frac{1}{2}\mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{4}$$

$$I_{D_{sub}} = I_0 e^{\left(\frac{V_{GS} - V_{TH} + \eta V_{DS}}{n V_T}\right)} (1 - e^{\frac{-V_{DS}}{V_T}}) \tag{5}$$

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) V_T^2 \tag{6}$$

where μ_0 is the surface mobility, C_{ox} is the capacitance of unit area of oxide, $\mu_0 \cdot C_{ox}$ is the intrinsic transconductance, I_0 is the nominal current, n is the subthreshold slope factor, V_T is the thermal voltage, and η is the Drain-Induced-Barrier-Lower coefficient. Simulating a NMOS transistor (W=$0.46\mu m$, L=$0.18\mu m$, $V_{TH} = 0.479V$, in a $0.18\mu m$ technology) shows that the drain current drops exponentially when $V_{GS} < V_{TH}$.

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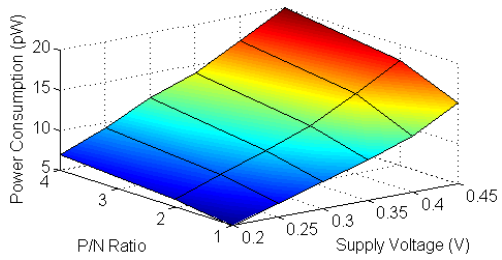

Fig. 1. Power Consumption vs P/N Ratio vs Supply Voltage of Inverter Chain in $0.18\mu m$ CMOS clocked at 250MHz.

C. Transistor Sizing

Transistor sizing should consider the mobility difference of PMOS and NMOS for balancing the rise and fall. Note that increasing the size of transistors not only improves the driving capability, but also increases the input capacitance which is the loading of the preceding cell. As shown in Eq.(7), the gate capacitance C_g is proportional to the gate area WL. So the L is usually sized smallest to minimize capacitance. The logic effort method can be chosen for the transistor sizing [3].

$$C_g = C_{ox} W L \tag{7}$$

III. Low Power Standard Cell Library Design

The logical effort design methodology, which is based on a model that gate delay is a linear function to gate load capacitance, is adopted to estimate and optimize the gate delay [1], [3]. The gate delay (d) is modeled as $d = gh + p$, where p is the parasitic delay, gh is the effort delay, g is the logic effort and h is the electrical effort. The characteristic inverter is first sized, followed by the other gates with stacking transistors accordingly. For example, the 3-stack series NMOS transistor path can be regarded with $3\times$ resistance, so the transistor width should be sized $3\times$ to compensate for it. The 3-parallel PMOS transistor should be sized for worst case that only a PMOS is ON, and the path should be with the same resistance. The length of transistors are sized minimum for lowering the capacitance. As shown in Fig.1, the power of various ratios of PMOS width to NMOS width is simulated with an 7-stage inverter chain running at 250MHz. It shows the 1:1 P/N ratio with the lowest power. The voltage transfer curve (VTC) of 1:1 P/N ratio inverter with fanout-of-4 is shown in Fig.2.

The design of the standard cell library has undergone several steps with transistor sizing of inverter, design corner simulations, other logical cells design with logical effort methodology [3], cell layout, Design Rule Check, Layout vs. Schematic check, and cell characterization for CAD tools. Tie-High and Tie-Low cells are designed for providing constant '1' and '0' internal signals. Level shifter is also designed for converting signals to the 1.8V voltage level.

IV. Result and Conclusion

Two versions of a 8-bit 4-tap direct form FIR filter are implemented with the custom library and a commercial library for comparison. The power consumptions of the FIR filter running at 100kHz are listed in Table.I. From the table we can see that the custom SCL consumes less power than the commercial library in all the four operating voltages, benefited from the smaller transistor sizes and smaller capacitances.

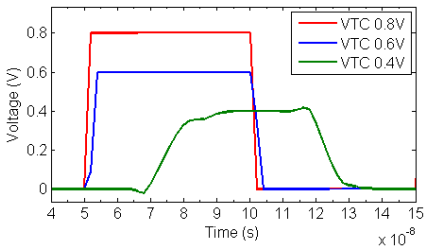

Fig. 2. VTC of Inverter with 1:1 P/N Ratio and Fanout-of-4

TABLE I
Power Consumption of FIR Filter Implemented with Custom SCL and a Commercial SCL.

Lib.	Volt. (V)	Cell No.	Area (μm^2)	Leakage (nW)	Dynamic (nW)	Total (nW)
Custom	1.8	214	8859	11.036	60187.78	60198.82
Custom	1.2	215	8850	5.17	13498.42	13503.59
Custom	0.6	652	17606	3.653	4833.11	4836.76
Custom	0.45	1796	35017	4.719	7013.98	7018.69
Comm'l	1.8	216	8310	16.259	90199.86	90216.12
Comm'l	1.2	216	8332	7.857	21872.25	21880.11
Comm'l	0.6	620	15677	4.922	7533.12	7538.05
Comm'l	0.45	1276	25367	4.922	7533.12	7538.04

The cell count and cell area dramatically increase in both libraries when operating in 0.6V and 0.45V. This is because the VLSI CAD tool automatically inserts buffers between registers to fix the hold time violations. The insertion of buffers is costly making both the static power and dynamic power increase. When the buffer insertion becomes serious, the power consumption of buffers overcomes the saving of a lower supply voltage. Thus the lowest-power supply voltage is 0.6V in this case. The power is $90216.12/4836.76 = 18.6\times$ lower by using the custom SCL at 0.6V to the commercial SCL at nominal voltage 1.8V. By re-characterizing/simulating the commercial SCL at 0.6V, the power of the custom SCL is still $7538.5/4836.76 = 1.55\times$ lower.

Voltage scaling affects power consumption largely, while transistor sizing can tune the driving capability and loading capacitance for reducing power. The custom SCL in 0.6V lowers the power by $18.6\times$ and $1.55\times$ comparing to a commercial SCL working in nominal 1.8V and re-characterized 0.6V.

V. Acknowledgement

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