Kinetics of the Slow-Trapping Instability at the Si/SiO_2 Interface

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ABSTRACT

The slow-trapping instability can be a potentially major threat to reliability of p-channel enhancement-mode IGFET's. We have determined the kinetics of slow trapping for Al-gate MOS structures on (111) n-Si and evaluated the role of surface states, N_{SS}, for n- and p-type Si of (111) and (100) orientation. Slow trapping, as revealed by negative bias-temperature aging, generates a characteristic distribution of N_{SS} with a peak near the midgap. This effect is responsible for the fact that for n-Si, the threshold shift, $\Delta V_T >> \Delta V_{FB}$, the flatband shift, and for p-Si, $\Delta V_T < \Delta V_{FB}$. In the regime where ΔV_{FB} is less than the saturation value, our data on slow-trapping kinetics can be represented by the factorial relationship

$$\Delta V_{FB} \sim A|V_B|^n t^{0.2} \exp\left(-\frac{\epsilon_a}{kT}\right)$$

where V_B is the applied negative bias (10-40V), t is the time (10-10^3 min), T is the temperature (373°-573°K), k is the Boltzmann constant, $n = 4.76 - 5.3 \times 10^{-3}T$, $A \sim 1.6 \times 10^3$, and ϵ_a is the thermal activation energy (~0.64 eV). This equation emphasizes the strong field dependence of ΔV_{FB} at lower temperatures.

The so-called slow-trapping instability [instability No. VI of XVII compiled by Deal (1)] can be a potentially major threat to reliability of p-channel enhancement mode IGFET devices (1-4). This instability is revealed by a negative bias-temperature aging test which causes a negative shift in the flatband voltage and hence in the threshold voltage of the device. The exact mechanism of slow trapping has not been established. But it is known that slow trapping is more pronounced for MOS structures with a high fixed charge, Q_{SS} (4). Slow-trapping instability can be also aggravated by radiation damage (5) and by a low temperature post Al-metallization H_2 anneal (6).

Accelerated aging tests are commonly used to compare the slow-trapping characteristics of different MOS structures and also to evaluate the effectivity of various processing improvements [such as high temperature H_2 annealing (6)] aimed at reducing the slow trapping. However, a knowledge of kinetics is also obviously necessary in order to estimate the lifetime under device operating conditions and to stimulate work on understanding of slow-trapping phenomena.

The objective of the present work is twofold. First, the role of surface states, N_{SS}, was investigated in the slow-trapping phenomena. It is shown that a characteristic distribution of N_{SS} is generated as a result of slow trapping, and depending upon whether the Si is n- or p-type, the flatband shift ΔV_{FB} can be less than or greater than ΔV_T. Second, detailed kinetics measurements were made of slow trapping in Al/SiO_2/(111) n-Si capacitors. The effect of applied bias (for a given time and at lower temperatures) is found to be more severe than previously believed.

Experimental

Slow-trapping measurements were made on both n- and p-type Si wafers [(111 and 100) orientation, 2 in. diam, $N_{D,A} \sim 10^{15}$ cm^{-3}]. The wafers were cleaned and then oxidized to 1000Å thickness at 1100°C in a dry oxygen ambient in an HCl-cleaned quartz tube. The oxidized wafers received an *in situ* Ar-anneal at 1100 C for ½ hr. An array of MOS capacitors was fabricated by filament evaporating Al-field plates (20 mil diam) through a mechanical shadow mask. The SiO_2 was etched off from the back side and an Al back contact was formed also by filament evaporation. The samples were then H_2-baked at 450°C, ½ hr.

MOS measurements were made in a test facility consisting of an electroglas 910 prober equipped with a Temptronix TP 35 thermochuck and enclosed in a dry N_2 glove box (7). High frequency (1 MHz) C-V measurements were made at a sweep rate of 100 mV/sec. Quasistatic measurements were made at 20 mV/sec using the slow-ramp technique (8). The data were analyzed in the usual manner to give the Si-doping level (9), the flatband capacitance and voltage, the oxide fixed charge Q_{SS}, and the surface-state density as a function of the relative surface potential, ψ_S. The surface-state density was obtained from the high-low frequency capacitance technique (10) and ψ_S found as a function of bias using the Berglund techniques (11).

The extent of slow trapping was evaluated through measurements of negative shift in the flatband voltage, ΔV_{FB}, following bias-temperature aging at various temperatures in the range 100°-300°C, with applied negative bias of 10-40V, and for times of 10 min-16 hr.

Results and Discussion

Positive bias-temperature aging under conditions (10^5 V/cm, 200°C, 30 min) where slow trapping is very small caused little or no negative shift (<0.1V) in the C-V curves, signifying that the mobile charge contamination levels were below 2×10^{10} cm^{-2}.

Representative C-V curves.—Figure 1 shows typical C-V curves for a MOS structure on (111) n-Si in the as-received condition and after B-T aging at −23.5V, 250°C, for 15 min. The as-received sample had a Q_{ss} of 2×10^{11} cm^{-2} and a midgap N_{SS} of $\sim 5 \times 10^{10}$ cm^{-2} eV^{-1}. Upon negative B-T aging, the slow trapping is revealed in three ways: (*i*) the high frequency C-V curve is shifted to more negative values reflecting an increase in the apparent Q_{SS} and a ΔV_{FB} of −0.8V; (*ii*) the initially single minimum in the quasistatic C-V curve is split into two minima which now occur at significantly higher C/C_{ox}; this higher C/C_{ox} is the result of an order of magnitude increase in the N_{SS} which has a peak near the midgap, as shown in Fig. 2; (*iii*) there is an increase (by ~1.5V) in the negative threshold voltage from V_{T1} to V_{T2}, as indicated by the vertical

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Key words: MOS devices, reliability, surface states.

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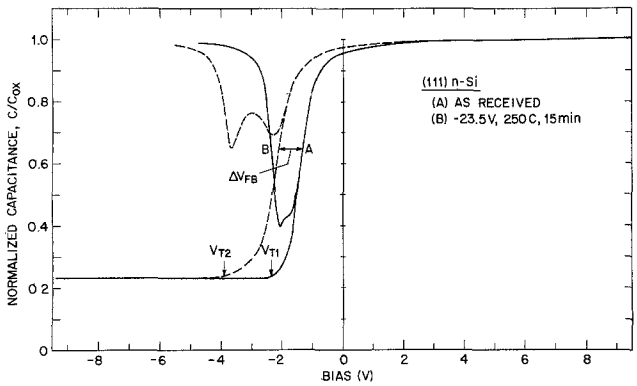

Fig. 1. C-V curves for Al/SiO$_2$/n(111)Si capacitors: (A) as-received; (B) after —23.5V, 250°C, 15 min bias-temperature aging.

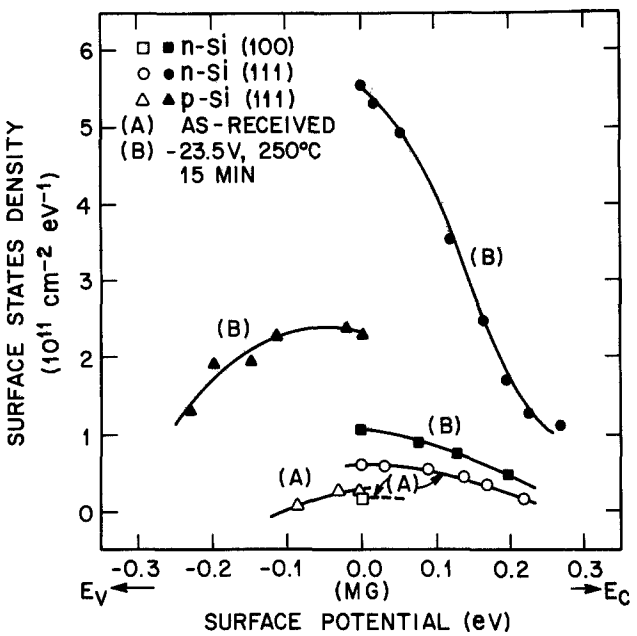

Fig. 2. Distribution of surface states in various Al/SiO$_2$/Si structures: (A) as-received; (B) after —23.5V, 250°C, 15 min B-T aging.

arrows in Fig. 1, with $\Delta V_T >> \Delta V_{FB}$. This is due to the fact that increases in both Q_{SS} and N_{SS} due to slow trapping with n-Si cause threshold shifts in the same direction, which are therefore additive. Moreover, for n-Si, there are fewer occupied surface states at V_T than at flatband voltage. For p-Si, there are more occupied states at T than at flatbands.

Figure 3 shows the effects of slow trapping in an Al-gate MOS structure on (111) p-Si. Here too there is a negative shift in the flatband voltage, ΔV_{FB}, which is nearly equal in magnitude to that observed with (111) n-Si. There is also a significant increase in N_{SS} and a tendency toward splitting of the minimum in the quasistatic C-V curve. However, in this case, ΔV_T is much smaller than ΔV_{FB}, since the apparent ΔV_T components due to additional Q_{SS} and N_{SS} now are in opposite directions. The distribution of $N_{SS}(\psi_S)$ for the (111) p-Si sample before and after B-T aging is shown in Fig. 2 and is similar to that for (111) n-Si.

Figure 4 shows C-V data for (100) n-Si before and after B-T aging. The magnitudes of both ΔV_{FB} and ΔV_T are smaller by a factor of four than those for (111) n-Si. It should be also noted that the initial Q_{SS} ($\lesssim 10^{10}$ cm^{-2}) and N_{SS} at midgap ($\sim 10^9$ cm^{-2} eV^{-1}, see Fig. 2) for this sample were lower by an order of magnitude when compared with (111) n-Si.

This and other recent work support the conclusion that the initial Q_{SS} may be a major factor controlling the slow-trapping instability—a small Q_{SS} correlates with reduced slow trapping. For (111) n-Si samples, the Q_{SS} can be decreased to $\lesssim 1 \times 10^{11}$ cm^{-2} by a high temperature H_2 anneal (800°-900°C, ½-1 hr). These samples show a very small ΔV_{FB} of ~0.2V after 250°C, —20V, 15 min aging. On the other hand, a low temperature H_2 anneal (450°C, ½ hr), which lowers the N_{SS}, tends to enhance the slow-trapping instability (6).

Kinetics data.—Kinetics measurements were made for (111) n-Si samples which had received the post-Al H_2-bake (450°C, ½ hr) but no high temperature H_2 anneal. The ΔV_{FB} was measured for various conditions of negative-bias temperature aging in which two of the three variables, namely, time, temperature, and bias, were kept constant and the third one was changed.

Figure 5 shows the effect of applied bias V_B on ΔV_{FB} induced by slow trapping. Results are shown for various temperatures (80°, 150°, 200°, 250°, and 300°C) for a fixed time of 15 min and for bias voltages ranging from —4 to —80V. [Although bias voltages are quoted in this paper, it should be understood that the field across the oxide and not the voltage is the parameter that determines ΔV_{FB} for various oxide thicknesses (4).] At a given temperature, ΔV_{FB} is a strong function of V_B, with

$$\frac{\partial \log (\Delta V_{FB})}{\partial \log |V_B|} \approx n \qquad [1]$$

where the exponent n ($1.5 < n < 3.2$) is an inverse function of the aging temperature T (°K), as shown in Fig. 6. According to this figure, n will approach unity around 400°C, at which temperature ΔV_{FB} will be a simple linear function of V_B. This is the form of ΔV_{FB} (V_B) relationship reported by Deal *et al.* (4) who plotted the maximum flatband shift measured at ~400°C. At this temperature, saturation in ΔV_{FB} is reached in a relatively short time of few minutes. For the temperatures used in the present work, 15 min was too short a time to reach saturation or steady-state

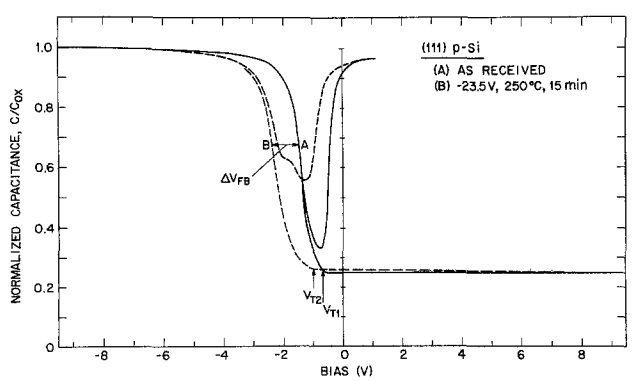

Fig. 3. C-V curves for Al/SiO$_2$/p(111)Si capacitors: (A) as-received; (B) after —23.5V, 250°C, 15 min B-T aging.

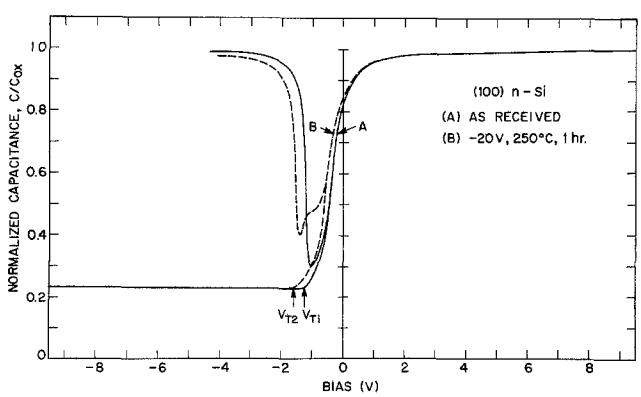

Fig. 4. C-V curves for Al/SiO$_2$/n(100)Si capacitors: (A) as-received; (B) after —23.5V, 250°C, 15 min B-T aging.

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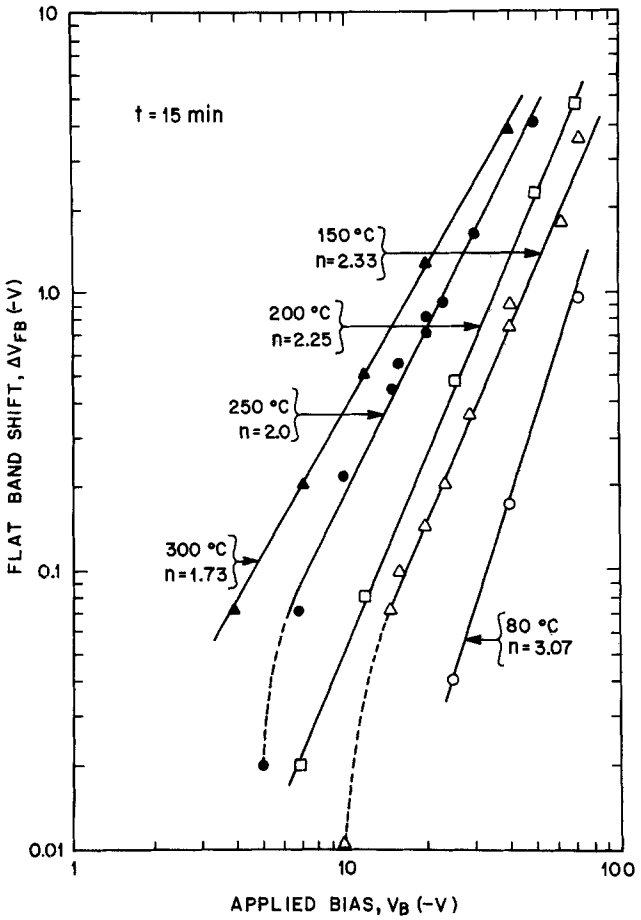

Fig. 5. Variation of slow-trapping induced flatband shift with applied bias at different temperatures, and for times of 15 min.

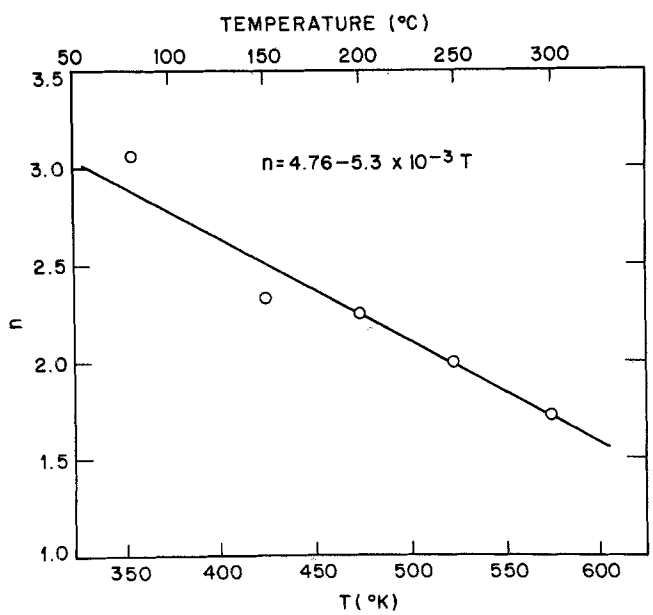

Fig. 6. Temperature dependence of exponent n in Fig. 5

conditions, yet it was adequate to reveal a ΔV_{FB} of 0.1-5V provided the bias fields were large enough.

The nonsteady-state conditions investigated in the present work were preferred because they were convenient and also because they correspond more closely to the device behavior during its operation. Thus, slow-trapping shifts usually cause the device threshold voltage to go out of specification long before the saturation value has been attained.

Figure 7 shows the variation with time of ΔV_{FB} at various temperatures, keeping V_B constant at -20V. It

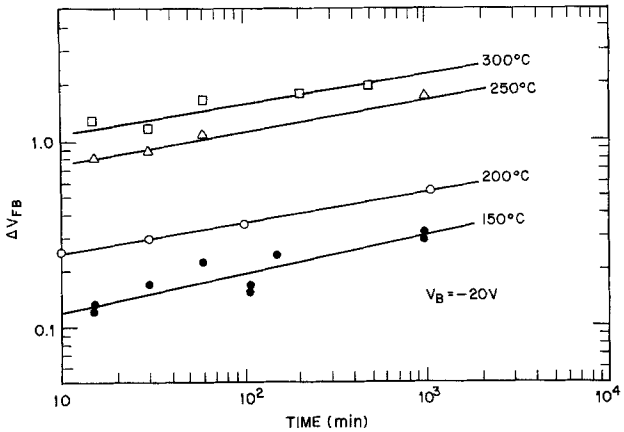

Fig. 7. Time dependence of flatband shift due to slow trapping at various temperatures and for an applied bias of −20V.

may be seen that a substantial portion of the slow trapping shift is revealed in 15 min; however, there continue to be additional shifts with increasing time. For the present samples, the time dependence ($t > 10$ min) was relatively weak, with

$$\frac{\partial \log \Delta V_{FB}}{\partial \log t} \approx 0.2 \qquad [2]$$

This form of time dependence again relates to ΔV_{FB} data below the saturation value.

Figure 8 shows an Arrhenius plot in which ΔV_{FB} has been normalized with $|V_B|^n$ and $t^{0.2}$. A remarkably good fit is obtained for the present set of samples, giving an apparent thermal activation energy of ~0.64 eV. Also shown in Fig. 8 are certain results taken from the work by Broydo and Waggener (12). The combined data show a relatively large degree of scatter, indicating that the slow-trapping kinetics are also a sensitive function of the starting material and that

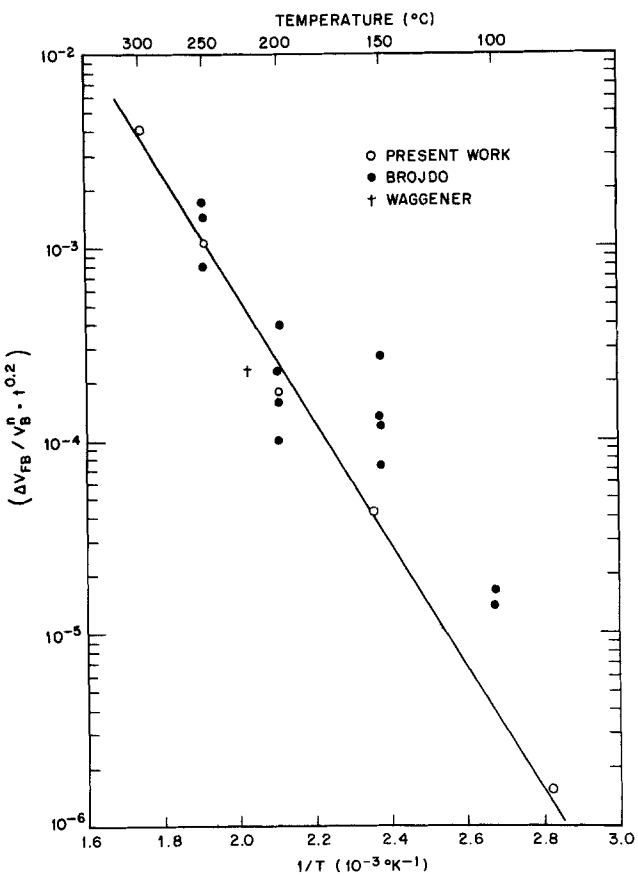

Fig. 8. Arrhenius plot of normalized ΔV_{FB} due to slow trapping

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it may not yet be possible to provide a universal equation for ΔV_{FB}.

Results in Fig. 8 for the present samples (a single lot of six wafers) do indicate, however, that it is possible to rationalize over 30 measurements of ΔV_{FB} in terms of the following simple factorial relationship

$$\Delta V_{FB} = A|V_B|^{n(T)}t^{0.2}\exp\left(-\frac{\epsilon_a}{kT}\right) \qquad [3]$$

where, $A = 1.576 \times 10^3$, $\epsilon_a = 0.64$ eV, $n = 4.76 - 5.3 \times 10^{-3}T$. Equation [3] contains only a single thermal activation energy term and it gives proper weight to the effects of applied bias and time. As noted earlier, the above functional dependence is valid only for ΔV_{FB} values prior to saturation.

The theoretical implications of Eq. [3] are not clear. We believe that the present results lend some support to the model of Deal (1), namely that slow trapping is caused by field-temperature induced structural rearrangements at the Si/SiO_2 interface. In Deal's model (1), a displaced oxygen atom which would otherwise bridge two Si atoms at the interface can simultaneously lead to a positive charge in the oxide and a surface state (dangling bond) in the Si. The ease of such a displacement would depend on the microstrain initially present in the Si-O bond at the interface. It is conceivable that the interfacial strain is related to the magnitude and screening distance of the fixed charge (excess Si atoms?) always present at the SiO_2/Si interface. It appears that this (compressive) strain also provides the driving force for slow trapping. The roles of temperature and applied field in causing dissociation of strained O-Si bonds appear to be complementary. Thus, as the temperature gets smaller, V_B tends to have a more pronounced effect on ΔV_{FB}.

Summary and Conclusions

The slow-trapping instability has been investigated for n- and p-type (111) Si and for n-type (100) Si.

1. For well-annealed MOS structures, negative bias-temperature aging causes a characteristic splitting of the quasistatic C-V curve; the resulting N_{SS} has a peak near the midgap. This N_{SS} effect is responsible for the fact that for n-Si, $\Delta V_T > \Delta V_{FB}$ whereas for p-Si, $\Delta V_T < \Delta V_{FB}$.
2. For a given time and temperature and ΔV_{FB} less than the saturation value, ΔV_{FB} increases with the applied field. The field dependence gets stronger at lower temperatures.
3. For a given field and temperature, and time greater than 10 min, there is a relatively slow variation ΔV_{FB} with time.
4. For a given set of identical samples, it is possible to normalize ΔV_{FB} with respect to the applied bias and time, the resulting temperature dependence yields a single-valued activation energy equal to 0.64 eV for the presently studied $Al/SiO_2/n(111)Si$ structures.

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Two-Layer Model for Heat-Treated Anodic Tantalum Oxide

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ABSTRACT

The dielectric properties of Ta_2O_5 thin films, grown anodically in a phosphoric acid solution and subjected to heat-treatment, have been investigated as a function of frequency in the range 0.1-100 kHz and temperatures from $-100°$ to 300°C. The experimental evolution of tan δ and series capacitance with the frequency and temperature is reproduced theoretically assuming that the anodic oxide has two layers with a different exponential conductivity gradient. The imaginary part of the dielectric constant shows a relaxation process of the Maxwell-Wagner type, which is also explained by the above model for the oxide.

In the manufacture of tantalum capacitors the anodic oxide is normally subjected to temperatures above 200°C in the process of the pyrolytic deposition of the manganese oxide solid electrolyte. The dielectric properties of the resulting oxide have been thoroughly investigated by Smyth *et al.* (1), who reached the conclusion that a gradient in the electrical conductivity

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Key words: dielectric properties, Maxwell-Wagner model, tantalum capacitors, heat-treatment in anodic oxides.

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