Nat.Lab. Unclassified Report NL-UR 2001/813

Date of issue: April 2001

MOS Model 11

Level 1100, Test Version

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Unclassified Report

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Unclassified Report: NL-UR 2001/813

Title: MOS Model 11
Level 1100, Test Version

Author(s): R. van Langevelde

Part of project: Compact modelling

Customer: Philips Semiconductors

Keywords: MOS Model 11, compact modelling, MOSFET, CMOS, circuit simulation, integrated circuits

Abstract: A new compact model for MOS transistors has been developed, MOS Model 11 (MM11), the successor of MOS Model 9. MM11 not only gives an accurate description of charges and currents and their first-order derivatives (transconductance, conductance, capacitances), but also of their higher-order derivatives. In other words it gives an accurate description of MOSFET distortion behaviour, and as such MM11 is suitable for digital, analog as well as RF circuit design.

MOS Model 11 is a symmetrical, surface-potential-based model. It includes an accurate description of all physical effects important for modern and future CMOS technologies, such as e.g. gate tunnelling current, influence of pocket implants, poly-depletion, quantum-mechanical effects and bias-dependent overlap capacitances.

The goal of this report is to present the full definition of the model, including the parameter set, the geometrical and temperature scaling rules, the model implementation, and all the equations for currents, charges and noise sources.

Apart from the definition also an introduction into the physical background is given, and a basic parameter extraction procedure is described. The complete physical background will be documented separately in a forthcoming report.

Preface and History of Model and Documentation

Preface

A first test version of the compact MOS model, MOS MODEL 11, has been put in the public domain in April 2001. Future changes and additions to the model will be documented by extending or changing the documentation in this Unclassified Report.

History of Model and Documentation

April 2001 : Release of MOS MODEL 11, level 1100, test version

Contents

1 Introduction

MOS Model 11 (MM11) is a new compact MOSFET model, intended for digital, analogue and RF circuit simulation in modern and future CMOS technologies. MM11 is the successor of MOS Model 9, it was especially developed to give not only an accurate description of currents and charges and their first-order derivatives (i.e. transconductance, conductance, capacitances), but also of the higher-order derivatives, resulting in an accurate description of electrical distortion behaviour [1]. The latter is especially important for analog and RF circuit design. The model furthermore gives an accurate description of the noise behaviour of MOSFETs.
MOS Model 11 gives a complete description of all transistor-action related quantities: nodal currents, nodal charges and noise-power spectral densities. The equations describing these quantities are based on surface-potential formulations, resulting in equations valid over all operation regions (i.e. accumulation, depletion and inversion). Although in general the surface potential is implicitly related to the terminal voltages and has to be calculated iteratively, in MM11 it has been approximated by an explicit expression [2]. Additionally, in order for the model to be valid for modern and future MOS devices, several important physical effects have been included in the model: mobility reduction, bias-dependent series-resistance, velocity saturation, drain-induced barrier lowering, static feedback, channel length modulation, self-heating, weak-avalanche (or impact ionization), gate current due to tunnelling, poly-depletion, quantum-mechanical effects on charges and bias-dependent overlap capacitances.

MOS Model 11 only provides a model for the intrinsic transistor and the gate/source- and gate/drain overlap regions. Junction charges, junction leakage currents and interconnect capacitances are not included. They are covered by separate models, which are not part of this documentation. This report has been arranged in the same way as the unclassified report on MOS Model 9 [3].

1.1 Structural Elements of MOS Model 11

The structure of MOS Model 11 is the same as the structure of MOS Model 9. The model is separable into a number of relatively independent parts, namely:

- **Model embedding:** It is convenient to use one single model for both *n*– and *p*–channel devices. For this reason, any *p*-channel device and its bias conditions are mapped onto those of an equivalent *n*-channel transistor. This mapping comprises a number of sign changes. Also, the model describes a symmetrical device, i.e. the source and drain nodes can be interchanged without changing the electrical properties. The assignment of source and drain to the channel nodes is based on the voltages of these nodes: for an *n*-channel transistor the node at the highest potential is called drain. In a circuit simulator the nodes are denoted by their network numbers, based on the circuit configuration. Again, a transformation is necessary involving a number of sign changes, including the directional noise-current sources.

- **Preprocessing:** The complete set of all the parameters, as they occur in the equations for the various electrical quantities, is denoted as the set of actual parameters, usually called the “miniset”. Each of these actual parameters can be determined by purely electrical measurements. Since most of these parameters scale with geometry and temperature the process as a whole is characterized by an enlarged set of parameters, which is denoted as the set of reference and scaling parameters, usually called the “maxiset”. This set of parameters contains most of the actual parameters for a reference device, a large set of sensitivity coefficients and the reference conditions. From this, the actual parameters for an arbitrary transistor under non-reference conditions are obtained by applying a set of transformation rules to the reference parameters. The transformation rules describe the dependencies of the actual parameters on the length, width, and temperature. This procedure is called preprocessing, as it is normally done only once, prior to the actual electrical simulation.

- **Clipping:** For very uncommon geometries or temperatures, the preprocessing rules may generate parameters that are outside a physically realistic range or that may create difficulties in the numerical evaluation of the model, for example division by zero. In order to prevent this, all parameters are limited to a pre-specified range directly after the preprocessing. This procedure is called clipping.
- **Current equations:** These are all expressions needed to obtain the DC nodal currents as a function of the bias conditions. They are segmentable in equations for the channel current, the gate tunnelling current and the avalanche current.
- **Charge equations:** These are all the equations that are used to calculate both the intrinsic and extrinsic charge quantities, which are assigned to the nodes.
- **Noise equations:** The total noise output of a transistor consists of a thermal noise and a flicker noise part, which create fluctuations in the channel current. Owing to the capacitive coupling between gate and channel region, current fluctuations in the gate current are induced as well, which is refered to as induced gate noise.

1.2 Structure of this Technical Note

After this introductory section, the physical background of the current, the charge and the noise equations is discussed to elucidate the model. Next the basic equations are presented. To facilitate an unambiguous discussion of these equations, the nomenclature of the parameter set for an individual transistor and the model constants is given right at the beginning of this documentation. Next all the information, which is needed for the implementation of the model in a circuit simulator, is presented. After the full nomenclature of all different model parameters, quantities and variables, the different structural elements of the model are discussed in detail. The extended model equations contain all the numerical adaptations necessary to facilitate unproblematic evaluation in a circuit simulator. Next the methodology to extract the model parameters is presented. Finally the default values and clipping limits of all parameters are presented, in addition the operating point output (OPO) parameters are described.

2 Physics

2.1 Comments and Physical Background

In this section some physical background on the current, charge and noise description of MOS Model 11 will be given. For the full details of the physical background of the drain-source channel current equations the reader is referred to [1],[2],[4]-[6]. The gate current, charge and noise equations have been newly developed and their physical background will be discussed in a future report. All equations refered to are to be found in Section 2.2.

2.1.1 List of Parameters for an Individual Transistor

In this table the symbolic representation and the recommended programming names for the different parameters of an individual transistor at the actual temperature are given. More information on the nomenclature can be found in Section 3.

No.	Parameter	Program Name	Units	Description
0		LEVEL	-	Must be 1100
1	V_{FB}	VFB	V	Flat-band voltage for the actual transistor at the actual temperature
2	k_0	KO	$\mathrm{V}^{1/2}$	Body-effect factor for the actual transistor
3	$1/k_{\mathrm{P}}$	KPINV	$\mathrm{V}^{-1/2}$	Inverse of body-effect factor of the poly-silicon gate for the actual transistor
4	ϕ_{B}	PHIB	V	Surface potential at the onset of strong inversion for the actual transistor at the actual temperature
5	β	BET	AV^{-2}	Gain factor for the actual transistor at the actual temperature
6	θ_{sr}	THESR	V^{-1}	Coefficient of the mobility reduction due to surface roughness scattering for the actual transistor at the actual temperature
7	θ_{ph}	THEPH	V^{-1}	Coefficient of the mobility reduction due to phonon scattering for the actual transistor at the actual temperature
8	η_{mob}	ETAMOB	-	Effective field parameter for dependence on depletion/inversion charge for the actual transistor at the actual temperature
9	ν	NU	-	Exponent of field dependence of mobility model at the actual temperature
10	θ_{R}	THER	V^{-1}	Coefficient of the series resistance for the actual transistor at the actual temperature: $\theta_{\mathrm{R}} = 2 \cdot \beta \cdot R_{\mathrm{S}}$
11	θ_{R1}	THER1	V	Numerator of the gate voltage dependent part of series resistance for the actual transistor
12	θ_{R2}	THER2	V	Denominator of the gate voltage dependent part of series resistance for the actual transistor

No.	Parameter	Program Name	Units	Description
13	θ_{sat}	THESAT	V^{-1}	Velocity saturation parameter due to optical/acoustic phonon scattering for the actual transistor at the actual temperature
14	θ_{Th}	THETH	V^{-3}	Coefficient of self-heating for the actual transistor at the actual temperature
15	σ_{dibl}	SDIBL	$\mathrm{V}^{-1/2}$	Drain-induced barrier-lowering parameter for the actual transistor
16	m_0	MO	-	Parameter for (short-channel) subthreshold slope for the actual transistor
17	σ_{sf}	SSF	$\mathrm{V}^{-1/2}$	Static-feedback parameter for the actual transistor
18	α	ALP	-	Factor of the channel length modulation for the actual transistor
19	V_{P}	VP	V	Characteristic voltage of the channel length modulation
20	m	MEXP	-	Smoothing factor for the actual transistor
21	ϕ_{T}	PHIT	V	Thermal voltage at the actual temperature
22	a_1	A1	-	Factor of the weak–avalanche current for the actual transistor at the actual temperature
23	a_2	A2	V	Exponent of the weak–avalanche current for the actual transistor
24	a_3	A3	-	Factor of the drain–source voltage above which weak–avalanche occurs for the actual transistor
25	I_{GINV}	IGINV	AV^{-2}	Gain factor for intrinsic gate tunnelling current in inversion for the actual transistor
26	B_{inv}	BINV	V	Probability factor for intrinsic gate tunnelling current in inversion
27	I_{GACC}	IGACC	AV^{-2}	Gain factor for intrinsic gate tunnelling current in accumulation for the actual transistor
28	B_{acc}	BACC	V	Probability factor for intrinsic gate tunnelling current in accumulation
29	V_{FBov}	VFBOV	V	Flat-band voltage for the Source/Drain overlap extensions
30	k_{ov}	KOV	$\mathrm{V}^{1/2}$	Body-effect factor for the Source/Drain overlap extensions
31	I_{GOV}	IGOV	AV^{-2}	Gain factor for Source/Drain overlap gate tunnelling current for the actual transistor
32	C_{ox}	COX	F	Oxide capacitance for the intrinsic channel for the actual transistor
33	C_{GDO}	CGDO	F	Oxide capacitance for the gate–drain overlap for the actual transistor
34	C_{GSO}	CGSO	F	Oxide capacitance for the gate–source overlap for the actual transistor

No.	**Parameter**	**Program Name**	**Units**	**Description**
35	–	GATENOISE		Flag for in/exclusion of induced gate thermal noise
36	N_{T}	NT	J	Coefficient of the thermal noise for the actual transistor at the actual temperature
37	N_{FA}	NFA	$\mathrm{V}^{-1}\mathrm{m}^{-4}$	First coefficient of the flicker noise for the actual transistor
38	N_{FB}	NFB	$\mathrm{V}^{-1}\mathrm{m}^{-2}$	Second coefficient of the flicker noise for the actual transistor
39	N_{FC}	NFC	V^{-1}	Third coefficient of the flicker noise for the actual transistor
40	t_{ox}	TOX	m	Thickness of gate oxide layer
41	N_{MULT}	MULT	-	Number of devices in parallel

Note: The parameter t_{ox} is used for calculation of the effective oxide thickness (due to quantum-mechanical effects) and the $1/f$ noise, not for the calculation of β!!!

2.1.2 List of Physical Constants

In this table the symbolic representation, the recommended programming names and the value of the various physical constants used in MOS Model 11 are given.

No.	**Constant**	**Program Name**	**Units**	**Description**
1	T_0	TO	K	Offset for conversion from Celsius to Kelvin temperature scale (273.15)
2	k_{B}	KB	JK^{-1}	Boltzmann constant ($1.3806226 \cdot 10^{-23}$)
3	q	Q	C	Elementary unit charge ($1.6021918 \cdot 10^{-19}$)
4	ϵ_{ox}	EPSOX	Fm^{-1}	Absolute permittivity of the oxide layer ($3.453143800 \cdot 10^{-11}$)
5	QM_{N}	QMN	$\mathrm{V\,m}^{\frac{4}{3}}\mathrm{C}^{-\frac{2}{3}}$	Constant of quantum-mechanical behaviour of electrons ($5.951993000 \cdot 10^{+00}$)
6	QM_{P}	QMP	$\mathrm{V\,m}^{\frac{4}{3}}\mathrm{C}^{-\frac{2}{3}}$	Constant of quantum-mechanical behaviour of holes ($7.448711000 \cdot 10^{+00}$)
7	$\chi_{\mathrm{B_N}}$	CHIBN	V	Tunnelling barrier height for electrons for Si/SiO2-structure ($3.100000000 \cdot 10^{+00}$)
7	$\chi_{\mathrm{B_P}}$	CHIBP	V	Tunnelling barrier height for holes for Si/SiO2-structure ($4.500000000 \cdot 10^{+00}$)

2.1.3 Comments on Current Equations

Conventional MOS models such as MOS Model 9 and BSIM4 are threshold-voltage-based models, which make use of approximate expressions of the drain-source channel current I_{DS} in the weak-inversion region (i.e. subthreshold) and in the strong-inversion region (i.e. well above threshold). These approximate equations are tied together using a mathematical smoothing function, resulting in neither a physical nor an accurate description of I_{DS} in the moderate inversion region (i.e. around threshold). With the constant downscaling of supply voltage the moderate inversion region becomes more and more important, and an accurate description of this region is thus essential.

A more accurate type of model is the surface-potential-based model, where the channel current I_{DS} is split up in a drift (I_{drift}) and a diffusion (I_{diff}) component, which are a function of the gate bias V_{GB} and the surface potential at the source (ψ_{s_0}) and the drain (ψ_{s_L}) side. In this way I_{DS} can be accurately described using one equation for all operating regions (i.e. weak, moderate and strong-inversion). MOS Model 11 is a surface-potential-based model.

Surface Potential: The surface potential ψ_s is defined as the electrostatic potential at the gate oxide/substrate interface with respect to the neutral bulk (due to the band bending, see Fig.2.1 (a)). For an n-MOS transistor with uniform doping concentration it can be calculated from the following implicit relation:

$$\left(\frac{V_{GB} - V_{FB} - \psi_p - \psi_s}{k_0}\right)^2 = \psi_s + \phi_T \cdot \left[\exp\left(-\frac{\psi_s}{\phi_T}\right) - 1\right]$$
$$+ \phi_T \cdot \exp\left(-\frac{\phi_B + V}{(1+m_0)\cdot\phi_T}\right) \cdot \left[\exp\left(\frac{\psi_s}{(1+m_0)\cdot\phi_T}\right) - 1\right]$$

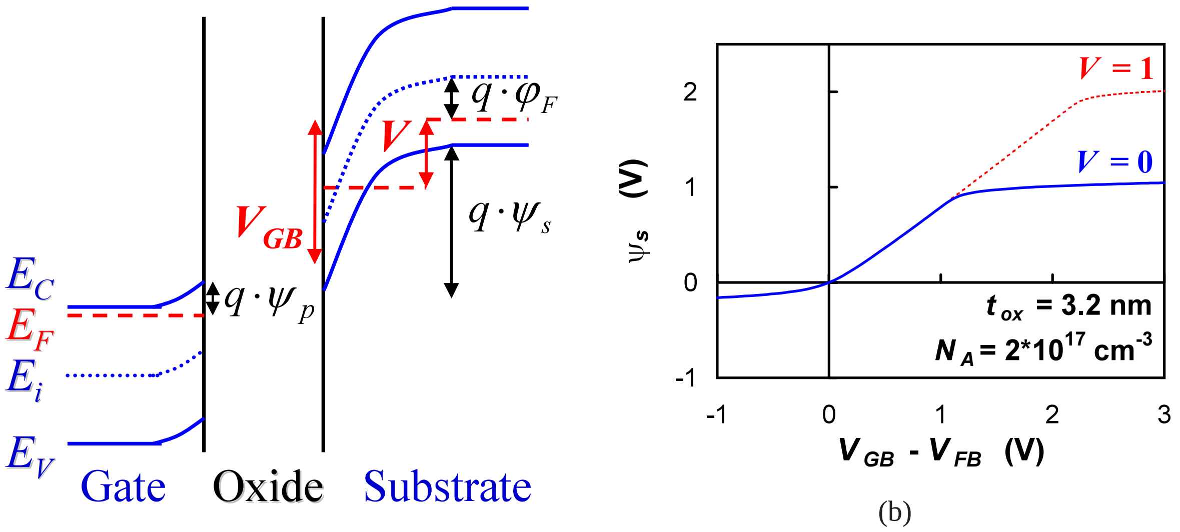
where V is the quasi-Fermi potential, which ranges from V_{SB} at the source side to V_{DB} at the drain side. The parameter m_0 has been added to model the non-ideal subthreshold behaviour of short-channel transistors[1], and ψ_p is the potential drop in the polysilicon gate material due to the poly-depletion effect. The latter is given by[2]:

$$\psi_p = \begin{cases} 0 & \text{for: } V_{GB} \le V_{FB} \\ \left(\sqrt{V_{GB} - V_{FB} - \psi_s + \frac{kp^2}{4}} - \frac{kp}{2}\right)^2 & \text{for: } V_{GB} > V_{FB} \end{cases}$$

In Fig. 2.1 (b) the surface potential is shown as a function of gate bias for a typical n-type MOS device. The surface potential ψ_s is implicitly related to the gate bias V_{GB} and the quasi-Fermi potential V, and cannot be calculated analytically. It can only be calculated using an iterative solution, which in general is computation-time consuming. In MOS Model 11 an explicit approximation of the surface potential is used, which has partly been treated in [2]. In the inversion region ($V_{GB} > V_{FB}$) the surface potential is approximated by $\psi_{s_{inv}}$ given by eqs. (2.8)-(2.10) and (2.17)-(2.21), where variable Δ_{acc} is used to describe the influence of majority carriers. In the accumulation region ($V_{GB} < V_{FB}$) the surface potential is approximated by $\psi_{s_{acc}}$ given by eqs. (2.22)-(2.24). The total surface potential ψ_s is simply given by $\psi_{s_{inv}} + \psi_{s_{acc}}$.

[1] Parameter $m_0 = 0$ for the ideal long-channel case.

[2] For $V_{GB} < V_{FB}$ an accumulation layer is formed in both the substrate silicon and the gate polysilicon, in this case ψ_p is slightly negative and weakly dependent on V_{GB}. This effect has been neglected.



(a) (b)

Figure 2.1: (a) The energy band diagram of an n-type MOS transistor in inversion ($V_{GB} > V_{FB}$), where ψ_s is the surface potential, ψ_p is the potential drop in the gate due to the poly-depletion effect, V is the quasi-Fermi potential and ϕ_F is the intrinsic Fermi-potential ($\phi_B = 2 \cdot \phi_F$).
(b) The surface potential as a function of gate bias for different values of quasi-Fermi potential V ($m_0 = 0$).

A surface-potential-based model automatically incorporates the pinch-off condition at the drain side, and as a result it gives a description of both the linear (or ohmic) region and the saturation region for the ideal long-channel case. In this case the saturation voltage V_{DSAT} (i.e. the drain-source voltage above which saturation occurs) corresponds to eq. (2.11). For short-channel devices, however, no real pinch-off occurs and the saturation voltage is affected by velocity saturation and series-resistance. In this case the saturation voltage V_{DSAT} is calculated using eqs. (2.11)-(2.15). The transition from linear to saturation region is no longer automatically described by the surface-potential-based model. This has been solved in the same way as in [7] by introducing an effective drain-source bias V_{DS_x} which changes smoothly from V_{DS} in the linear region to V_{DSAT} in the saturation region, see eq. (2.16).

A surface-potential-based model makes no use of threshold voltage V_T. Circuit designers, however, are used to think in terms of threshold voltage, and as a consequence it would be useful to have a description of V_T in the framework of a surface-potential-model. It has been found that an accurate expression of threshold voltage is simply given by:

$$V_T = V_{FB} + \left(1 + \frac{k_0{}^2}{k_p{}^2}\right) \cdot (V_{SB} + \phi_B + 2 \cdot \phi_T) - V_{SB} + k_0 \cdot \sqrt{V_{SB} + \phi_B + 2 \cdot \phi_T}$$

The threshold voltage and other important parameters for circuit design are part of the operating point output as given in Section 8.3.

Channel Current: Neglecting the influence of gate and bulk current, the channel current can be written as:

$$I_{DS} = I_{drift} + I_{diff}$$

where ideally the drift component I_{drift} can be approximated by (for $V_{\mathrm{GB}} > V_{\mathrm{FB}}$):

$$I_{\mathrm{drift}} = \beta \cdot \left(\frac{2 \cdot \left[V_{\mathrm{GB}} - V_{\mathrm{FB}} - \frac{\psi_{\mathrm{s_L}} + \psi_{\mathrm{s_0}}}{2} \right]}{1 + \sqrt{1 + \frac{4}{k_{\mathrm{P}}{}^2} \cdot \left[V_{\mathrm{GB}} - V_{\mathrm{FB}} - \frac{\psi_{\mathrm{s_L}} + \psi_{\mathrm{s_0}}}{2} \right]}} - k_0 \cdot \sqrt{\frac{\psi_{\mathrm{s_L}} + \psi_{\mathrm{s_0}}}{2}} \right) \cdot \left(\psi_{\mathrm{s_L}} - \psi_{\mathrm{s_0}} \right)$$

and the diffusion component I_{diff} can be approximated by (for $V_{\mathrm{GB}} > V_{\mathrm{FB}}$):

$$I_{\mathrm{diff}} = \beta \cdot \phi_{\mathrm{T}} \cdot \left(Q_{\mathrm{inv_L}} - Q_{\mathrm{inv_0}} \right) \cdot \frac{t_{\mathrm{ox}}}{\epsilon_{\mathrm{ox}}}$$

In the latter equation $Q_{\mathrm{inv_0}}$ and $Q_{\mathrm{inv_L}}$ denote the inversion-layer charge density at the source and drain side, respectively, which are given by eqs. (2.40)-(2.42) (where $Q_{\mathrm{inv}} = -\epsilon_{\mathrm{ox}} / t_{\mathrm{ox}} \cdot V_{\mathrm{inv}}$).

In the non-ideal case the channel current is affected by several physical effects, such as drain-induced barrier lowering, static feedback, mobility reduction, series-resistance, velocity saturation, channel length modulation and self-heating, which have to be taken into account in the channel current expression:

- In threshold-voltage-based models drain-induced barrier lowering and static feedback are traditionally implemented as a decrease in threshold voltage with drain bias. Here these effects have been implemented as an increase in effective gate bias ΔV_{G} given by eqs. (2.1)-(2.7). An effective drain-source voltage $V_{\mathrm{DS_{eff}}}$ has been used to preserve non-singular behaviour in the higher-order derivatives of I_{DS} at $V_{\mathrm{DS}} = 0$ V.

- The effects of mobility reduction and series-resistance on channel current have been described in [5], and have consequently been implemented using eqs. (2.33) and (2.37), respectively.

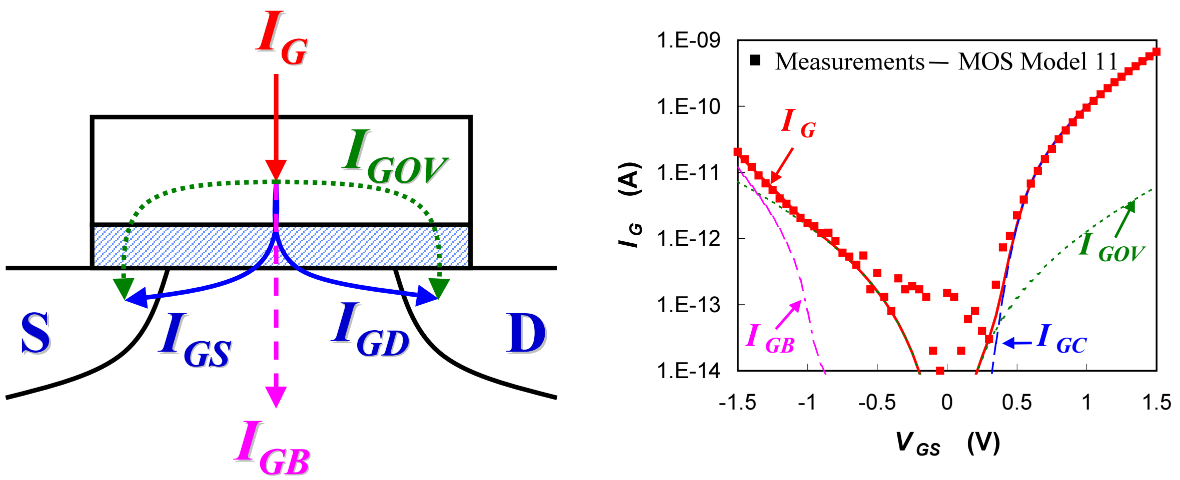
- The effect of velocity saturation has been modelled along the same lines as was done in [6] with the exception of the electrical field distribution. In [6] the influence of the electron velocity saturation expression

  $$v = \frac{\mu \cdot E_{\parallel}}{\sqrt{1 + \left(\mu / v_{\mathrm{sat}} \cdot E_{\parallel} \right)^2}}$$

  was approximated assuming that the lateral electric field $E_{\parallel}$ in the denominator is constant and equal to $\left(\psi_{\mathrm{s_L}} - \psi_{\mathrm{s_0}} \right) / L$. Here we assume that $E_{\parallel}$ (in the denominator) increases linearly along the channel (from 0 at the source to $2 \cdot \left(\psi_{\mathrm{s_L}} - \psi_{\mathrm{s_0}} \right) / L$ at the drain), and obtain a more accurate expression for velocity saturation, which has been implemented using eq. (2.35).

- The effect of channel length modulation and self-heating on channel current have been described in [6], and have consequently been implemented using eqs. (2.36) and (2.38), respectively.

All the above effects can be incorporated into the channel current expression using eq. (2.39) and eq. (2.45).



(a) (b)

Figure 2.2: (a) The different gate current components in a MOS transistor. One can distinguish the intrinsic components, i.e. the gate-to-channel current I_{GC} $(= I_{GS} + I_{GD})$ and the gate-to-bulk current I_{GB}, and the extrinsic, i.e. the gate/source and gate/drain overlap components I_{Gov}. (b) Measured and modelled gate current as a function of gate bias V_{GS} at $V_{DS} = V_{SB} = 0$ V, the different gate current components are also shown. NMOS-transistor, $W/L = 10/0.6\mu$m and $t_{ox} = 2$nm.

Weak-Avalanche Current: At high drain bias, owing to the weak-avalanche effect (or impact ionization), a current I_{avl} will flow between drain and bulk[3]. The description of the weak-avalanche current has been taken from MOS Model 9 [3], and is given by eq. (2.46). With the down-scaling of supply voltage for modern CMOS technologies, weak-avalanche becomes less and less important.

Gate Tunnelling Current: With CMOS technology scaling the gate oxide thickness is reduced and, due to the direct-tunnelling of carriers through the oxide, the gate current is no longer negligible, and has to be taken into account. Several gate current components can be distinguished, three components (I_{GS}, I_{GD} and I_{GB}) due to the intrinsic MOS channel, and two components (I_{Gov_0} and I_{Gov_L}) due to gate/source and gate/drain overlap region, see Fig. 2.2 (a).

For an n-type MOS transistor operating in inversion, the intrinsic gate current density J_G consists of electrons tunnelling from the inversion layer to the gate, the so-called conductance band tunnelling, which in general can be written as [8] (for $V_{GB} > V_{FB}$):

$$J_G \propto -V_{ox} \cdot Q_{inv} \cdot P_{tun} \{V_{ox}; \chi_B; B\}$$

where V_{ox} is the oxide voltage given by $V_{ox} = V_{GB} - V_{FB} - \psi_p - \psi_s$. The carrier tunnelling probability P_{tun} is a function of the oxide voltage V_{ox}, the oxide energy barrier χ_B as observed by the inversion-layer carriers, and a parameter B. This probability is given by eq. (2.47), where both direct-tunnelling for $V_{ox} < \chi_B$ and Fowler-Nordheim tunnelling for $V_{ox} > \chi_B$ have been taken into account.

Owing to quantum-mechanical energy quantization in the potential well at the SiO_2-surface, the electrons in the inversion layer are not situated at the bottom of the conduction band, but in the lowest

[3] In reality part of the generated avalanche current will also flow from drain to source [1], this has been neglected.

energy subband which lies $\Delta\chi_{\rm B}$ above the conduction band. Assuming that only the lowest energy subband is occupied by electrons, the value of $\Delta\chi_{\rm B}$ can be given by eq. (2.64) [9]. As a result the oxide barrier $\chi_{\rm B_{eff}}$ has to be lowered by an amount of $\Delta\chi_{\rm B}$, see eq. (2.65).
In inversion the total intrinsic gate current consists of electrons tunnelling from inversion layer to gate, the so-called gate-to-channel current $I_{\rm GC}$. These electrons are supplied by both source ($I_{\rm GS}$) and drain ($I_{\rm GD}$). The gate-to-channel current $I_{\rm GC}$ can be calculated from:

$$I_{\rm GC} = W \cdot \int_0^L J_{\rm G} \cdot dx$$

where x is the coordinate along the channel. Using a first-order perturbation approximation, i.e. assuming the gate current is small enough so that it does not change the distribution of surface potential along the channel, $I_{\rm GC}$ can be calculated by eqs. (2.64)-(2.74). In the same way the partitioning of $I_{\rm GC}$ into $I_{\rm GS}$ and $I_{\rm GD}$ can be calculated using:

$$I_{\rm GS} = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) \cdot J_{\rm G} \cdot dx$$

$$I_{\rm GD} = W \cdot \int_0^L \frac{x}{L} \cdot J_{\rm G} \cdot dx$$

which results in expressions for $I_{\rm GS}$ and $I_{\rm GD}$ as given by eqs. (2.75)-(2.77). The gate-to-channel current $I_{\rm GC}$ can be seen in Fig. 2.2 (b) as a function of gate bias for a typical n-MOS transistor at $V_{\rm DS} = 0$ (i.e. $I_{\rm GS} = I_{\rm GD} = 1/2 \cdot I_{\rm GC}$).

For an n-type MOS transistor operating in accumulation, an accumulation layer of holes is formed in the p-type substrate and an accumulation layer of electrons is formed in the n^+-type polysilicon gate. Since the oxide energy barrier for electrons $\chi_{\rm B_N}$ is considerably lower than that for holes $\chi_{\rm B_P}$, the gate current will mainly consist of electrons tunnelling from the gate to the bulk silicon, where they are swept to the bulk terminal. In this case the (intrinsic) gate current density $J_{\rm G}$ can be written as [8] (for $V_{\rm GB} < V_{\rm FB}$):

$$J_{\rm G} \propto -V_{\rm ox} \cdot Q_{\rm acc} \cdot P_{\rm tun}\left\{-V_{\rm ox};\, \chi_{\rm B};\, B\right\}$$

where $Q_{\rm acc}$ is the accumulation charge density in the gate given by $\epsilon_{\rm ox} \big/ t_{\rm ox} \cdot V_{\rm ox}$. In order to limit calculation time the quantum-mechanical oxide barrier lowering in this case is neglected, and the resulting expression for $I_{\rm GB}$ is given by eqs. (2.62)-(2.63). The gate-to-bulk current $I_{\rm GB}$ can be seen in Fig. 2.2 (b) as a function of gate bias for a typical n-MOS transistor at $V_{\rm DS} = 0$.

Apart from the intrinsic components $I_{\rm GC}$ and $I_{\rm GB}$, considerable gate current can be generated in the gate/source- and gate/drain-overlap regions. Concentrating on the gate/source[4]-overlap region, in order to calculate the overlap gate current, the overlap region is treated as an n^+-gate/oxide/n^+-bulk MOS capacitance where the source acts as bulk. Although the impurity doping concentration in the n^+-source extension region is non-uniform in both lateral and transversal direction, it is assumed that an effective flat-band voltage $V_{\rm FBov}$ and body-factor $k_{\rm ov}$ can be defined for this structure. Furthermore

[4] In the following derivation, the same can be done for the gate/drain-overlap region by replacing the source by the drain.

assuming that only accumulation and depletion occur in the n^+-source region[5], a surface potential ψ_{sov} can be calculated using:

$$\left(\frac{V_{GS} - V_{FBov} - \psi_{p_{ov}} - \psi_{sov}}{k_{ov}}\right)^2 = -\psi_{sov} + \phi_T \cdot \left[\exp\left(\frac{\psi_{sov}}{\phi_T}\right) - 1\right]$$

where the potential drop in the polysilicon gate material due to the poly-depletion effect $\psi_{p_{ov}}$ is given by:

$$\psi_{p_{ov}} = \begin{cases} 0 & \text{for: } V_{GS} \leq V_{FBov} \\ \left(\sqrt{V_{GS} - V_{FBov} - \psi_{sov} + \frac{k_P{}^2}{4}} - \frac{k_P}{2}\right)^2 & \text{for: } V_{GS} > V_{FBov} \end{cases}$$

Again the surface potential $\psi_{p_{ov}}$ can be explicitly approximated, this is done by using eqs. (2.48)-(2.54).

For $V_{GS} > V_{FBov}$ a negatively charged accumulation layer is formed in the overlapped n^+-source extension and a positively charged depletion layer is formed in the overlapping gate. In this case the overlap gate current will mostly consist of electrons tunnelling from the source accumulation layer to the gate, it is given by:

$$I_{Gov} \propto -V_{ov} \cdot Q_{ov} \cdot P_{tun}\{V_{ov}; \chi_B; B\}$$

where V_{ov} is the oxide voltage for the gate/source-overlap ($= V_{GS} - V_{FBov} - \psi_{p_{ov}} - \psi_{sov}$), given by eqs. (2.55)-(2.57), and Q_{ov} is the total charge density in the n^+-source region ($= -\epsilon_{ox}/t_{ox} \cdot V_{ov}$). For $V_{GS} < V_{FBov}$ the situation is reversed, a positively charged depletion layer is formed in the overlapped n^+-source extension and a negatively charged accumulation layer is formed in the overlapping gate. In this case the overlap gate current will mostly consist of electrons tunnelling from the gate accumulation layer to the source, it is given by:

$$I_{Gov} \propto V_{ov} \cdot Q_{ov} \cdot P_{tun}\{-V_{ov}; \chi_B; B\}$$

The overlap gate current components can now be given by eqs. (2.58)-(2.61). In Fig. 2.2 (b) the gate overlap current I_{Gov} is shown as a function of gate bias for a typical n-MOS transistor at $V_{DS} = 0$ (i.e. $I_{Gov_L} = I_{Gov_0}$).

For n-type and p-type MOS transistors the gate current behaviour is different due to the type of carriers that constitute the different gate current components[6]. The difference is summarized in Tab. 2.1.

2.1.4 Comments on Charge Equations

In a typical MOS structure we can distinguish intrinsic and extrinsic charges. The latter are due to the gate/source and gate/drain overlap regions. The drain/source junctions also contribute to the capacitance behaviour of a MOSFET, but this is not taken into account in MOS Model 11; it is described by a separate junction diode model.

[5] Since the source extension has a very high doping concentration, an inversion layer in the gate/source overlap will only be formed at very negative gate-source bias values. This effect has been neglected.

[6] It is assumed here that the gate current is only determined by conductance band tunnelling. For high values of gate bias (i.e. $q \cdot V_{ox} > E_g$) electrons in the bulk valence band may also tunnel through the oxide to the gate conduction band. This mechanism is referred to as valence band tunnelling, and it has not been taken into account in MOS Model 11.

Table 2.1: The type of carriers that contribute to the gate tunnelling current in the various operation regions for the intrinsic MOSFET, the gate/drain- and gate/source-overlap regions. The type of carriers determine the value of oxide energy barrier χ_B that has to be used (χ_{B_N} for electrons, χ_{B_P} for holes). In the last row the direction of gate current is indicated.

Type	Intrinsic MOSFET		Overlap Regions
	Accumulation	Inversion	
NMOS	electrons	electrons	electrons
PMOS	electrons	holes	holes
	I_{GB}	I_{GS} / I_{GD}	I_{GS} / I_{GD}

Intrinsic Charges: In the intrinsic MOS transistor charges can be attributed to the four terminals. The bulk charge Q_B, which is determined by either the depletion charge (for $V_{GB} > V_{FB}$) or the accumulation charge (for $V_{GB} < V_{FB}$), can be calculated from:

$$Q_B = W \cdot \int_0^L (Q_{tot} - Q_{inv}) \cdot dx$$

where Q_{tot} is the total charge density in the silicon bulk ($Q_{tot} = -\epsilon_{ox}/t_{ox} \cdot V_{ox}$). The total inversion-layer charge Q_{inv} is split up in a source Q_S and a drain Q_D charge, they can be calculated using the Ward-Dutton charge partitioning scheme [10]:

$$Q_S = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) \cdot Q_{inv} \cdot dx$$

$$Q_D = W \cdot \int_0^L \frac{x}{L} \cdot Q_{inv} \cdot dx$$

Since charge neutrality holds for the complete transistor, the gate charge is simply given by:

$$Q_G = -Q_S - Q_D - Q_B$$

The above equations have been solved, and the charges are given by eqs. (2.81)-(2.89). In these equations $C_{ox_{eff}}$ is the effective oxide capacitance, which is smaller than the ideal oxide capacitance C_{ox} due to quantum-mechanical effects: Quantum-mechanically, the inversion/accumulation charge concentration is not maximum at the Si-SiO$_2$-interface (as it would be in the classical case), but reaches a maximum at a distance Δz from the interface [9]. This quantum-mechanical effect can be taken into account by an effective oxide thickness $t_{ox} + \epsilon_{ox} / \epsilon_{Si} \cdot \Delta z$, where Δz is dependent on the effective electric field E_{eff} [9], [11] ($E_{eff} = -\epsilon_{ox} / \epsilon_{Si} \cdot V_{eff} / t_{ox}$). The effective oxide thickness results in an effective oxide capacitance $C_{ox_{eff}}$, see eq. (2.80).

It should be noted that the above charge model is quasi-static. A phase-shift between drain channel current and gate voltage is not taken into account. This implies that for a few applications at high frequencies approaching the cut-off frequency, errors have to be expected due to non-quasi-static effects. Nevertheless non-quasi-effects can be taken into account using a segmentation model as described in [12].

Extrinsic Charges: The gate/source- and gate/drain-overlap regions act as bias-dependent capacitances. In order to take this bias-dependence into account the overlap regions are treated as an n^+-gate/oxide/n^+-bulk MOS capacitance along the same lines as was done for the overlap gate current, see Section 2.1.3. The charge in the overlap regions can simply be given by eqs. (2.78)-(2.79). The quantum-mechanical effect on oxide thickness has been neglected here in order to reduce calculation time.

2.1.5 Comments on Noise Equations

In a MOS transistor generally three different types of noise can be observed: $1/f$-noise, thermal noise and induced gate noise. The gate tunnel current and the bulk avalanche current will also exhibit noisy behaviour (due to shot noise), however this has been neglected in MOS Model 11.

$1/f$-Noise: At low frequencies flicker (or $1/f$) noise becomes dominant in MOSFETs. In the past this type of noise has been interpreted either in terms of trapping and detrapping of charge carriers in the gate oxide or in terms of mobility fluctuations. Over the past years, a general model for $1/f$-noise which combines both of the above physical origins [13], [14], has found wide acceptance in the field of MOS modelling. The model assumes that the carrier number in the channel fluctuates due to trapping/detrapping in the gate oxide, and that these number fluctuations also affect the carrier mobility resulting in (correlated) mobility fluctuations.

The same model is part of MOS Model 9 [15], and has been used to calculate the $1/f$-noise for MOS Model 11. The calculations have been performed in such a way that the resulting expression for spectral density is valid for all operation regions (i.e. both in subthreshold and above threshold), it is given by eqs. (2.94)-(2.97).

Thermal Noise: Since the MOSFET channel can be considered as a non–linear resistor, the channel current is subject to thermal noise. Let thermal–noise current sources be parallel connected to each infinitesimal short element of the channel, it can be shown that the noise spectral density, which is defined by [16]:

$$< \Delta i_{\mathrm{th}}{}^2 > \;=\; \int_0^{\infty} S_{\mathrm{th}}\,(f)\,\mathrm{d}f$$

is given by a generalized Nyquist relation:

$$S_{\mathrm{th}} \;=\; \frac{N_{\mathrm{T}}}{L^2}\int_0^{L} g\,(x)\,\mathrm{d}x$$

where N_{T} is equal to $4 \cdot k_{\mathrm{B}} \cdot T$ and $g\,(x)$ is the local specific channel conductance:

$$g\,(x) = -\mu\,(x) \cdot W \cdot Q_{\mathrm{inv}}(x)$$

Here the mobility $\mu\,(x)$ is position dependent mainly due to the effect of velocity saturation. Elaborating the latter integral via a transform of the x–variable into the quasi-Fermi potential $V(x)$, we obtain the spectral density given by eqs. (2.91)-(2.93). Again continuity of the noise model is assured along all modes of operation. The above thermal noise model has been found to accurately describe experimental results for various CMOS technologies without having to invoke carrier heating effects [17].

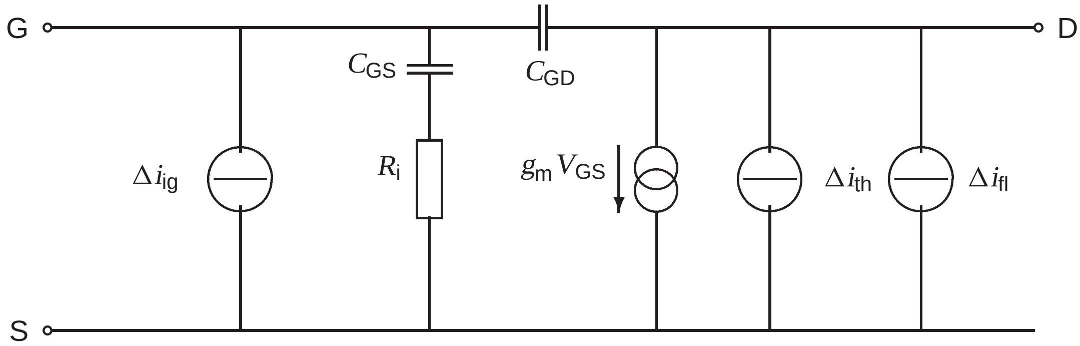


Figure 2.3: Noise current sources in the electrical scheme of the MOS transistor

Induced Gate Noise: Owing to capacitive coupling between gate and channel, the fluctuating channel current induces noise in the gate terminal at high frequencies. Unfortunately the calculation of this component from first principles is too complicated to provide a result applicable to circuit simulation. It is more practical to derive the desired result from an equivalent circuit presentation given in Fig. 2.3. Owing to the mentioned capacitive coupling, a part of the channel is present as a resistance in series with the gate input capacitance. In saturation this resistance is approximately equal to:

$$R_i = \frac{1}{3 \cdot g_m}$$

It can be easily shown that the latter resistance produces an input noise current with a spectral density given by eq. (2.98). In addition, since Δi_{th} and Δi_{ig} have the same physical source, both spectral densities are correlated. This is expressed by eqs. (2.99) and (2.100).
The induced gate noise S_{ig} is a so-called non-quasi static (NQS) effect. Since the use of the channel current noise description in an NQS segmentation model [12] would automatically result in a correct description of induced gate noise, S_{ig} can be made equal to zero by using parameter GATENOISE, see eq. (2.98).

2.2 Basic Equations

The equations listed in the following sections, are the basic equations of MOS Model 11 without any adaptations necessary for numerical reasons. As such they form the bas of parameter extraction. In the following, a function is denoted by $F\{variable, \ldots\}$, where F denotes the function name and the function variables are enclosed by braces {}.

2.2.1 Internal Parameters

$$P_\mathrm{D} = 1 + \left(k_0 \big/ k_\mathrm{P}\right)^2$$

$$V_\mathrm{limit} = 5 \cdot \phi_\mathrm{T}$$

$$\theta_{\mathrm{R_{eff}}} = \frac{1}{2}\theta_\mathrm{R} \cdot \left(1 + \frac{\theta_\mathrm{R1}}{1/2 + \theta_\mathrm{R2}}\right)$$

$$Acc = \left.\frac{\partial \psi_\mathrm{s}}{\partial V_\mathrm{GB}}\right|_{V_\mathrm{GB}=V_\mathrm{FB}} = \frac{1}{1 + k_0 \big/ \sqrt{2\phi_\mathrm{T}}}$$

$$N_{\phi_\mathrm{T}} = (2.6)^2 / k_0$$

$$Acc_\mathrm{ov} = \left.\frac{\partial \psi_\mathrm{sov}}{\partial V_\mathrm{GB}}\right|_{V_\mathrm{GB}=V_\mathrm{FBov}} = \frac{1}{1 + k_\mathrm{ov} \big/ \sqrt{2\phi_\mathrm{T}}}$$

$$QM_\psi = \begin{cases} QM_\mathrm{N} \cdot \left(\epsilon_\mathrm{ox} \big/ t_\mathrm{ox}\right)^{2/3} & \text{for NMOS} \\ QM_\mathrm{P} \cdot \left(\epsilon_\mathrm{ox} \big/ t_\mathrm{ox}\right)^{2/3} & \text{for PMOS} \end{cases}$$

$$QM_\mathrm{tox} = \frac{2}{5} \cdot QM_\psi$$

$$\chi_{\mathrm{B_{inv}}} = \begin{cases} \chi_{\mathrm{B_N}} & \text{for NMOS} \\ \chi_{\mathrm{B_P}} & \text{for PMOS} \end{cases}$$

$$\chi_{\mathrm{B_{acc}}} = \chi_{\mathrm{B_N}}$$

2.2.2 Basic Current Equations

Drain induced barrier lowering and Static Feedback:

$$V_{\mathrm{GB_{eff}}} = \begin{cases} 0 & \text{for:} \quad V_\mathrm{GS} + V_\mathrm{SB} - V_\mathrm{FB} \le 0 \\ V_\mathrm{GS} + V_\mathrm{SB} - V_\mathrm{FB} & \text{for:} \quad V_\mathrm{GS} + V_\mathrm{SB} - V_\mathrm{FB} > 0 \end{cases} \tag{2.1}$$

$$\psi_{\mathrm{sat_0}} = \left(\frac{\sqrt{P_\mathrm{D} \cdot V_{\mathrm{GB_{eff}}} + {k_0}^2/4} - k_0/2}{P_\mathrm{D}}\right)^2 \tag{2.2}$$

$$D_{\mathrm{dibl}} = \sigma_{\mathrm{dibl}} \cdot \sqrt{V_{\mathrm{SB}} + \phi_{\mathrm{B}}} \tag{2.3}$$

$$D_{\mathrm{sf}} = \begin{cases} 0 & \text{for:} \quad \psi_{\mathrm{sat}_0} - V_{\mathrm{SB}} - \phi_{\mathrm{B}} \leq 0 \\ \sigma_{\mathrm{sf}} \cdot \sqrt{\psi_{\mathrm{sat}_0} - V_{\mathrm{SB}} - \phi_{\mathrm{B}}} & \text{for:} \quad \psi_{\mathrm{sat}_0} - V_{\mathrm{SB}} - \phi_{\mathrm{B}} > 0 \end{cases} \tag{2.4}$$

$$D = \begin{cases} D_{\mathrm{dibl}} & \text{for:} \quad D_{\mathrm{sf}} \leq D_{\mathrm{dibl}} \\ D_{\mathrm{sf}} & \text{for:} \quad D_{\mathrm{sf}} > D_{\mathrm{dibl}} \end{cases} \tag{2.5}$$

$$V_{\mathrm{DS_{eff}}} = \frac{{V_{\mathrm{DS}}}^4}{\left({V_{\mathrm{limit}}}^2 + {V_{\mathrm{DS}}}^2\right)^{3/2}} \tag{2.6}$$

$$\Delta V_{\mathrm{G}} = D \cdot V_{\mathrm{DS_{eff}}} \tag{2.7}$$

Redefinition of $V_{\mathrm{GB_{eff}}}$, equation (2.1):

$$V_{\mathrm{GB_{eff}}} = \begin{cases} 0 & \text{for:} \quad V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}} \leq 0 \\ V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}} & \text{for:} \quad V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}} > 0 \end{cases} \tag{2.8}$$

$$\Delta_{\mathrm{acc}} = \phi_{\mathrm{T}} \cdot \left[\exp\left(-\frac{Acc \cdot V_{\mathrm{GB_{eff}}}}{\phi_{\mathrm{T}}}\right) - 1\right] \tag{2.9}$$

$$\psi_{\mathrm{sat}_1} = \left(\frac{\sqrt{P_{\mathrm{D}} \cdot \left(V_{\mathrm{GB_{eff}}} + \Delta_{\mathrm{acc}}\right) + {k_0}^2/4} - k_0/2}{P_{\mathrm{D}}}\right)^2 - \Delta_{\mathrm{acc}} \tag{2.10}$$

Drain Saturation Voltage:

$$V_{\mathrm{DSAT_{long}}} = \begin{cases} 0 & \text{for:} \quad \psi_{\mathrm{sat}_1} - V_{\mathrm{SB}} - \phi_{\mathrm{B}} \leq 0 \\ \psi_{\mathrm{sat}_1} - V_{\mathrm{SB}} - \phi_{\mathrm{B}} & \text{for:} \quad \psi_{\mathrm{sat}_1} - V_{\mathrm{SB}} - \phi_{\mathrm{B}} > 0 \end{cases} \tag{2.11}$$

$$T_{\mathrm{sat}} = \begin{cases} \theta_{\mathrm{sat}} & \text{for NMOS} \\ \frac{\theta_{\mathrm{sat}}}{\left(1+{\theta_{\mathrm{sat}}}^2 \cdot {V_{\mathrm{DSAT_{long}}}}^2\right)^{1/4}} & \text{for PMOS} \end{cases} \tag{2.12}$$

$$\Delta_{\mathrm{SAT}} = \frac{T_{\mathrm{sat}} - \theta_{\mathrm{R_{eff}}}}{\sqrt{\frac{2}{{V_{\mathrm{DSAT_{long}}}}^2} + {T_{\mathrm{sat}}}^2} + \theta_{\mathrm{R_{eff}}}} \tag{2.13}$$

$$V_{\mathrm{DSAT_{short}}} = V_{\mathrm{DSAT_{long}}} \cdot \left(1 - \frac{9}{10} \cdot \frac{\Delta_{\mathrm{SAT}}}{1 + \sqrt{1 - {\Delta_{\mathrm{SAT}}}^2}}\right) \tag{2.14}$$

$$V_{\mathrm{DSAT}} = \begin{cases} V_{\mathrm{limit}} & \text{for:} \quad V_{\mathrm{DSAT_{short}}} \leq V_{\mathrm{limit}} \\ V_{\mathrm{DSAT_{short}}} & \text{for:} \quad V_{\mathrm{DSAT_{short}}} > V_{\mathrm{limit}} \end{cases} \tag{2.15}$$

$$V_{\mathrm{DS_x}} = \frac{V_{\mathrm{DS}} \cdot V_{\mathrm{DSAT}}}{\left[{V_{\mathrm{DS}}}^{2m} + {V_{\mathrm{DSAT}}}^{2m} \right]^{1/2m}} \tag{2.16}$$

Surface Potential:

$$f_1\left\{\psi\right\} = \begin{cases} \psi_{\mathrm{sat_1}} & \text{for:} \quad \psi_{\mathrm{sat_1}} \leq \psi \\ \psi & \text{for:} \quad \psi_{\mathrm{sat_1}} > \psi \end{cases} \tag{2.17}$$

$$f_2\left\{\psi\right\} = f_1\{\psi\} + \frac{\psi_{\mathrm{sat_1}} - f_1\{\psi\}}{\sqrt{1 + \frac{\left[\psi_{\mathrm{sat_1}} - f_1\{\psi\}\right]^2}{N_{\phi_{\mathrm{T}}} \cdot {\phi_{\mathrm{T}}}^2}}} \tag{2.18}$$

$$f_3\left\{\psi\right\} = \frac{2 \cdot \left[V_{\mathrm{GB_{eff}}} - f_2\{\psi\}\right]}{1 + \sqrt{1 + 4/{k_{\mathrm{P}}}^2 \cdot \left[V_{\mathrm{GB_{eff}}} - f_2\{\psi\}\right]}} \tag{2.19}$$

$$\psi_{\mathrm{s_{inv}}}\left\{\psi\right\} = f_1\{\psi\} + \phi_{\mathrm{T}} \cdot [1 + m_0] \cdot \ln\left[\frac{\left[\frac{f_3\{\psi\}}{k_0}\right]^2 - f_1\{\psi\} - \Delta_{\mathrm{acc}} + \phi_{\mathrm{T}}}{\phi_{\mathrm{T}}}\right] \tag{2.20}$$

$$\begin{aligned} \psi_{\mathrm{s_0}}^* &= \psi_{\mathrm{s_{inv}}}\left\{V_{\mathrm{SB}} + \phi_{\mathrm{B}}\right\} \\ \psi_{\mathrm{s_L}}^* &= \psi_{\mathrm{s_{inv}}}\left\{V_{\mathrm{DS_x}} + V_{\mathrm{SB}} + \phi_{\mathrm{B}}\right\} \end{aligned} \tag{2.21}$$

Surface Potential in Accumulation:

$$f_1 = \begin{cases} Acc \cdot (V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}}) & \text{for:} \quad V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}} \leq 0 \\ 0 & \text{for:} \quad V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}} > 0 \end{cases} \tag{2.22}$$

$$f_2 = \frac{f_1}{\sqrt{1 + \frac{{f_1}^2}{N_{\phi_{\mathrm{T}}} \cdot {\phi_{\mathrm{T}}}^2}}} \tag{2.23}$$

$$\psi_{\mathrm{sacc}} = -\phi_{\mathrm{T}} \cdot \ln\left[\frac{\left[\frac{f_1/Acc - f_2}{k_0}\right]^2 - f_2 + \phi_{\mathrm{T}}}{\phi_{\mathrm{T}}}\right] \tag{2.24}$$

Auxiliary Variables:

$$\Delta\psi = \psi^*_{s_L} - \psi^*_{s_0} \tag{2.25}$$

$$\bar{\psi}_{inv} = \frac{\psi^*_{s_L} + \psi^*_{s_0}}{2} \tag{2.26}$$

$$V_{G_T}\left\{\psi_{s_{inv}}\right\} = \frac{2 \cdot \left[V_{GB_{eff}} - \psi_{s_{inv}}\right]}{1 + \sqrt{1 + 4/k_P{}^2 \cdot \left[V_{GB_{eff}} - \psi_{s_{inv}}\right]}} - k_0 \cdot \sqrt{\psi_{s_{inv}} + \Delta_{acc}} \tag{2.27}$$

$$\bar{V}_{G_T} = V_{G_T}\left\{\bar{\psi}_{inv}\right\} \tag{2.28}$$

$$V_{ox} = \frac{2 \cdot \left[V_{GS} + V_{SB} + \Delta V_G - V_{FB} - \bar{\psi}_{inv} - \psi_{acc}\right]}{1 + \sqrt{1 + 4/k_P{}^2 \cdot \left[V_{GB_{eff}} - \bar{\psi}_{inv}\right]}} \tag{2.29}$$

$$\partial V_{ox} = \frac{2}{1 + \sqrt{1 + 4/k_P{}^2 \cdot \left[V_{GB_{eff}} - \bar{\psi}_{inv}\right]}} \tag{2.30}$$

$$V_{eff} = \bar{V}_{G_T} + \eta_{mob} \cdot \left(V_{ox} - \bar{V}_{G_T}\right) \tag{2.31}$$

$$\xi = \phi_T \cdot \frac{\partial \bar{V}_{G_T}}{\partial \bar{\psi}_{inv}} = \phi_T \cdot \left[\frac{1}{1 + \sqrt{1 + 4/k_P{}^2 \cdot \left[V_{GB_{eff}} - \bar{\psi}_{inv}\right]}} + \frac{k_0}{2\sqrt{\bar{\psi}_{inv} + \Delta_{acc}}}\right] \tag{2.32}$$

Second-Order Effects

Mobility Degradation:

$$G_{mob} = \frac{\mu_0}{\mu} = \begin{cases} 1 + \left[\left(\theta_{ph} \cdot V_{eff}\right)^{\nu/3} + \left(\theta_{sr} \cdot V_{eff}\right)^{2\nu}\right]^{1/\nu} & \text{for NMOS} \\ \left[1 + \left(\theta_{ph} \cdot V_{eff}\right)^{\nu/3} + \left(\theta_{sr} \cdot V_{eff}\right)^{\nu}\right]^{1/\nu} & \text{for PMOS} \end{cases} \tag{2.33}$$

Velocity Saturation:

$$x = \begin{cases} \frac{2 \cdot \theta_{sat} \cdot \Delta\psi}{\sqrt{G_{mob}}} & \text{for NMOS} \\ \frac{2 \cdot \theta_{sat}}{\sqrt{G_{mob}}} \cdot \frac{\Delta\psi}{\left(1 + \theta_{sat}{}^2 \cdot \Delta\psi^2\right)^{1/4}} & \text{for PMOS} \end{cases} \tag{2.34}$$

$$G_{vsat} = \frac{G_{mob}}{2} \cdot \left[\sqrt{1 + x^2} + \frac{\ln\left(x + \sqrt{1 + x^2}\right)}{x}\right] \tag{2.35}$$

Channel Length Modulation:

$$G_{\Delta L} = 1 - \frac{\Delta L}{L} = 1 - \alpha \cdot \ln\left[\frac{V_{DS} - V_{DS_x} + \sqrt{\left(V_{DS} - V_{DS_x}\right)^2 + {V_P}^2}}{V_P}\right] \tag{2.36}$$

Series Resistance + Self-Heating:

$$G_R = \theta_R \cdot \left(1 + \frac{\theta_{R1}}{\theta_{R2} + \bar{V}_{G_T}}\right) \cdot \bar{V}_{G_T} \tag{2.37}$$

$$G_{Th} = \theta_{Th} \cdot V_{DS} \cdot \Delta\psi \cdot \bar{V}_{G_T} \tag{2.38}$$

$$G_{tot} = G_{Th} + \frac{\left[G_{\Delta L} \cdot G_{vsat} + G_R\right]}{2} \cdot$$

$$\cdot \left[1 + \sqrt{1 - \frac{4 \cdot G_R / G_{vsat}}{\left[G_{\Delta L} \cdot G_{vsat} + G_R\right]^2} \cdot \left({G_{vsat}}^2 - {G_{mob}}^2\right)}\right] \tag{2.39}$$

Inversion-Layer Charge ($Q_{inv} = -\epsilon_{ox} / t_{ox} \cdot V_{inv}$):

$$V_{inv}\left\{\psi_{s_{inv}}, \psi\right\} = \frac{k_0 \cdot \phi_T \cdot \exp\left[\frac{\psi_{s_{inv}} - \psi}{[1+m_0] \cdot \phi_T}\right]}{\sqrt{\psi_{s_{inv}} + \Delta_{acc} + \phi_T \cdot \exp\left[\frac{\psi_{s_{inv}} - \psi}{[1+m_0] \cdot \phi_T}\right]} + \sqrt{\psi_{s_{inv}} + \Delta_{acc}}} \tag{2.40}$$

$$V_{inv_0} = V_{inv}\left\{\psi^*_{s_0}, V_{SB} + \phi_B\right\} \tag{2.41}$$

$$V_{inv_L} = V_{inv}\left\{\psi^*_{s_L}, V_{DS_x} + V_{SB} + \phi_B\right\} \tag{2.42}$$

Drain Current

$$I_{drift} = \beta \cdot \bar{V}_{G_T} \cdot \Delta\psi \tag{2.43}$$

$$I_{diff} = \beta \cdot \phi_T \cdot \left(V_{inv_0} - V_{inv_L}\right) \tag{2.44}$$

$$I_{DS} = \frac{I_{drift} + I_{diff}}{G_{tot}} \tag{2.45}$$

Weak-Avalanche:

$$I_{avl} = \begin{cases} 0 & \text{for:} \quad V_{DS} \le a_3 \cdot V_{DSAT} \\ a_1 \cdot I_{DS} \cdot \exp\left(-\frac{a_2}{V_{DS} - a_3 \cdot V_{DSAT}}\right) & \text{for:} \quad V_{DS} > a_3 \cdot V_{DSAT} \end{cases} \tag{2.46}$$

Gate Current Equations:

The tunnelling probability is given by:

$$P_{\mathrm{tun}}\{V_{\mathrm{ox}};\chi_{\mathrm{B}};B\} = \begin{cases} \exp\left(-B\cdot\frac{\left[1-\left(1-V_{\mathrm{ox}}/\chi_{\mathrm{B}}\right)^{\frac{3}{2}}\right]}{V_{\mathrm{ox}}}\right) & \text{for:} \quad V_{\mathrm{ox}} < \chi_{\mathrm{B}} \\ \exp\left(-B\big/V_{\mathrm{ox}}\right) & \text{for:} \quad V_{\mathrm{ox}} \geq \chi_{\mathrm{B}} \end{cases} \tag{2.47}$$

Source/Drain Gate Overlap Current: First calculate the oxide voltage V_{ov} at both Source and Drain overlap:

$$V_{\mathrm{GX_{eff}}}\{V_{\mathrm{GX}}\} = \begin{cases} V_{\mathrm{GX}} - V_{\mathrm{FBov}} & \text{for:} \quad V_{\mathrm{GX}} - V_{\mathrm{FBov}} \leq 0 \\ 0 & \text{for:} \quad V_{\mathrm{GX}} - V_{\mathrm{FBov}} > 0 \end{cases} \tag{2.48}$$

$$\Delta_{\mathrm{ov}}\{V_{\mathrm{GX}}\} = \phi_{\mathrm{T}}\cdot\left[\exp\left[\frac{Acc_{\mathrm{ov}}\cdot V_{\mathrm{GX_{eff}}}\{V_{\mathrm{GX}}\}}{\phi_{\mathrm{T}}}\right]-1\right] \tag{2.49}$$

$$\psi_{\mathrm{sat_{ov}}}\{V_{\mathrm{GX}}\} = -\left[\sqrt{\frac{k_{\mathrm{ov}}{}^2}{4} - V_{\mathrm{GX_{eff}}}\{V_{\mathrm{GX}}\} + \Delta_{\mathrm{ov}}\{V_{\mathrm{GX}}\}} - \frac{k_{\mathrm{ov}}}{2}\right]^2 + \Delta_{\mathrm{ov}}\{V_{\mathrm{GX}}\} \tag{2.50}$$

$$f_1\{V_{\mathrm{GX}}\} = \begin{cases} 0 & \text{for:} \quad V_{\mathrm{GX}} - V_{\mathrm{FBov}} \leq 0 \\ Acc_{\mathrm{ov}}\cdot\left[V_{\mathrm{GX}} - V_{\mathrm{FBov}}\right] & \text{for:} \quad V_{\mathrm{GX}} - V_{\mathrm{FBov}} > 0 \end{cases} \tag{2.51}$$

$$f_2\{V_{\mathrm{GX}}\} = \frac{f_1\{V_{\mathrm{GX}}\}}{\sqrt{1+\frac{\left[f_1\{V_{\mathrm{GX}}\}\right]^2}{N_{\phi_{\mathrm{T}}}\cdot\phi_{\mathrm{T}}{}^2}}} \tag{2.52}$$

$$f_3\{V_{\mathrm{GX}}\} = \frac{2\cdot\left[\frac{f_1\{V_{\mathrm{GX}}\}}{Acc_{\mathrm{ov}}} - f_2\{V_{\mathrm{GX}}\}\right]}{1+\sqrt{1+4/k_{\mathrm{P}}{}^2\cdot\left[\frac{f_1\{V_{\mathrm{GX}}\}}{Acc_{\mathrm{ov}}} - f_2\{V_{\mathrm{GX}}\}\right]}} \tag{2.53}$$

$$\psi^*_{\mathrm{s_{ov}}}\{V_{\mathrm{GX}}\} = \phi_{\mathrm{T}}\cdot\ln\left[\frac{\left[\frac{f_3\{V_{\mathrm{GX}}\}}{k_{\mathrm{ov}}}\right]^2 + f_2\{V_{\mathrm{GX}}\} + \phi_{\mathrm{T}}}{\phi_{\mathrm{T}}}\right] \tag{2.54}$$

$$V_{\mathrm{ov}}\{V_{\mathrm{GX}}\} = \frac{2\cdot\left[V_{\mathrm{GX}} - V_{\mathrm{FBov}} - \psi^*_{\mathrm{s_{ov}}}\{V_{\mathrm{GX}}\} - \psi_{\mathrm{sat_{ov}}}\{V_{\mathrm{GX}}\}\right]}{1+\sqrt{1+4/k_{\mathrm{P}}{}^2\cdot\left[f_1\{V_{\mathrm{GX}}\}/Acc_{\mathrm{ov}} - \psi^*_{\mathrm{s_{ov}}}\{V_{\mathrm{GX}}\}\right]}} \tag{2.55}$$

$$V_{\mathrm{ov_0}} = V_{\mathrm{ov}}\{V_{\mathrm{GS}}\} \tag{2.56}$$

$$V_{\mathrm{ov_L}} = V_{\mathrm{ov}}\{V_{\mathrm{GS}} - V_{\mathrm{DS}}\} \tag{2.57}$$

Next calculate the gate tunnelling current in both Source and Drain overlap:

$$P_{\rm ov}\left\{V_{\rm ov}\right\} = P_{\rm tun}\left\{V_{\rm ov};\, \chi_{\rm B_{inv}};\, B_{\rm inv}\right\} \tag{2.58}$$

$$I_{\rm Gov}\left\{V_{\rm GX}, V_{\rm ov}\right\} = I_{\rm GOV}\cdot V_{\rm GX}\cdot V_{\rm ov}\cdot\left[P_{\rm ov}\left\{V_{\rm ov}\right\} - P_{\rm ov}\left\{-V_{\rm ov}\right\}\right] \tag{2.59}$$

$$I_{\rm Gov_0} = I_{\rm Gov}\left\{V_{\rm GS}\ ,\ V_{\rm ov_0}\right\} \tag{2.60}$$

$$I_{\rm Gov_L} = I_{\rm Gov}\left\{V_{\rm GS} - V_{\rm DS}\ ,\ V_{\rm ov_L}\right\} \tag{2.61}$$

Intrinsic Gate Current: The gate tunnelling current in accumulation:

$$P_{\rm acc} = P_{\rm tun}\left\{-V_{\rm ox};\, \chi_{\rm B_{acc}};\, B_{\rm acc}\right\} \tag{2.62}$$

$$I_{\rm GB} = \begin{cases} -I_{\rm GACC}\cdot\left(V_{\rm GS} + V_{\rm SB}\right)\cdot V_{\rm ox}\cdot P_{\rm acc} & \text{for:}\quad V_{\rm ox}\le 0 \\ 0 & \text{for:}\quad V_{\rm ox} > 0 \end{cases} \tag{2.63}$$

The tunnelling current in inversion, including quantum-mechanical barrier lowering $\Delta\chi_{\rm B}$:

$$\Delta\chi_{\rm B} = QM_{\psi}\cdot\left(\bar{V}_{\rm G_T}\big/ 3 + V_{\rm ox} - \bar{V}_{\rm G_T}\right)^{2/3} \tag{2.64}$$

$$\chi_{\rm B_{eff}} = \chi_{\rm B_{inv}} - \Delta\chi_{\rm B} \tag{2.65}$$

$$B_{\rm eff} = B_{\rm inv}\cdot\left(\chi_{\rm B_{eff}}\big/\chi_{\rm B_{inv}}\right)^{3/2} \tag{2.66}$$

$$P_{\rm inv} = P_{\rm tun}\left\{V_{\rm ox};\, \chi_{\rm B_{eff}};\, B_{\rm eff}\right\} \tag{2.67}$$

$$B^*_{\rm inv} = \frac{3}{8}\cdot{\chi_{\rm B_{eff}}}^{-2}\cdot B_{\rm eff}\cdot\partial V_{\rm ox} \tag{2.68}$$

$$\xi^* = \frac{\xi}{\phi_{\rm T}\cdot\bar{V}^*_{\rm G_T}} \tag{2.69}$$

$$\partial V^*_{\rm ox} = \frac{\partial V_{\rm ox}}{V_{\rm ox}} \tag{2.70}$$

$$P_{\rm GC} = 1 + \frac{\left[{B^*_{\rm inv}}^2 + 4\cdot B^*_{\rm inv}\cdot\xi^* + 2\cdot B^*_{\rm inv}\cdot\partial V^*_{\rm ox} + 2\cdot\xi^{*2} + 4\cdot\partial V^*_{\rm ox}\cdot\xi^*\right]\cdot\Delta\psi^2}{24} \tag{2.71}$$

$$\bar{I}_{\rm GC} = I_{\rm GINV}\cdot G_{\Delta\rm L}\cdot\left(V_{\rm GS} - \frac{1}{2}V_{\rm DS_X}\right)\cdot P_{\rm inv} \tag{2.72}$$

$$\bar{V}_{\rm inv} = \frac{V_{\rm inv_0} + V_{\rm inv_L}}{2} \tag{2.73}$$

The total intrinsic gate current I_{GC}:

$$I_{\mathrm{GC}} = \bar{I}_{\mathrm{GC}} \cdot \bar{V}_{\mathrm{inv}} \cdot P_{\mathrm{GC}} \tag{2.74}$$

$$P_{\mathrm{GS}} = \left[B_{\mathrm{inv}}^* + \partial V_{\mathrm{ox}}^*\right] \cdot \frac{\Delta\psi}{12} + \left[{B_{\mathrm{inv}}^*}^2 \cdot \left(B_{\mathrm{inv}}^* + 5 \cdot \xi^* + 3 \cdot \partial V_{\mathrm{ox}}^*\right)\right.$$

$$\left. + 2 \cdot \xi^{*2} \cdot \left(B_{\mathrm{inv}}^* - \xi^* + \partial V_{\mathrm{ox}}^*\right) + 10 \cdot B_{\mathrm{inv}}^* \cdot \xi^* \cdot \partial V_{\mathrm{ox}}^*\right] \cdot \frac{\Delta\psi^3}{480} \tag{2.75}$$

$$I_{\mathrm{GS}} = \frac{1}{2} \cdot I_{\mathrm{GC}} + \left(P_{\mathrm{GS}} \cdot \bar{V}_{\mathrm{inv}} + \frac{V_{\mathrm{inv}_0} - V_{\mathrm{inv}_\mathrm{L}}}{12}\right) \cdot \bar{I}_{\mathrm{GC}} + I_{\mathrm{Gov}_0} \tag{2.76}$$

$$I_{\mathrm{GD}} = I_{\mathrm{GC}} - I_{\mathrm{GS}} + I_{\mathrm{Gov}_0} + I_{\mathrm{Gov}_\mathrm{L}} \tag{2.77}$$

2.2.3 Basic Charge Equations

Bias-Dependent Overlap Capacitance:

$$Q_{\mathrm{ov}_0} = C_{\mathrm{GSO}} \cdot V_{\mathrm{ov}_0} \tag{2.78}$$

$$Q_{\mathrm{ov}_\mathrm{L}} = C_{\mathrm{GDO}} \cdot V_{\mathrm{ov}_\mathrm{L}} \tag{2.79}$$

Intrinsic Charges:

$$C_{\mathrm{ox}_{\mathrm{eff}}} = \frac{C_{\mathrm{ox}}}{1 + QM_{\mathrm{tox}} \cdot \left[\frac{V_{\mathrm{eff}}}{\eta_{\mathrm{mob}}}\right]^{-1/3}} \tag{2.80}$$

$$V_{\mathrm{GT}_0} = V_{\mathrm{G_T}}\left\{\psi_{\mathrm{s}_0}^*\right\} \tag{2.81}$$

$$V_{\mathrm{GT}_\mathrm{L}} = V_{\mathrm{G_T}}\left\{\psi_{\mathrm{s}_\mathrm{L}}^*\right\} \tag{2.82}$$

$$\bar{V}_{\mathrm{G_T}}^* = \frac{V_{\mathrm{GT}_0} + V_{\mathrm{GT}_\mathrm{L}}}{2} + \xi \tag{2.83}$$

$$\Delta V_{\mathrm{G_T}} = \frac{V_{\mathrm{GT}_0} - V_{\mathrm{GT}_\mathrm{L}}}{2 \cdot \left(1 + \theta_{\mathrm{R}} \cdot \frac{\bar{V}_{\mathrm{G_T}}^*}{G_{\mathrm{tot}}}\right)} \tag{2.84}$$

$$F_{\mathrm{j}} = \frac{\Delta V_{\mathrm{G_T}}}{\bar{V}_{\mathrm{G_T}}^*} \tag{2.85}$$

$$Q_{\mathrm{S}} = -\frac{C_{\mathrm{ox}_{\mathrm{eff}}}}{2} \cdot \left[\bar{V}_{\mathrm{G_T}}^* + \frac{\Delta V_{\mathrm{G_T}}}{3} \cdot \left(F_{\mathrm{j}} - \frac{{F_{\mathrm{j}}}^2}{5} + 1\right) - \xi\right] \tag{2.86}$$

$$Q_{\mathrm{D}} = -\frac{C_{\mathrm{ox_{eff}}}}{2} \cdot \left[\bar{V}^{*}_{\mathrm{G_T}} + \frac{\Delta V_{\mathrm{G_T}}}{3} \cdot \left(F_{\mathrm{j}} + \frac{F_{\mathrm{j}}{}^{2}}{5} - 1 \right) - \xi \right] \tag{2.87}$$

$$Q_{\mathrm{B}} = -C_{\mathrm{ox_{eff}}} \cdot \left[V_{\mathrm{ox}} - \bar{V}^{*}_{\mathrm{G_T}} + \xi \right] \tag{2.88}$$

$$Q_{\mathrm{G}} = -\left[Q_{\mathrm{S}} + Q_{\mathrm{D}} + Q_{\mathrm{B}} \right] \tag{2.89}$$

2.2.4 Basic Noise Equations

In these equations f represents the operation frequency of the transistor.

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}} \tag{2.90}$$

$$T_{\mathrm{sat}} = \begin{cases} \theta_{\mathrm{sat}}{}^{2} & \text{for NMOS} \\ \frac{\theta_{\mathrm{sat}}{}^{2}}{\sqrt{1+\theta_{\mathrm{sat}}{}^{2}\cdot\Delta\psi^{2}}} & \text{for PMOS} \end{cases} \tag{2.91}$$

$$R_{\mathrm{ideal}} = \frac{\beta \cdot G_{\mathrm{vsat}}{}^{2}}{G_{\mathrm{tot}}} \cdot \left[\bar{V}_{\mathrm{G_T}} + \frac{\frac{\Delta\psi^{2}}{12} - \xi \cdot \left(\bar{V}_{\mathrm{G_T}} - \frac{V_{\mathrm{inv_0}} + V_{\mathrm{inv_L}}}{2} \right)}{\bar{V}_{\mathrm{G_T}} + \xi} \right] \tag{2.92}$$

$$S_{\mathrm{th}} = \frac{N_{\mathrm{T}}}{G_{\mathrm{mob}}{}^{2}} \cdot \left(R_{\mathrm{ideal}} - T_{\mathrm{sat}} \cdot I_{\mathrm{DS}} \cdot \Delta\psi \right) \tag{2.93}$$

$$N_0 = \frac{\epsilon_{ox}}{q t_{ox}} \cdot V_{\mathrm{inv_0}} \tag{2.94}$$

$$N_L = \frac{\epsilon_{ox}}{q t_{ox}} \cdot V_{\mathrm{inv_L}} \tag{2.95}$$

$$N^{*} = \frac{\epsilon_{ox}}{q t_{ox}} \cdot \xi \tag{2.96}$$

$$\begin{aligned} S_{\mathrm{fl}} = \frac{q \cdot \phi_{\mathrm{T}}{}^{2} \cdot t_{ox} \cdot \beta \cdot I_{\mathrm{DS}}}{f \cdot \epsilon_{ox} \cdot G_{\mathrm{mob}} \cdot N^{*}} \cdot \Bigg[& \left(N_{\mathrm{FA}} - N^{*} \cdot N_{\mathrm{FB}} + N^{*2} \cdot N_{\mathrm{FC}} \right) \cdot \ln \frac{N_0 + N^{*}}{N_L + N^{*}} \\ & + \left(N_{\mathrm{FB}} - N^{*} \cdot N_{\mathrm{FC}} \right) \cdot \left(N_0 - N_L \right) + \frac{N_{\mathrm{FC}}}{2} \cdot \left(N_0{}^{2} - N_L{}^{2} \right) \Bigg] \\ & + \frac{\phi_{\mathrm{T}} \cdot I_{\mathrm{DS}}{}^{2}}{f} \cdot \left(1 - G_{\Delta L} \right) \cdot \left[\frac{N_{\mathrm{FA}} + N_{\mathrm{FB}} \cdot N_L + N_{\mathrm{FC}} \cdot N_L{}^{2}}{\left(N_L + N^{*} \right)^{2}} \right] \end{aligned} \tag{2.97}$$

$$S_{\mathrm{ig}} = \begin{cases} \frac{\frac{1}{3}\cdot N_{\mathrm{T}} \cdot \left(2\cdot\pi\cdot f\cdot C_{\mathrm{ox}} \right)^{2} / g_{\mathrm{m}}}{1+0.075\cdot\left(2\cdot\pi\cdot f\cdot C_{\mathrm{ox}} / g_{\mathrm{m}} \right)^{2}} & \text{for:} \quad \mathrm{GATENOISE} = 0 \\ 0 & \text{for:} \quad \mathrm{GATENOISE} = 1 \end{cases} \tag{2.98}$$

$$\rho_{\mathrm{igth}} = 0.4\mathrm{j} \tag{2.99}$$

$$S_{\mathrm{igth}} = \rho_{\mathrm{igth}} \cdot \sqrt{S_{\mathrm{ig}} \cdot S_{\mathrm{th}}} \tag{2.100}$$

3 Nomenclature

3.1 General Remarks

The symbolic representation and the recommended programming names of the quantities listed in the following sections, have been chosen in such a way to express their purpose and relations to other quantities and to preclude ambiguity and inconsistency.

All parameters which refer to the reference transistor and/or the reference temperature have a symbol with the subscript R and a programming name ending with R. All characters 0 (zero) in subscripts of parameters are represented by the capital letter O in the programming name, because often they are distinguishable with great difficulty! Scaling parameters are indicated by S with a subscript where the variables on which the parameter depends, precede a semicolon whereas the parameter succeeds it, e.g. $S_{\mathrm{T};\theta_{\mathrm{S}r}}$.

Note: Since the list of parameters for an individual transistor (i.e. the so-called miniset parameters) and the list of physical constants can be found in Sections 2.1.1 and 2.1.2, respectively, they will not be repeated here.

3.2 List of Input Variables

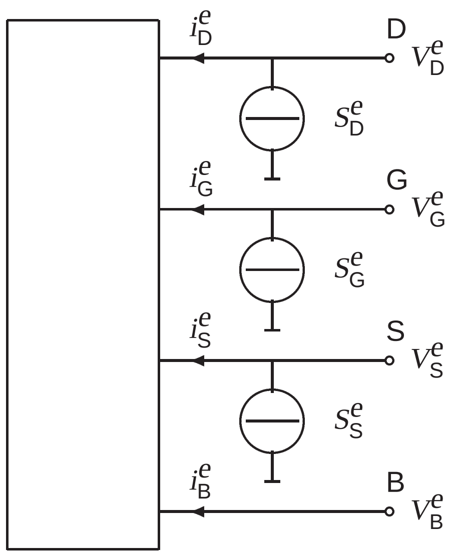
No.	Symbol	Program Name	Units	Description
1	L	L	m	Drawn channel length in the lay-out of the actual transistor
2	W	W	m	Drawn channel width in the lay-out of the actual transistor
3	T_{A}	TA	^{o}C	Ambient circuit temperature
4	f	F	s^{-1}	Operation frequency

3.3 List of Electrical Quantities and Variables

For the electrical quantities and variables, the distinction is made between external, referring to the nodes of the physical device, and internal, referring to their use in the model equations.

3.3.1 External Electrical Quantities and Variables

The definitions of the external electrical variables are illustrated in fig.3.1.



$$i^e_{\mathrm{D}} = I^e_{\mathrm{D}} + \frac{\mathrm{d}Q^e_{\mathrm{D}}}{\mathrm{d}t}$$

$$i^e_{\mathrm{G}} = I^e_{\mathrm{G}} + \frac{\mathrm{d}Q^e_{\mathrm{G}}}{\mathrm{d}t}$$

$$i^e_{\mathrm{S}} = I^e_{\mathrm{S}} + \frac{\mathrm{d}Q^e_{\mathrm{S}}}{\mathrm{d}t}$$

$$i^e_{\mathrm{B}} = I^e_{\mathrm{B}} + \frac{\mathrm{d}Q^e_{\mathrm{B}}}{\mathrm{d}t}$$

Figure 3.1: Definition of the external electrical quantities and variables

No.	Variable	Program Name	Units	Description
1	V_{D}^{e}	VDE	V	Potential applied to the drain node
2	V_{G}^{e}	VGE	V	Potential applied to the gate node
3	V_{S}^{e}	VSE	V	Potential applied to the source node
4	V_{B}^{e}	VBE	V	Potential applied to the bulk node
5	I_{D}^{e}	IDE	A	DC current into the drain
6	I_{G}^{e}	IGE	A	DC current into the gate
7	I_{S}^{e}	ISE	A	DC current into the source
8	I_{B}^{e}	IBE	A	DC current into the bulk
9	Q_{D}^{e}	QDE	C	Charge in the device attributed to the drain node
10	Q_{G}^{e}	QGE	C	Charge in the device attributed to the gate node
11	Q_{S}^{e}	QSE	C	Charge in the device attributed to the source node
12	Q_{B}^{e}	QBE	C	Charge in the device attributed to the bulk node
13	S_{D}^{e}	SDE	A^2s	Spectral density of the noise current into the drain
14	S_{G}^{e}	SGE	A^2s	Spectral density of the noise current into the gate
15	S_{S}^{e}	SSE	A^2s	Spectral density of the noise current into the source
16	S_{DG}^{e}	SDGE	A^2s	Cross spectral density between the drain and the gate noise currents
17	S_{GS}^{e}	SGSE	A^2s	Cross spectral density between the gate and the source noise currents
18	S_{SD}^{e}	SSDE	A^2s	Cross spectral density between the source and the drain noise currents

3.3.2 Internal Electrical Quantities and Variables

No.	Variable	Program Name	Units	Description
1	V_{DS}	VDS	V	Drain–to–source voltage applied to the equivalent n–MOST
2	V_{GS}	VGS	V	Gate–to–source voltage applied to the equivalent n–MOST
3	V_{SB}	VSB	V	Source–to–bulk voltage applied to the equivalent n–MOST
4	I_{DS}	IDS	A	DC current through the channel flowing from drain to source
5	I_{AVL}	IAVL	A	DC current flowing from drain to bulk due to the weak–avalanche effect
6	I_{GS}	IGS	A	DC current flowing from gate to source due to the direct tunnelling effect
7	I_{GD}	IGD	A	DC current flowing from gate to drain due to the direct tunnelling effect
8	I_{GB}	IGB	A	DC current flowing from gate to bulk due to the direct tunnelling effect
9	Q_{D}	QD	C	Intrinsic charge in the equivalent n–MOST attributed to the drain node
10	Q_{G}	QG	C	Intrinsic charge in the equivalent n–MOST attributed to the gate node
11	Q_{S}	QS	C	Intrinsic charge in the equivalent n–MOST attributed to the source node
12	Q_{B}	QB	C	Intrinsic charge in the equivalent n–MOST attributed to the bulk node
13	Q_{ov_0}	QOVO	C	Extrinsic charge in the equivalent n–MOST attributed to the gate-source overlap
14	Q_{ov_L}	QOVL	C	Extrinsic charge in the equivalent n–MOST attributed to the gate-drain overlap
15	S_{th}	STH	$\mathrm{A^2s}$	Spectral density of the thermal–noise current of the channel
16	S_{fl}	SFL	$\mathrm{A^2s}$	Spectral density of the flicker–noise current of the channel
17	S_{ig}	SIG	$\mathrm{A^2s}$	Spectral density of the noise current induced in the gate
18	S_{igth}	SIGTH	$\mathrm{A^2s}$	Cross spectral density of the noise current induced in the gate and the thermal–noise current of the channel

3.4 List of Reference & Scaling Parameters

No.	Symbol	Program Name	Units	Description
0		LEVEL	-	Must be 1100
1	L_{ER}	LER	m	Effective channel length of the reference transistor
2	W_{ER}	WER	m	Effective channel width of the reference transistor
3	ΔL_{PS}	LVAR	m	Difference between the actual and the programmed poly–silicon gate length
4	$\Delta L_{\mathrm{overlap}}$	LAP	m	Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions
5	ΔW_{OD}	WVAR	m	Difference between the actual and the programmed field–oxide opening
6	$\Delta W_{\mathrm{narrow}}$	WOT	m	Effective reduction of the channel width per side due to the lateral diffusion of the channel–stop dopant ions
7	T_{R}	TR	^{o}C	Temperature at which the parameters for the reference transistor have been determined
8	V_{FBR}	VFBR	V	Flat-band voltage for the reference transistor at the reference temperature
9	$S_{\mathrm{T};V_{\mathrm{FB}}}$	STVFB	VK^{-1}	Coefficient of the temperature dependence of V_{FB}
10	$k_{0\mathrm{R}}$	KOR	V$^{1/2}$	Body-effect factor for the reference transistor
11	$S_{\mathrm{L};k_0}$	SLKO	V$^{1/2}$m	Coefficient of the length dependence of k_0
12	$S_{\mathrm{L2};k_0}$	SL2KO	V$^{1/2}$m^2	Second coefficient of the length dependence of k_0
13	$S_{\mathrm{W};k_0}$	SWKO	V$^{1/2}$m	Coefficient of the width dependence of k_0
14	$1/k_{\mathrm{P}}$	KPINV	V$^{-1/2}$	Inverse of body-effect factor of the poly-silicon gate
15	ϕ_{BR}	PHIBR	V	Surface potential at the onset of strong inversion at the reference temperature
16	$S_{\mathrm{L};\phi_{\mathrm{B}}}$	SLPHIB	Vm	Coefficient of the length dependence of ϕ_{B}
17	$S_{\mathrm{L2};\phi_{\mathrm{B}}}$	SL2PHIB	Vm^2	Second coefficient of the length dependence of ϕ_{B}
18	$S_{\mathrm{W};\phi_{\mathrm{B}}}$	SWPHIB	Vm	Coefficient of the width dependence of ϕ_{B}
19	β_{sq}	BETSQ	AV^{-2}	Gain factor for an infinite square transistor at the reference temperature
20	η_β	ETABET	-	Exponent of the temperature dependence of the gain factor
21	$f_{\beta,1}$	FBET1	-	Relative mobility decrease due to first lateral profile
22	$L_{\mathrm{P},1}$	LP1	m	Characteristic length of first lateral profile
23	$f_{\beta,2}$	FBET2	-	Relative mobility decrease due to second lateral profile
24	$L_{\mathrm{P},2}$	LP2	m	Characteristic length of second lateral profile

No.	Symbol	Program Name	Units	Description
25	θ_{srR}	THESRR	V^{-1}	Coefficient of the mobility reduction due to surface roughness scattering for the reference transistor at the reference temperature
26	$S_{\mathrm{W};\theta_{\mathrm{sr}}}$	SWTHESR	m	Coefficient of the width dependence of θ_{sr}
27	θ_{phR}	THEPHR	V^{-1}	Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature
28	η_{ph}	ETAPH	-	Exponent of the temperature dependence of θ_{ph} for the reference transistor
29	$S_{\mathrm{W};\theta_{\mathrm{ph}}}$	SWTHEPH	m	Coefficient of the width dependence of θ_{ph}
30	η_{mobR}	ETAMOBR	-	Effective field parameter for dependence on depletion/inversion charge for the reference transistor
31	$S_{\mathrm{T};\eta_{\mathrm{mob}}}$	STETAMOB	K^{-1}	Coefficient of the temperature dependence of η_{mob}
32	$S_{\mathrm{W};\eta_{\mathrm{mob}}}$	SWETAMOB	m	Coefficient of the width dependence of η_{mob}
33	ν_{R}	NUR	-	Exponent of the field dependence of the mobility model minus 1 (i.e. $\nu - 1$) at the reference temperature
34	ν_{EXP}	NUEXP	-	Exponent of the temperature dependence of parameter ν
35	θ_{RR}	THERR	V^{-1}	Coefficient of the series resistance for the reference transistor at the reference temperature
36	η_{R}	ETAR	-	Exponent of the temperature dependence of θ_{R}
37	$S_{\mathrm{W};\theta_{\mathrm{R}}}$	SWTHER	m	Coefficient of the width dependence of θ_{R}
38	θ_{R1}	THER1	V	Numerator of the gate voltage dependent part of series resistance for the reference transistor
39	θ_{R2}	THER2	V	Denominator of the gate voltage dependent part of series resistance for the reference transistor
40	θ_{satR}	THESATR	V^{-1}	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature
41	$S_{\mathrm{L};\theta_{\mathrm{sat}}}$	SLTHESAT	-	Coefficient of the length dependence of θ_{sat}
42	θ_{satEXP}	THESATEXP	-	Exponent of the length dependence of θ_{sat}
43	η_{sat}	ETASAT	-	Exponent of the temperature dependence of θ_{sat}
44	$S_{\mathrm{W};\theta_{\mathrm{sat}}}$	SWTHESAT	m	Coefficient of the width dependence of θ_{sat}
45	θ_{ThR}	THETHR	V^{-3}	Coefficient of self-heating for the reference transistor at the reference temperature
46	θ_{ThEXP}	THETHEXP	-	Exponent of the length dependence of θ_{Th}
47	$S_{\mathrm{W};\theta_{\mathrm{Th}}}$	SWTHETH	m	Coefficient of the width dependence of θ_{Th}
48	σ_{dibl0}	SDIBLO	$\mathrm{V}^{-1/2}$	Drain-induced barrier-lowering parameter for the reference transistor
49	$\sigma_{\mathrm{diblEXP}}$	SDIBLEXP	-	Exponent of the length dependence of σ_{dibl}

No.	**Symbol**	**Program Name**	**Units**	**Description**
50	m_{0R}	MOR	-	Parameter for short-channel subthreshold slope for the reference transistor
51	m_{0EXP}	MOEXP	-	Exponent of the length dependence of m_0
52	σ_{sfR}	SSFR	$V^{-1/2}$	Static feedback parameter for the reference transistor
53	$S_{L;\sigma_{sf}}$	SLSSF	m	Coefficient of the length dependence of σ_{sf}
54	$S_{W;\sigma_{sf}}$	SWSSF	m	Coefficient of the width dependence of σ_{sf}
55	α_R	ALPR	-	Factor of the channel length modulation for the reference transistor
56	$S_{L;\alpha}$	SLALP	-	Coefficient of the length dependence of α
57	α_{EXP}	ALPEXP	-	Exponent of the length dependence of α
58	$S_{W;\alpha}$	SWALP	m	Coefficient of the width dependence of α
59	V_P	VP	V	Characteristic voltage of the channel length modulation
60	L_{min}	LMIN	m	Minimum effective channel length in technology, used for calculation of smoothing factor m
61	a_{1R}	A1R	-	Factor of the weak–avalanche current for the reference transistor at the reference temperature
62	$S_{T;a_1}$	STA1	K^{-1}	Coefficient of the temperature dependence of a_1
63	$S_{L;a_1}$	SLA1	m	Coefficient of the length dependence of a_1
64	$S_{W;a_1}$	SWA1	m	Coefficient of the width dependence of a_1
65	a_{2R}	A2R	V	Exponent of the weak–avalanche current for the reference transistor
66	$S_{L;a_2}$	SLA2	Vm	Coefficient of the length dependence of a_2
67	$S_{W;a_2}$	SWA2	Vm	Coefficient of the width dependence of a_2
68	a_{3R}	A3R	-	Factor of the drain–source voltage above which weak–avalanche occurs, for the reference transistor
69	$S_{L;a_3}$	SLA3	m	Coefficient of the length dependence of a_3
70	$S_{W;a_3}$	SWA3	m	Coefficient of the width dependence of a_3
71	I_{GINVR}	IGINVR	AV^{-2}	Gain factor for intrinsic gate tunnelling current in inversion for the reference transistor
72	B_{inv}	BINV	V	Probability factor for intrinsic gate tunnelling current in inversion
73	I_{GACCR}	IGACCR	AV^{-2}	Gain factor for intrinsic gate tunnelling current in accumulation for the reference transistor
74	B_{acc}	BACC	V	Probability factor for intrinsic gate tunnelling current in accumulation
75	V_{FBov}	VFBOV	V	Flat-band voltage for the Source/Drain overlap extensions
76	k_{ov}	KOV	$V^{1/2}$	Body-effect factor for the Source/Drain overlap extensions

No.	Symbol	Program Name	Units	Description
77	I_{GOVR}	IGOVR	AV^{-2}	Gain factor for Source/Drain overlap gate tunnelling current for the reference transistor
78	t_{ox}	TOX	m	Thickness of the gate oxide layer
79	C_{ol}	COL	Fm^{-1}	Gate overlap capacitance per unit channel width
80	–	GATENOISE		Flag for in/exclusion of induced gate thermal noise
81	N_{TR}	NTR	J	Coefficient of the thermal noise at the actual temperature
82	N_{FAR}	NFAR	$\mathrm{V}^{-1}\mathrm{m}^{-4}$	First coefficient of the flicker noise for the reference transistor
83	N_{FBR}	NFBR	$\mathrm{V}^{-1}\mathrm{m}^{-2}$	Second coefficient of the flicker noise for the reference transistor
84	N_{FCR}	NFCR	V^{-1}	Third coefficient of the flicker noise for the reference transistor
85	L	L	m	Drawn channel length in the lay-out of the actual transistor
86	W	W	m	Drawn channel width in the lay-out of the actual transistor
87	ΔT_{A}	DTA	K	Temperature offset of the device with respect to T_{A}
88	N_{MULT}	MULT	-	Number of devices in parallel

Remark: The parameters L, W and DTA are used to calculate the electrical parameters of the actual transistor as specified in the section on parameter preprocessing.

4 Embedding

4.1 Embedding MOS Model 11 in a Circuit Simulator

In CMOS technologies both *n*– and *p*–channel MOS transistors are supported. It is convenient to use one model for both type of transistors instead of two separate models. This is accomplished by mapping a *p*–channel device with its bias conditions and parameter set onto an equivalent *n*–channel device with appropriately changed bias conditions (i.e. currents, voltages and charges) and parameters. In this way both type of transistors can be treated as an *n*–channel transistor. Nevertheless, the electrical behaviour of electrons and holes is not exactly the same (e.g. the mobility and tunnelling behaviour), and consequently slightly different equations have to be used in case of *n*– or *p*–type transistors, see Section 2.2.

As said earlier, any circuit simulator internally identifies the terminals of a MOS transistor by a number. However, designers are used to the standard terminology of source, drain, gate and bulk. Therefore, in the context of a circuit simulator it is traditionally possible to address, say, the drain of MOST number 17, even if in reality the corresponding source is at a higher potential (*n*–channel case). More strongly, most circuit simulators provide for model evaluation a so–called V_{DS}, V_{GS}, and V_{SB} based on an a priori assignment of source, drain and bulk that is independent of the actual bias conditions. Since MOS Model 11 assumes saturation occurs at the drain side of the MOSFET, the basic model cannot cope with bias conditions that correspond to $V_{DS} < 0$. Again a transformation of the bias conditions is necessary. In this case, the transformation corresponds to internally reassigning source and drain, applying the standard electrical model, and then reassigning the currents and charges to the original terminals. In MOS Model 11 care has been taken to preserve symmetry with respect to drain and source at $V_{DS} = 0$. In other words no non-singularities will occur in the higher-order derivatives at $V_{DS} = 0$.

In detail, in order to embed MOS Model 11 correctly into a circuit simulator, the following procedure, illustrated in Fig. 4.1 should be followed. We have assumed that indeed the simulator provides the nodal potentials V_D^e, V_G^e, V_S^e and V_B^e based on an a priori assignment of drain, gate, source and bulk.

Step 1 Calculate the voltages V_{DS}'', V_{GS}'' and V_{SB}'', and the additional voltages V_{DG}'' and V_{SG}''. The latter are used for calculating the charges associated with overlap capacitances.

Step 2 Based on *n*– or *p*–channel devices, calculate the modified voltages V_{DS}', V_{GS}' and V_{SB}'. From here onwards only *n*–channel behaviour needs to be considered.

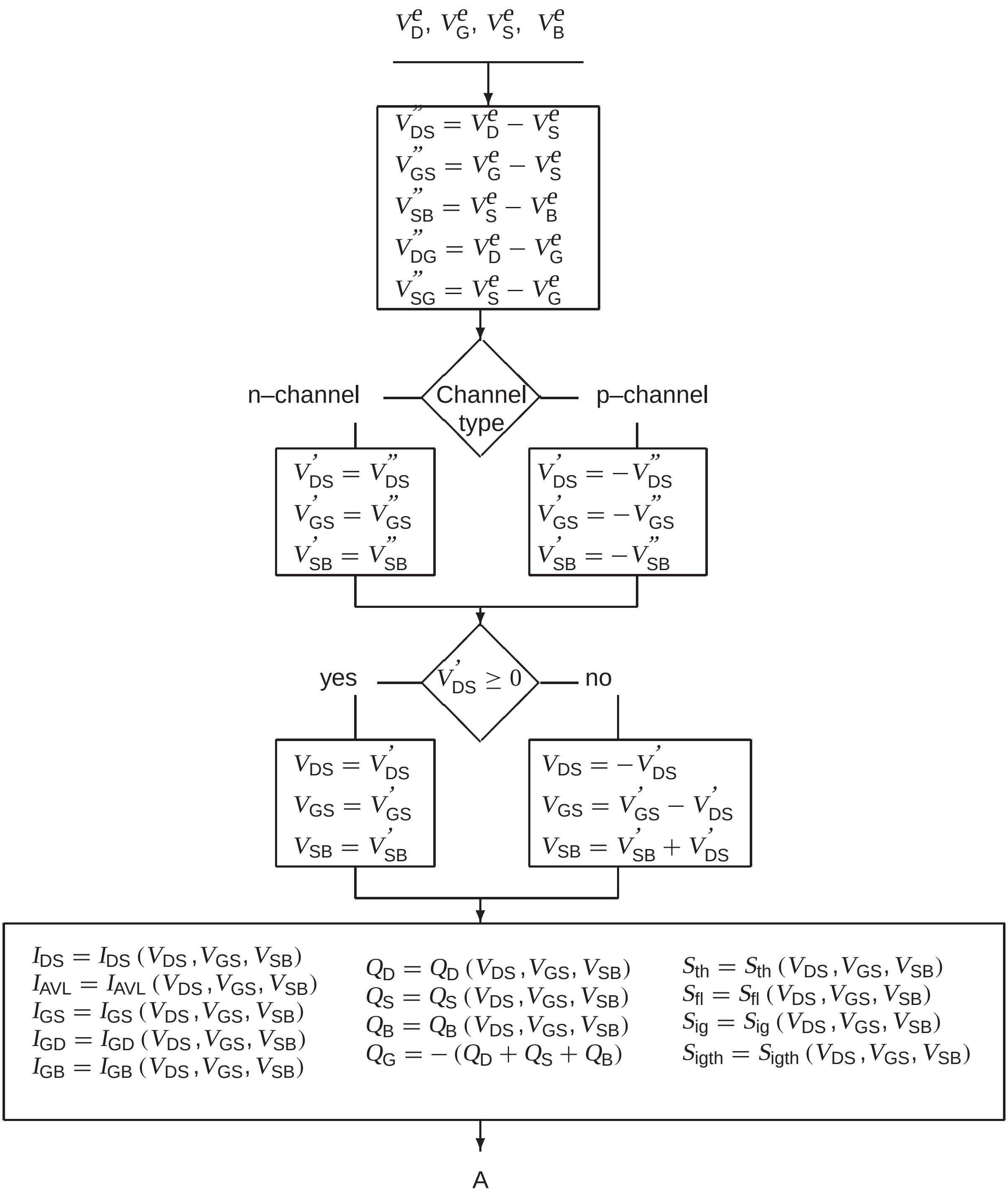
Step 3 Based on a positive or negative V_{DS}', calculate the internal nodal voltages. At this level, the voltages – and the parameters, see below – comply to all the requirements for input quantities of MOS Model 11.

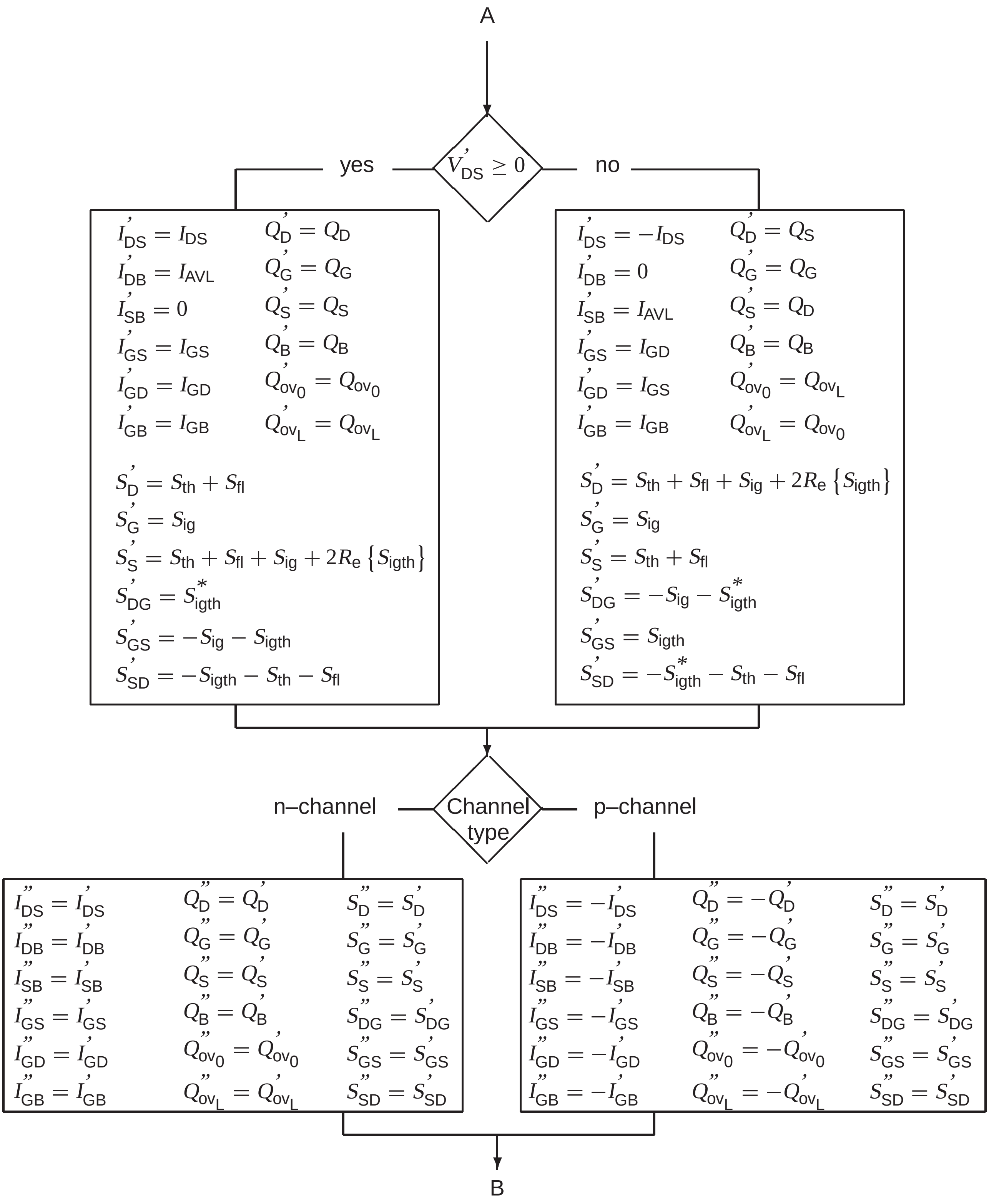
Step 4 Evaluate all the internal output quantities – channel current, weak–avalanche current, gate current, nodal charges, and noise–power spectral densities – using the standard MOS Model 11 equations and the internal voltages.

Step 5 Correct the internal output quantities for a possible source–drain interchange. In fact, this directly establishes the external noise–power spectral densities.

Step 6 Correct for a possible *p*–channel transformation.

Step 7 Change from branch current to nodal currents, establishing the external current output quantities. Calculate the overlap charges that are related to the physical regions and add them to the nodal charges, thus forming the external charge output quantities.


$V_D^e, V_G^e, V_S^e, V_B^e$
$V''_{DS} = V_D^e - V_S^e$
$V''_{GS} = V_G^e - V_S^e$
$V''_{SB} = V_S^e - V_B^e$
$V''_{DG} = V_D^e - V_G^e$
$V''_{SG} = V_S^e - V_G^e$
n–channel
Channel type
p–channel
$V'_{DS} = V''_{DS}$
$V'_{GS} = V''_{GS}$
$V'_{SB} = V''_{SB}$
$V'_{DS} = -V''_{DS}$
$V'_{GS} = -V''_{GS}$
$V'_{SB} = -V''_{SB}$
yes
$V'_{DS} \geq 0$
no
$V_{DS} = V'_{DS}$
$V_{GS} = V'_{GS}$
$V_{SB} = V'_{SB}$
$V_{DS} = -V'_{DS}$
$V_{GS} = V'_{GS} - V'_{DS}$
$V_{SB} = V'_{SB} + V'_{DS}$
$I_{DS} = I_{DS}(V_{DS}, V_{GS}, V_{SB})$
$I_{AVL} = I_{AVL}(V_{DS}, V_{GS}, V_{SB})$
$I_{GS} = I_{GS}(V_{DS}, V_{GS}, V_{SB})$
$I_{GD} = I_{GD}(V_{DS}, V_{GS}, V_{SB})$
$I_{GB} = I_{GB}(V_{DS}, V_{GS}, V_{SB})$
$Q_D = Q_D(V_{DS}, V_{GS}, V_{SB})$
$Q_S = Q_S(V_{DS}, V_{GS}, V_{SB})$
$Q_B = Q_B(V_{DS}, V_{GS}, V_{SB})$
$Q_G = -(Q_D + Q_S + Q_B)$
$S_{th} = S_{th}(V_{DS}, V_{GS}, V_{SB})$
$S_{fl} = S_{fl}(V_{DS}, V_{GS}, V_{SB})$
$S_{ig} = S_{ig}(V_{DS}, V_{GS}, V_{SB})$
$S_{igth} = S_{igth}(V_{DS}, V_{GS}, V_{SB})$
A


A
$V'_{DS} \geq 0$
yes
no
$I'_{DS} = I_{DS}$ $Q'_D = Q_D$
$I'_{DB} = I_{AVL}$ $Q'_G = Q_G$
$I'_{SB} = 0$ $Q'_S = Q_S$
$I'_{GS} = I_{GS}$ $Q'_B = Q_B$
$I'_{GD} = I_{GD}$ $Q'_{ov_0} = Q_{ov_0}$
$I'_{GB} = I_{GB}$ $Q'_{ov_L} = Q_{ov_L}$
$S'_D = S_{th} + S_{fl}$
$S'_G = S_{ig}$
$S'_S = S_{th} + S_{fl} + S_{ig} + 2R_e\{S_{igth}\}$
$S'_{DG} = S^*_{igth}$
$S'_{GS} = -S_{ig} - S_{igth}$
$S'_{SD} = -S_{igth} - S_{th} - S_{fl}$
$I'_{DS} = -I_{DS}$ $Q'_D = Q_S$
$I'_{DB} = 0$ $Q'_G = Q_G$
$I'_{SB} = I_{AVL}$ $Q'_S = Q_D$
$I'_{GS} = I_{GD}$ $Q'_B = Q_B$
$I'_{GD} = I_{GS}$ $Q'_{ov_0} = Q_{ov_L}$
$I'_{GB} = I_{GB}$ $Q'_{ov_L} = Q_{ov_0}$
$S'_D = S_{th} + S_{fl} + S_{ig} + 2R_e\{S_{igth}\}$
$S'_G = S_{ig}$
$S'_S = S_{th} + S_{fl}$
$S'_{DG} = -S_{ig} - S^*_{igth}$
$S'_{GS} = S_{igth}$
$S'_{SD} = -S^*_{igth} - S_{th} - S_{fl}$
Channel type
n–channel
p–channel
$I''_{DS} = I'_{DS}$ $Q''_D = Q'_D$ $S''_D = S'_D$
$I''_{DB} = I'_{DB}$ $Q''_G = Q'_G$ $S''_G = S'_G$
$I''_{SB} = I'_{SB}$ $Q''_S = Q'_S$ $S''_S = S'_S$
$I''_{GS} = I'_{GS}$ $Q''_B = Q'_B$ $S''_{DG} = S'_{DG}$
$I''_{GD} = I'_{GD}$ $Q''_{ov_0} = Q'_{ov_0}$ $S''_{GS} = S'_{GS}$
$I''_{GB} = I'_{GB}$ $Q''_{ov_L} = Q'_{ov_L}$ $S''_{SD} = S'_{SD}$
$I''_{DS} = -I'_{DS}$ $Q''_D = -Q'_D$ $S''_D = S'_D$
$I''_{DB} = -I'_{DB}$ $Q''_G = -Q'_G$ $S''_G = S'_G$
$I''_{SB} = -I'_{SB}$ $Q''_S = -Q'_S$ $S''_S = S'_S$
$I''_{GS} = -I'_{GS}$ $Q''_B = -Q'_B$ $S''_{DG} = S'_{DG}$
$I''_{GD} = -I'_{GD}$ $Q''_{ov_0} = -Q'_{ov_0}$ $S''_{GS} = S'_{GS}$
$I''_{GB} = -I'_{GB}$ $Q''_{ov_L} = -Q'_{ov_L}$ $S''_{SD} = S'_{SD}$
B

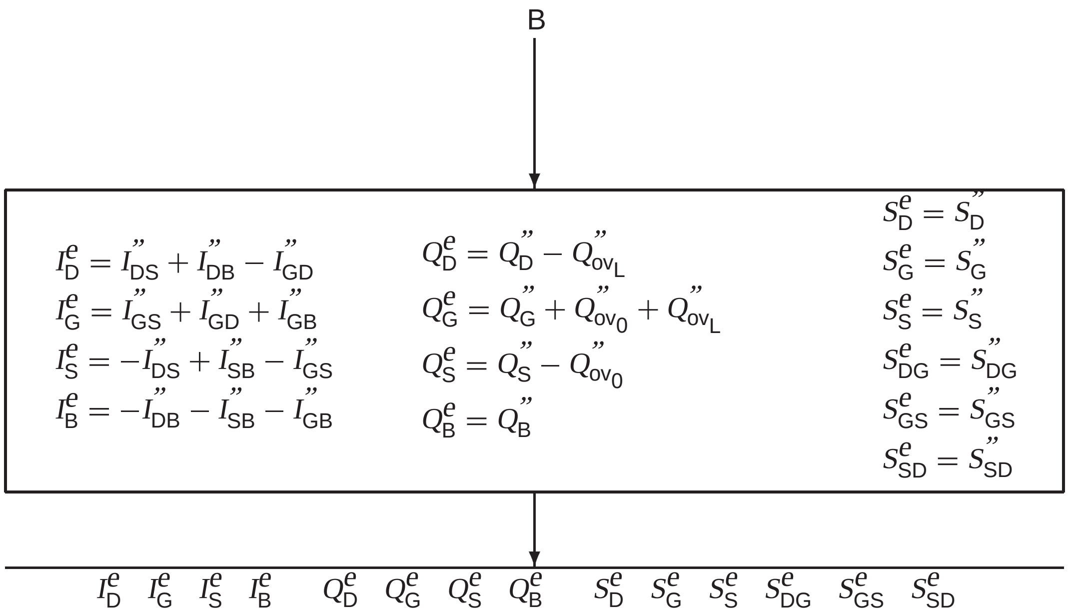


Figure 4.1: Transformation scheme

It is customary to have separate user models in the circuit simulators for n – and p – channel transistors. In that manner it is easy to use a different set of reference and scaling parameters for the two channel types. As a consequence, the changes in the parameter values necessary for a p – channel type transistor are normally already included in the parameter sets on file. The changes should not be included in the simulator.

5 Preprocessing and Clipping

In this Chapter the geometry- and temperature scaling rules for the model parameters will be given.

5.1 Calculation of Transistor Geometry

$$L_E = L - \Delta L = L + \Delta L_{PS} - 2 \cdot \Delta L_{overlap} \quad (5.1)$$

$$W_E = W - \Delta W = W + \Delta W_{OD} - 2 \cdot \Delta W_{narrow} \quad (5.2)$$

WARNING : L_E and W_E after calculation can not be less than 0 !

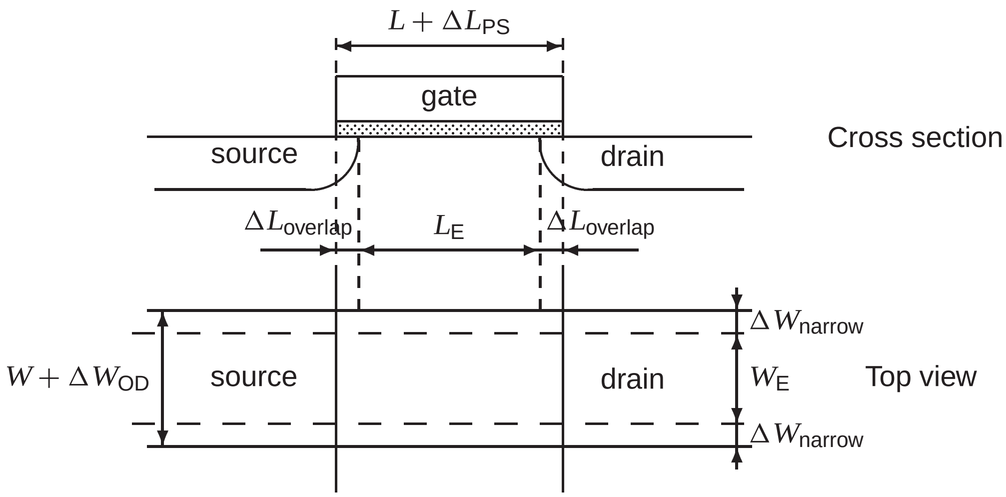


Figure 5.1: Specification of the dimensions of a MOS transistor

5.2 Calculation of Transistor Temperature

$$T_{KR} = T_0 + T_R \quad (5.3)$$

$$T_{KD} = T_0 + T_A + \Delta T_A \quad (5.4)$$

5.3 Calculation of Geometry-Dependent Parameters

Calculation of Threshold–Voltage Parameters

$$\tilde{V}_{FB} = V_{FBR} \quad (5.5)$$

$$k_0 = k_{0R} \cdot \left[1 + \left(\frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L;k_0} + \left(\frac{1}{L_E^2} - \frac{1}{L_{ER}^2} \right) \cdot S_{L2;k_0} \right] \cdot$$

$$\cdot \left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};k_0}\right] \tag{5.6}$$

$$\begin{aligned}\tilde{\phi}_{\mathrm{B}} &= \phi_{\mathrm{BR}}\cdot\left[1+\left(\frac{1}{L_{\mathrm{E}}}-\frac{1}{L_{\mathrm{ER}}}\right)\cdot S_{\mathrm{L};\phi_{\mathrm{B}}}+\left(\frac{1}{L_{\mathrm{E}}^2}-\frac{1}{L_{\mathrm{ER}}^2}\right)\cdot S_{\mathrm{L2};\phi_{\mathrm{B}}}\right]\cdot\\ &\quad\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\phi_{\mathrm{B}}}\right]\end{aligned} \tag{5.7}$$

Calculation of Mobility/Series-Resistance Parameters

$$G_{\mathrm{P,E}} = 1+f_{\beta,1}\cdot\frac{L_{\mathrm{P},1}}{L_{\mathrm{E}}}\cdot\left(1-\mathrm{e}^{-\frac{L_{\mathrm{E}}}{L_{\mathrm{P},1}}}\right)+f_{\beta,2}\cdot\frac{L_{\mathrm{P},2}}{L_{\mathrm{E}}}\cdot\left(1-\mathrm{e}^{-\frac{L_{\mathrm{E}}}{L_{\mathrm{P},2}}}\right) \tag{5.8}$$

$$G_{\mathrm{P,R}} = 1+f_{\beta,1}\cdot\frac{L_{\mathrm{P},1}}{L_{\mathrm{ER}}}\cdot\left(1-\mathrm{e}^{-\frac{L_{\mathrm{ER}}}{L_{\mathrm{P},1}}}\right)+f_{\beta,2}\cdot\frac{L_{\mathrm{P},2}}{L_{\mathrm{ER}}}\cdot\left(1-\mathrm{e}^{-\frac{L_{\mathrm{ER}}}{L_{\mathrm{P},2}}}\right) \tag{5.9}$$

$$\tilde{\beta} = \frac{\beta_{\mathrm{sq}}}{G_{\mathrm{P,E}}}\cdot\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}} \tag{5.10}$$

$$\tilde{\theta}_{\mathrm{sr}} = \theta_{\mathrm{srR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\theta_{\mathrm{sr}}}\right] \tag{5.11}$$

$$\tilde{\theta}_{\mathrm{ph}} = \theta_{\mathrm{phR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\theta_{\mathrm{ph}}}\right] \tag{5.12}$$

$$\tilde{\eta}_{\mathrm{mob}} = \eta_{\mathrm{mobR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\eta_{\mathrm{mob}}}\right] \tag{5.13}$$

$$\tilde{\theta}_{\mathrm{R}} = \theta_{\mathrm{RR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\theta_{\mathrm{R}}}\right]\cdot\frac{L_{\mathrm{ER}}}{L_{\mathrm{E}}}\cdot\frac{G_{\mathrm{P,R}}}{G_{\mathrm{P,E}}} \tag{5.14}$$

$$\tilde{\theta}_{\mathrm{sat}} = \theta_{\mathrm{satR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\theta_{\mathrm{sat}}}\right]\cdot\left[1+S_{\mathrm{L};\theta_{\mathrm{sat}}}\cdot\left\{\left(\frac{L_{\mathrm{ER}}}{L_{\mathrm{E}}}\right)^{\theta_{\mathrm{satEXP}}}-1\right\}\right] \tag{5.15}$$

Calculation of Conductance Parameters

$$\tilde{\theta}_{\mathrm{Th}} = \theta_{\mathrm{ThR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\theta_{\mathrm{Th}}}\right]\cdot\left[\frac{L_{\mathrm{ER}}}{L_{\mathrm{E}}}\right]^{\theta_{\mathrm{ThEXP}}} \tag{5.16}$$

$$\sigma_{\mathrm{sf}} = \sigma_{\mathrm{sfR}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\sigma_{\mathrm{sf}}}\right]\cdot\left[1+\left(\frac{1}{L_{\mathrm{E}}}-\frac{1}{L_{\mathrm{ER}}}\right)\cdot S_{\mathrm{L};\sigma_{\mathrm{sf}}}\right] \tag{5.17}$$

$$\alpha = \alpha_{\mathrm{R}}\cdot\left[1+\left(\frac{1}{W_{\mathrm{E}}}-\frac{1}{W_{\mathrm{ER}}}\right)\cdot S_{\mathrm{W};\alpha}\right]\cdot\left[1+S_{\mathrm{L};\alpha}\cdot\left\{\left(\frac{L_{\mathrm{ER}}}{L_{\mathrm{E}}}\right)^{\alpha_{\mathrm{EXP}}}-1\right\}\right] \tag{5.18}$$

Calculation of Sub–Threshold Parameters

$$\tilde{\phi}_{\mathrm{T}} = \frac{k_{\mathrm{B}} \cdot T_{\mathrm{KR}}}{q} \tag{5.19}$$

$$\sigma_{\mathrm{dibl}} = \sigma_{\mathrm{dibl0}} \cdot \left(\frac{L_{\mathrm{ER}}}{L_{\mathrm{E}}} \right)^{\sigma_{\mathrm{diblEXP}}} \tag{5.20}$$

$$m_0 = m_{0\mathrm{R}} \cdot \left(\frac{L_{\mathrm{ER}}}{L_{\mathrm{E}}} \right)^{m_{0\mathrm{EXP}}} \tag{5.21}$$

Calculation of Smoothing Parameters

$$L_{\max} = 10 \cdot 10^{-6} \tag{5.22}$$

$$m = \frac{8 \cdot (L_{\max} - L_{\min})}{L_{\max} - 4 \cdot L_{\min} + 3 \cdot \frac{L_{\max} \cdot L_{\min}}{L_{\mathrm{E}}}} \tag{5.23}$$

(m is rounded off to the nearest integer)

Calculation of Weak–Avalanche Parameters

$$\tilde{a}_1 = a_{1\mathrm{R}} + \left(\frac{1}{L_{\mathrm{E}}} - \frac{1}{L_{\mathrm{ER}}} \right) \cdot S_{\mathrm{L};\mathrm{a}_1} + \left(\frac{1}{W_{\mathrm{E}}} - \frac{1}{W_{\mathrm{ER}}} \right) \cdot S_{\mathrm{W};\mathrm{a}_1} \tag{5.24}$$

$$a_2 = a_{2\mathrm{R}} + \left(\frac{1}{L_{\mathrm{E}}} - \frac{1}{L_{\mathrm{ER}}} \right) \cdot S_{\mathrm{L};a_2} + \left(\frac{1}{W_{\mathrm{E}}} - \frac{1}{W_{\mathrm{ER}}} \right) \cdot S_{\mathrm{W};a_2} \tag{5.25}$$

$$a_3 = a_{3\mathrm{R}} + \left(\frac{1}{L_{\mathrm{E}}} - \frac{1}{L_{\mathrm{ER}}} \right) \cdot S_{\mathrm{L};a_3} + \left(\frac{1}{W_{\mathrm{E}}} - \frac{1}{W_{\mathrm{ER}}} \right) \cdot S_{\mathrm{W};a_3} \tag{5.26}$$

Calculation of Gate Current Parameters

$$I_{GINV} = \frac{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}{W_{\mathrm{ER}} \cdot L_{\mathrm{ER}}} \cdot I_{\mathrm{GINVR}} \tag{5.27}$$

$$I_{GACC} = \frac{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}{W_{\mathrm{ER}} \cdot L_{\mathrm{ER}}} \cdot I_{\mathrm{GACCR}} \tag{5.28}$$

$$I_{GOV} = \frac{W_{\mathrm{E}}}{W_{\mathrm{ER}}} \cdot I_{\mathrm{GOVR}} \tag{5.29}$$

Calculation of Charge Parameters

$$C_{\mathrm{ox}} = \epsilon_{\mathrm{ox}} \cdot \frac{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}{t_{\mathrm{ox}}} \tag{5.30}$$

$$C_{\mathrm{GDO}} = W_{\mathrm{E}} \cdot C_{\mathrm{ol}} \tag{5.31}$$

$$C_{\mathrm{GSO}} = W_{\mathrm{E}} \cdot C_{\mathrm{ol}} \tag{5.32}$$

Calculation of Noise Parameters

$$\tilde{N}_{\mathrm{T}} = N_{\mathrm{TR}} \tag{5.33}$$

$$N_{\mathrm{FA}} = \frac{W_{\mathrm{ER}} \cdot L_{\mathrm{ER}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}} \cdot N_{\mathrm{FAR}} \tag{5.34}$$

$$N_{\mathrm{FB}} = \frac{W_{\mathrm{ER}} \cdot L_{\mathrm{ER}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}} \cdot N_{\mathrm{FBR}} \tag{5.35}$$

$$N_{\mathrm{FC}} = \frac{W_{\mathrm{ER}} \cdot L_{\mathrm{ER}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}} \cdot N_{\mathrm{FCR}} \tag{5.36}$$

5.4 Calculation of Temperature-Dependent Parameters

Calculation of Threshold–Voltage Parameters

$$V_{\mathrm{FB}} = \tilde{V}_{\mathrm{FB}} + (T_{\mathrm{KD}} - T_{\mathrm{KR}}) \cdot S_{\mathrm{T};V_{\mathrm{FB}}} \tag{5.37}$$

$$S_{\mathrm{T};\phi_{\mathrm{B}}} = \frac{\phi_{\mathrm{BR}} - 1.13 - 2.5 \cdot 10^{-4} \cdot T_{\mathrm{KR}}}{300} \tag{5.38}$$

$$\phi_{\mathrm{B}} = \tilde{\phi}_{\mathrm{B}} + (T_{\mathrm{KD}} - T_{\mathrm{KR}}) \cdot S_{\mathrm{T};\phi_{\mathrm{B}}} \tag{5.39}$$

Calculation of Mobility/Series-Resistance Parameters

$$\beta = \tilde{\beta} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)^{\eta_\beta} \tag{5.40}$$

$$\theta_{\mathrm{sr}} = \begin{cases} \tilde{\theta}_{\mathrm{sr}} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)^{\eta_\beta/2} & \text{for NMOS} \\ \tilde{\theta}_{\mathrm{sr}} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)^{\eta_\beta} & \text{for PMOS} \end{cases} \tag{5.41}$$

$$\theta_{\mathrm{ph}} = \tilde{\theta}_{\mathrm{phR}} \cdot \left(\frac{T_{\mathrm{KD}}}{T_{\mathrm{KR}}}\right)^{3\eta_{\mathrm{ph}} - 3\eta_\beta} \tag{5.42}$$

$$\eta_{\mathrm{mob}} = \tilde{\eta}_{\mathrm{mob}} \cdot \left[1 + (T_{\mathrm{KD}} - T_{\mathrm{KR}}) \cdot S_{\mathrm{T};\eta_{\mathrm{mob}}}\right] \tag{5.43}$$

$$\nu = 1 + \nu_{\mathrm{R}} \cdot \left(T_{\mathrm{KR}} / T_{\mathrm{KD}}\right)^{\nu_{\mathrm{exp}}} \tag{5.44}$$

$$\theta_{\mathrm{R}} = \tilde{\theta}_{\mathrm{R}} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)^{\eta_{\mathrm{R}}} \tag{5.45}$$

$$\theta_{\mathrm{sat}} = \tilde{\theta}_{\mathrm{sat}} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)^{\eta_{\mathrm{sat}}} \tag{5.46}$$

Calculation of Conductance Parameters

$$\theta_{\mathrm{Th}} = \tilde{\theta}_{\mathrm{Th}} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)^{\eta_\beta} \tag{5.47}$$

Calculation of Sub–Threshold Parameters

$$\phi_{\mathrm{T}} = \frac{T_{\mathrm{KD}}}{T_{\mathrm{KR}}} \cdot \tilde{\phi}_{\mathrm{T}} \tag{5.48}$$

Calculation of Weak–Avalanche Parameters

$$a_1 = \tilde{a}_1 \cdot \left[1 + (T_{\mathrm{KD}} - T_{\mathrm{KR}}) \cdot S_{\mathrm{T;a_1}}\right] \tag{5.49}$$

Calculation of Noise Parameters

$$N_{\mathrm{T}} = \frac{T_{\mathrm{KD}}}{T_{\mathrm{KR}}} \cdot \tilde{N}_{\mathrm{T}} \tag{5.50}$$

5.5 Clipping

For the clipping of a parameter the lower bound B_L and/or the upper bound B_U are specified for the value range of that parameter. If both bounds are given the value range is the closed interval $[B_L, B_U]$ and in the case of one bound it is either the half–open interval $[B_L, \infty)$ or $(-\infty, B_U]$. If the value of a parameter exceeds its bound it has to be replaced by that particular bound. The following (miniset) parameters have clipping bounds:

Parameter	**Lower bound**	**Upper bound**
k_0	10^{-12}	–
$1/k_P$	0	–
ϕ_B	10^{-12}	–
β	0	–
θ_{sr}	10^{-12}	–
θ_{ph}	10^{-12}	–
η_{mob}	0	–
ν	1	–
θ_R	0	–
θ_{R1}	0	–
θ_{R2}	0	–
θ_{sat}	0	–
θ_{Th}	0	–
σ_{dibl}	10^{-12}	–
m_0	0	0.5
σ_{sf}	10^{-12}	–
α	0	–
V_P	10^{-12}	–
m	1	–
ϕ_T	10^{-12}	–
V_{SBT}	0	–
a_1	0	–
a_2	10^{-12}	–
a_3	0	–
I_{GINV}	0	–
B_{INV}	0	–
I_{GACC}	0	–
B_{ACC}	0	–
k_{ov}	10^{-12}	–
I_{GOV}	0	–
C_{ox}	0	–
C_{GDO}	0	–
C_{GSO}	0	–
N_T	0	–
N_{FA}	10^{-12}	–
t_{ox}	10^{-12}	–
N_{MULT}	1	–

6 Implemented Model Equations

The electrical equations of MOS Model 11 to be implemented are essentially the basic equations of Section 2. Since in circuit design equal parallel circuited transistors are frequently applied the specification of one transistor together with a multiplication factor N_{MULT} in the circuit description is convenient and saves computation time. The general and safe method to implement this mechanism into the model is to evaluate the currents, charges, noise spectral densities and their derivatives with respect to the external voltages and, at the end, to multiply them by N_{MULT}. In MOS Model 11 it is allowed to circumvent these multiplications for each model evaluation during circuit simulation by adjusting some parameters. In this case the following rules apply:

$$\begin{aligned}
\beta &= \beta \cdot N_{\mathrm{MULT}} \\
I_{\mathrm{GINV}} &= I_{\mathrm{GINV}} \cdot N_{\mathrm{MULT}} \\
I_{\mathrm{GACC}} &= I_{\mathrm{GACC}} \cdot N_{\mathrm{MULT}} \\
I_{\mathrm{GOV}} &= I_{\mathrm{GOV}} \cdot N_{\mathrm{MULT}} \\
C_{\mathrm{ox}} &= C_{\mathrm{ox}} \cdot N_{\mathrm{MULT}} \\
C_{\mathrm{GDO}} &= C_{\mathrm{GDO}} \cdot N_{\mathrm{MULT}} \\
C_{\mathrm{GSO}} &= C_{\mathrm{GSO}} \cdot N_{\mathrm{MULT}} \\
N_{\mathrm{F}} &= \frac{N_{\mathrm{F}}}{N_{\mathrm{MULT}}} \\
N_{\mathrm{FA}} &= \frac{N_{\mathrm{FA}}}{N_{\mathrm{MULT}}} \\
N_{\mathrm{FB}} &= \frac{N_{\mathrm{FB}}}{N_{\mathrm{MULT}}} \\
N_{\mathrm{FC}} &= \frac{N_{\mathrm{FC}}}{N_{\mathrm{MULT}}}
\end{aligned}$$

Although the basic equations, given in Section 2, form a complete set of model equations, they are not yet suited for a circuit simulator. Several equations have to be adapted in order to obtain smooth transitions of the characteristics between adjacent regions of operation and to prevent numerical problems during the iteration process for solving the network equations. In the following section a list of numerical adaptations and elucidations is given, followed by the extended set of model equations.

The definition of the hyp-function, which provides for a smooth C_{∞}-continuous clipping, is to be found in Appendix A.

6.1 Numerical Adaptations

The implemented electrical equations of MOS Model 11 are essentially based on the physical description given in Section 2. The following numerical adaptations have been made in order to obtain smooth transitions and prevent numerical problems, leading to the equations given in Section6.2:

- The piece-wise eqs. (2.1) and (2.8) for $V_{\mathrm{GB_{eff}}}$, (2.4) for D_{sf}, (2.5) for D, (2.11) for $V_{\mathrm{DSAT_{long}}}$, (2.15) for V_{DSAT}, (2.17), (2.22) and (2.51) for different functions f_1, (2.48) for $V_{\mathrm{GX_{eff}}}$ and (2.63) for I_{GB} have been replaced by smooth C_∞-continuous functions based on hyp-functions.

- Expression (2.3) describing the drain-induced barrier lowering effect has no numerical solution for $V_{\mathrm{SB}} + \phi_{\mathrm{B}} < 0$. In order to solve this problem the expression $V_{\mathrm{SB}} + \phi_{\mathrm{B}}$ is clipped at a minimum value of $0.1 \cdot \phi_{\mathrm{B}}$ using eq. (6.2). In order to maintain symmetry (with respect to source and drain) the same method must be applied to the drain side, this is done in eq. (6.18).
- The effective voltage V_{eff} given by eq. (6.33) becomes negative in the accumulation region, which leads to strange behaviour in the mobility reduction expression (2.33). In order to prevent V_{eff} from becoming negative, a hyp-smoothing function is used in the actual implementation, see eq. (6.35).
- The theoretical velocity saturation expression (2.35) results in zero divided by zero for $V_{\mathrm{DS}} = 0$. This numerical problem has been circumvented by replacing this expression by a third-order Taylor polynomial for small values of V_{DS}, see eq. (6.38).
- The theoretical channel length modulation expression (2.36) can become negative for high values of α and V_{DS}. This corresponds to a negative effective channel length, which is not physical. In order to prevent $G_{\Delta\mathrm{L}}$ from becoming negative, a hyp-smoothing function is used in the actual implementation, see eq. (6.39).
- The term in the square root of eq. (2.39) can become negative for very high values of parameter θ_{R}, which would result in numerical errors. This has been prevented in the actual implementation (6.42) by using a hyp-smoothing function.
- The term $\psi_{\mathrm{s_{inv}}} + \Delta_{\mathrm{acc}}$ in expression (2.40) may become negative in accumulation for certain parameter values. Since a square root is taken of this term, it has to be prevented that the above term becomes negative; this has been done using a hyp-smoothing function (6.43) in eq. (6.44). The same type of problem occurs in eq. (2.32) for variable ξ, it has been circumvented in the same way, see eq. (6.34).
- Theoretically in subthreshold the drift current given by eq. (2.43) is much smaller than the diffusion current, due to the term $\Delta\psi$ which rapidly approaches zero for decreasing gate bias. Owing to the approximations made in the calculation of surface potential in MOS Model 11, for certain conditions $\Delta\psi$ may not go to zero rapidly enough. As a result the drift current is forced to very small values in subthreshold by making use of eqs. (6.47) to (6.50).
- The exponent in the tunnelling probability P_{tun}, given by eq. (2.47), results in zero divided by zero for $V_{\mathrm{ox}} = 0$. By simply rewriting the exponent, this problem can be circumvented as has been done in eq. (6.54).
- The expression of effective oxide barrier lowering $\Delta\chi_{\mathrm{B}}$, given by eq. (2.64), can become equal to zero (at $V_{\mathrm{GB}} = V_{\mathrm{FB}}$), resulting in numerical errors in the first-order derivatives of $\Delta\chi_{\mathrm{B}}$ to the terminal voltages. In order to prevent $\Delta\chi_{\mathrm{B}}$ from becoming zero, eq. (6.72) has been used.
- For very high gate bias values, which could occur during the iteration process of the circuit simulator, the expression of effective oxide barrier $\chi_{\mathrm{B_{eff}}}$, given by eq. (2.65), can become zero or negative resulting in numerical errors. In order to prevent this problem $\chi_{\mathrm{B_{eff}}}$ is clipped at a minimum (arbitrary) value of $0.7 \cdot \chi_{\mathrm{B_{inv}}}$ using a hyp-smoothing function, see eq. (6.73).
- The expression of $\partial V_{\mathrm{ox}}^*$, given by eq. (2.70), gives numerical problems when the oxide voltage V_{ox} is equal to zero. This problem has been circumvented by replacing V_{ox} by $\sqrt{{V_{\mathrm{ox}}}^2 + {V_{\mathrm{limit}}}^2}$, see eq. (6.78).

- The expression of effective oxide capacitance (2.80) due to quantum-mechanical effects gives erroneous results for $V_{\mathrm{eff}} = 0$ (i.e. $V_{\mathrm{GB}} = V_{\mathrm{FB}}$). This can be prevented by replacing $V_{\mathrm{eff}} / \eta_{\mathrm{mob}}$ by $\sqrt{\left(V_{\mathrm{eff}} / \eta_{\mathrm{mob}}\right)^2 + (20 \cdot \phi_{\mathrm{T}})^2}$, where the value of $20 \cdot \phi_{\mathrm{T}}$ is rather arbitrary but it nevertheless ensures a smooth transition from accumulation to depletion/inversion.

6.2 Extended Equations

In the following sections a function is denoted by $F\{variable, \ldots\}$, where F denotes the function name and the function variables are enclosed by braces {}. The definitions of the hyp-functions are found in Appendix A.

6.2.1 Internal Parameters

$$\epsilon_1 = 2 \cdot 10^{-2}$$

$$\epsilon_2 = 1 \cdot 10^{-2}$$

$$\epsilon_3 = 4 \cdot 10^{-2}$$

$$\epsilon_4 = 1 \cdot 10^{-1}$$

$$\epsilon_5 = 1 \cdot 10^{-4}$$

$$P_\mathrm{D} = 1 + \left(k_0 \big/ k_\mathrm{P}\right)^2$$

$$V_\mathrm{limit} = 5 \cdot \phi_\mathrm{T}$$

$$\theta_{\mathrm{R_{eff}}} = \frac{1}{2}\theta_\mathrm{R} \cdot \left(1 + \frac{\theta_\mathrm{R1}}{1/2 + \theta_\mathrm{R2}}\right)$$

$$Acc = \left.\frac{\partial \psi_\mathrm{s}}{\partial V_\mathrm{GB}}\right|_{V_\mathrm{GB}=V_\mathrm{FB}} = \frac{1}{1 + k_0 \big/ \sqrt{2\phi_\mathrm{T}}}$$

$$N_{\phi_\mathrm{T}} = (2.6)^2 / k_0$$

$$Acc_\mathrm{ov} = \left.\frac{\partial \psi_\mathrm{sov}}{\partial V_\mathrm{GB}}\right|_{V_\mathrm{GB}=V_\mathrm{FBov}} = \frac{1}{1 + k_\mathrm{ov} \big/ \sqrt{2\phi_\mathrm{T}}}$$

$$QM_\psi = \begin{cases} QM_\mathrm{N} \cdot \left(\epsilon_\mathrm{ox} \big/ t_\mathrm{ox}\right)^{2/3} & \text{for NMOS} \\ QM_\mathrm{P} \cdot \left(\epsilon_\mathrm{ox} \big/ t_\mathrm{ox}\right)^{2/3} & \text{for PMOS} \end{cases}$$

$$QM_\mathrm{tox} = \frac{2}{5} \cdot QM_\psi$$

$$\chi_{\mathrm{B_{inv}}} = \begin{cases} \chi_{\mathrm{B_N}} & \text{for NMOS} \\ \chi_{\mathrm{B_P}} & \text{for PMOS} \end{cases}$$

$$\chi_{\mathrm{B_{acc}}} = \chi_{\mathrm{B_N}}$$

6.2.2 Extended Current Equations

$$V_{\mathrm{GB_{eff}}} = \mathrm{hyp}_1 \left\{V_{\mathrm{GS}} + V_{\mathrm{SB}} - V_{\mathrm{FB}}; \epsilon_1\right\} \tag{6.1}$$

$$V_{\mathrm{SB_t}} = \mathrm{hyp}_1 \left\{V_{\mathrm{SB}} + 0.9 \cdot \phi_{\mathrm{B}}; \epsilon_2\right\} + 0.1 \cdot \phi_{\mathrm{B}} \tag{6.2}$$

$$\psi_{\mathrm{sat_0}} = \left(\frac{\sqrt{P_{\mathrm{D}} \cdot V_{\mathrm{GB_{eff}}} + {k_0}^2/4} - k_0/2}{P_{\mathrm{D}}}\right)^2 \tag{6.3}$$

Drain induced barrier lowering and Static Feedback:

$$D_{\mathrm{dibl}} = \sigma_{\mathrm{dibl}} \cdot \sqrt{V_{\mathrm{SB_t}}} \tag{6.4}$$

$$D_{\mathrm{sf}} = \sigma_{\mathrm{sf}} \cdot \sqrt{\mathrm{hyp}_1 \left\{\psi_{\mathrm{sat_0}} - V_{\mathrm{SB_t}}; \epsilon_3\right\}} \tag{6.5}$$

$$D = D_{\mathrm{dibl}} + \mathrm{hyp}_1 \left\{D_{\mathrm{sf}} - D_{\mathrm{dibl}}; \sigma_{\mathrm{sf}} \cdot \epsilon_4\right\} \tag{6.6}$$

$$V_{\mathrm{DS_{eff}}} = \frac{{V_{\mathrm{DS}}}^4}{\left({V_{\mathrm{limit}}}^2 + {V_{\mathrm{DS}}}^2\right)^{3/2}} \tag{6.7}$$

$$\Delta V_{\mathrm{G}} = D \cdot V_{\mathrm{DS_{eff}}} \tag{6.8}$$

Redefinition of $V_{\mathrm{GB_{eff}}}$, equation (6.1):

$$V_{\mathrm{GB_{eff}}} = \mathrm{hyp}_1 \left\{V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}}; \epsilon_1\right\} \tag{6.9}$$

$$\Delta_{\mathrm{acc}} = \phi_{\mathrm{T}} \cdot \left[\exp\left(-\frac{Acc \cdot \left[V_{\mathrm{GB_{eff}}} - \epsilon_1\right]}{\phi_{\mathrm{T}}}\right) - 1\right] \tag{6.10}$$

$$\psi_{\mathrm{sat_1}} = \left(\frac{\sqrt{P_{\mathrm{D}} \cdot \left(V_{\mathrm{GB_{eff}}} + \Delta_{\mathrm{acc}}\right) + {k_0}^2/4} - k_0/2}{P_{\mathrm{D}}}\right)^2 - \Delta_{\mathrm{acc}} \tag{6.11}$$

Drain Saturation Voltage:

$$V_{\mathrm{DSAT_{long}}} = \psi_{\mathrm{sat_1}} - V_{\mathrm{SB_t}} \tag{6.12}$$

$$T_{\mathrm{sat}} = \begin{cases} \theta_{\mathrm{sat}} & \text{for NMOS} \\ \dfrac{\theta_{\mathrm{sat}}}{\left(1+{\theta_{\mathrm{sat}}}^2 \cdot {V_{\mathrm{DSAT_{long}}}}^2\right)^{1/4}} & \text{for PMOS} \end{cases} \tag{6.13}$$

$$\Delta_{\mathrm{SAT}} = \frac{T_{\mathrm{sat}} - \theta_{\mathrm{R_{eff}}}}{\sqrt{\frac{2}{V_{\mathrm{DSAT_{long}}}{}^2 + \epsilon_4} + T_{\mathrm{sat}}{}^2} + \theta_{\mathrm{R_{eff}}}} \tag{6.14}$$

$$V_{\mathrm{DSAT_{short}}} = V_{\mathrm{DSAT_{long}}} \cdot \left(1 - \frac{9}{10} \cdot \frac{\Delta_{\mathrm{SAT}}}{1 + \sqrt{1 - \Delta_{\mathrm{SAT}}{}^2}}\right) \tag{6.15}$$

$$V_{\mathrm{DSAT}} = V_{\mathrm{limit}} + \mathrm{hyp}_1 \left\{ V_{\mathrm{DSAT_{short}}} - V_{\mathrm{limit}}; \epsilon_3 \right\} \tag{6.16}$$

$$V_{\mathrm{DS_x}} = \frac{V_{\mathrm{DS}} \cdot V_{\mathrm{DSAT}}}{\left[V_{\mathrm{DS}}{}^{2m} + V_{\mathrm{DSAT}}{}^{2m} \right]^{1/2m}} \tag{6.17}$$

$$V_{\mathrm{DB_t}} = \mathrm{hyp}_1 \left\{ V_{\mathrm{DS_x}} + V_{\mathrm{SB}} + 0.9 \cdot \phi_{\mathrm{B}}; \epsilon_2 \right\} + 0.1 \cdot \phi_{\mathrm{B}} \tag{6.18}$$

Surface Potential:

$$f_1 \{\psi\} = \psi_{\mathrm{sat_1}} - \mathrm{hyp}_1 \left\{ \psi_{\mathrm{sat_1}} - \psi; \epsilon_1 \right\} \tag{6.19}$$

$$f_2 \{\psi\} = f_1\{\psi\} + \frac{\psi_{\mathrm{sat_1}} - f_1\{\psi\}}{\sqrt{1 + \frac{\left[\psi_{\mathrm{sat_1}} - f_1\{\psi\}\right]^2}{N_{\phi_{\mathrm{T}}} \cdot \phi_{\mathrm{T}}{}^2}}} \tag{6.20}$$

$$f_3 \{\psi\} = \frac{2 \cdot \left[V_{\mathrm{GB_{eff}}} - f_2\{\psi\} \right]}{1 + \sqrt{1 + 4/k_{\mathrm{P}}{}^2 \cdot \left[V_{\mathrm{GB_{eff}}} - f_2\{\psi\} \right]}} \tag{6.21}$$

$$\psi_{\mathrm{s_{inv}}} \{\psi\} = f_1\{\psi\} + \phi_{\mathrm{T}} \cdot [1 + m_0] \cdot \ln \left[\frac{\left[\frac{f_3\{\psi\}}{k_0} \right]^2 - f_1\{\psi\} - \Delta_{\mathrm{acc}} + \phi_{\mathrm{T}}}{\phi_{\mathrm{T}}} \right] \tag{6.22}$$

$$\begin{aligned} \psi^*_{\mathrm{s_0}} &= \psi_{\mathrm{s_{inv}}} \left\{ V_{\mathrm{SB_t}} \right\} \\ \psi^*_{\mathrm{s_L}} &= \psi_{\mathrm{s_{inv}}} \left\{ V_{\mathrm{DB_t}} \right\} \end{aligned} \tag{6.23}$$

Surface Potential in Accumulation:

$$f_1 = Acc \cdot \left[V_{\mathrm{GS}} + V_{\mathrm{SB}} + \Delta V_{\mathrm{G}} - V_{\mathrm{FB}} - V_{\mathrm{GB_{eff}}} \right] \tag{6.24}$$

$$f_2 = \frac{f_1}{\sqrt{1 + \frac{f_1{}^2}{N_{\phi_{\mathrm{T}}} \cdot \phi_{\mathrm{T}}{}^2}}} \tag{6.25}$$

$$\psi_{\mathrm{sacc}} = -\phi_{\mathrm{T}} \cdot \ln \left[\frac{\left[\frac{f_1/Acc - f_2}{k_0} \right]^2 - f_2 + \phi_{\mathrm{T}}}{\phi_{\mathrm{T}}} \right] \tag{6.26}$$

Auxiliary Variables:

$$\Delta\psi = \psi^*_{s_L} - \psi^*_{s_0} \tag{6.27}$$

$$\bar{\psi}_{inv} = \frac{\psi^*_{s_L} + \psi^*_{s_0}}{2} \tag{6.28}$$

$$V_{G_T}\left\{\psi_{s_{inv}}\right\} = \frac{2\cdot\left[V_{GB_{eff}} - \psi_{s_{inv}}\right]}{1+\sqrt{1+4/k_P{}^2\cdot\left[V_{GB_{eff}} - \psi_{s_{inv}}\right]}} - k_0\cdot\sqrt{\mathrm{hyp}_1\left\{\psi_s + \Delta_{acc};\epsilon_2\right\}} \tag{6.29}$$

$$\bar{V}_{G_T} = V_{G_T}\left\{\bar{\psi}_{inv}\right\} \tag{6.30}$$

$$V_{ox} = \frac{2\cdot\left[V_{GS} + V_{SB} + \Delta V_G - V_{FB} - \bar{\psi}_{inv} - \psi_{acc}\right]}{1+\sqrt{1+4/k_P{}^2\cdot\left[V_{GB_{eff}} - \bar{\psi}_{inv}\right]}} \tag{6.31}$$

$$\partial V_{ox} = \frac{2}{1+\sqrt{1+4/k_P{}^2\cdot\left[V_{GB_{eff}} - \bar{\psi}_{inv}\right]}} \tag{6.32}$$

$$V_{eff} = \bar{V}_{G_T} + \eta_{mob}\cdot\left(V_{ox} - \bar{V}_{G_T}\right) \tag{6.33}$$

$$\xi = \phi_T\cdot\left[\frac{1}{1+\sqrt{1+4/k_P{}^2\cdot\left[V_{GB_{eff}} - \bar{\psi}_{inv}\right]}} + \frac{k_0}{2\sqrt{\mathrm{hyp}_1\left(\bar{\psi}_{inv} + \Delta_{acc};\epsilon_5\right)}}\right] \tag{6.34}$$

Second-Order Effects

Mobility Degradation:

$$V_{eff_1} = \mathrm{hyp}_1\left\{V_{eff};\epsilon_2\right\} \tag{6.35}$$

$$G_{mob} = \frac{\mu_0}{\mu} = \begin{cases} 1+\left[\left(\theta_{ph}\cdot V_{eff_1}\right)^{\nu/3} + \left(\theta_{sr}\cdot V_{eff_1}\right)^{2\nu}\right]^{1/\nu} & \text{for NMOS} \\ \left[1+\left(\theta_{ph}\cdot V_{eff_1}\right)^{\nu/3} + \left(\theta_{sr}\cdot V_{eff_1}\right)^{\nu}\right]^{1/\nu} & \text{for PMOS} \end{cases} \tag{6.36}$$

Velocity Saturation:

$$x = \begin{cases} \frac{2\cdot\theta_{sat}\cdot\Delta\psi}{\sqrt{G_{mob}}} & \text{for NMOS} \\ \frac{2\cdot\theta_{sat}}{\sqrt{G_{mob}}}\cdot\frac{\Delta\psi}{\left(1+\theta_{sat}{}^2\cdot\Delta\psi^2\right)^{1/4}} & \text{for PMOS} \end{cases} \tag{6.37}$$

$$G_{vsat} = \begin{cases} \frac{G_{mob}}{2}\cdot\left[\sqrt{1+x^2} + 1 - \frac{x^2}{6}\right] & \text{for:}\quad x < 1\cdot 10^{-4} \\ \frac{G_{mob}}{2}\cdot\left[\sqrt{1+x^2} + \frac{\ln\left(x+\sqrt{1+x^2}\right)}{x}\right] & \text{for:}\quad x \geq 1\cdot 10^{-4} \end{cases} \tag{6.38}$$

Channel Length Modulation:

$$G_{\Delta L} = \mathrm{hyp}_1 \left\{ 1 - \alpha \cdot \ln \left[\frac{V_{DS} - V_{DS_x} + \sqrt{\left(V_{DS} - V_{DS_x}\right)^2 + V_P{}^2}}{V_P} \right]; \epsilon_5 \right\} \tag{6.39}$$

Series Resistance + Self-Heating:

$$G_R = \theta_R \cdot \left(1 + \frac{\theta_{R1}}{\theta_{R2} + \bar{V}_{G_T}} \right) \cdot \bar{V}_{G_T} \tag{6.40}$$

$$G_{Th} = \theta_{Th} \cdot V_{DS} \cdot \Delta\psi \cdot \bar{V}_{G_T} \tag{6.41}$$

$$G_{tot} = G_{Th} + \frac{[G_{\Delta L} \cdot G_{vsat} + G_R]}{2} \cdot$$

$$\cdot \left[1 + \sqrt{\mathrm{hyp}_1 \left\{ 1 - \frac{4 \cdot G_R / G_{vsat}}{[G_{\Delta L} \cdot G_{vsat} + G_R]^2} \cdot \left[G_{vsat}{}^2 - G_{mob}{}^2 \right]; \epsilon_5 \right\}} \right] \tag{6.42}$$

Inversion-Layer Charge ($Q_{inv} = -\epsilon_{ox} \big/ t_{ox} \cdot V_{inv}$):

$$\psi_{s_{inv}}{}^* \left\{ \psi_{s_{inv}} \right\} = \mathrm{hyp}_1 \left\{ \psi_{s_{inv}} + \Delta_{acc}; \epsilon_5 \right\} \tag{6.43}$$

$$V_{inv} \left\{ \psi_{s_{inv}}, \psi \right\} = \frac{k_0 \cdot \phi_T \cdot \exp\left[\frac{\psi_{s_{inv}} - \psi}{[1+m_0] \cdot \phi_T} \right]}{\sqrt{\psi_{s_{inv}}{}^* \left\{ \psi_{s_{inv}} \right\} + \phi_T \cdot \exp\left[\frac{\psi_{s_{inv}} - \psi}{[1+m_0] \cdot \phi_T} \right]} + \sqrt{\psi_{s_{inv}}{}^* \left\{ \psi_s \right\}}} \tag{6.44}$$

$$V_{inv_0} = V_{inv} \left\{ \psi^*_{s_0}, V_{SB_t} \right\} \tag{6.45}$$

$$V_{inv_L} = V_{inv} \left\{ \psi^*_{s_L}, V_{DB_t} \right\} \tag{6.46}$$

Drain Current

$$x_0 = \frac{2}{\phi_T} \cdot \left(\psi_{sat_1} + \phi_T - V_{SB_t} \right) \tag{6.47}$$

$$x_L = \frac{2}{\phi_T} \cdot \left(\psi_{sat_1} + \phi_T - V_{DB_t} \right) \tag{6.48}$$

$$G = \frac{\exp(x_0) + \exp(x_L)}{\exp(x_0) + \exp(x_L) + 1} \tag{6.49}$$

$$I_{drift} = \begin{cases} \beta \cdot \bar{V}_{G_T} \cdot \Delta\psi & \text{for:} \quad x_0 > 80 \quad \text{or} \quad x_L > 80 \\ \beta \cdot \bar{V}_{G_T} \cdot \Delta\psi \cdot G & \text{for:} \quad x_0 \leq 80 \quad \text{and} \quad x_L \leq 80 \end{cases} \tag{6.50}$$

$$I_{\mathrm{diff}} = \beta \cdot \phi_{\mathrm{T}} \cdot \left(V_{\mathrm{inv}_0} - V_{\mathrm{inv}_{\mathrm{L}}}\right) \tag{6.51}$$

$$I_{\mathrm{DS}} = \frac{I_{\mathrm{drift}} + I_{\mathrm{diff}}}{G_{\mathrm{tot}}} \tag{6.52}$$

Weak-Avalanche:

$$I_{\mathrm{avl}} = \begin{cases} 0 & \text{for:} \quad V_{\mathrm{DS}} \leq a_3 \cdot V_{\mathrm{DSAT}} \\ a_1 \cdot I_{\mathrm{DS}} \cdot \exp\left(-\frac{a_2}{V_{\mathrm{DS}} - a_3 \cdot V_{\mathrm{DSAT}}}\right) & \text{for:} \quad V_{\mathrm{DS}} > a_3 \cdot V_{\mathrm{DSAT}} \end{cases} \tag{6.53}$$

Gate Current Equations:

The tunnelling probability is given by:

$$P_{\mathrm{tun}}\left\{V_{\mathrm{ox}}; \chi_{\mathrm{B}}; B\right\} = \begin{cases} \exp\left(-\frac{B}{\chi_{\mathrm{B}}} \cdot \frac{\left[\left(\frac{V_{\mathrm{ox}}}{\chi_{\mathrm{B}}}\right)^2 - 3 \cdot \frac{V_{\mathrm{ox}}}{\chi_{\mathrm{B}}} + 3\right]}{1 + \left(1 - \frac{V_{\mathrm{ox}}}{\chi_{\mathrm{B}}}\right)^{\frac{3}{2}}}\right) & \text{for:} \quad V_{\mathrm{ox}} < \chi_{\mathrm{B}} \\ \exp\left(-\, B \big/ V_{\mathrm{ox}}\right) & \text{for:} \quad V_{\mathrm{ox}} \geq \chi_{\mathrm{B}} \end{cases} \tag{6.54}$$

Source/Drain Gate Overlap Current: First calculate the oxide voltage V_{ov} at both Source and Drain overlap:

$$V_{\mathrm{GX}_{\mathrm{eff}}}\left\{V_{\mathrm{GX}}\right\} = V_{\mathrm{GX}} - V_{\mathrm{FBov}} - \mathrm{hyp}_1\left\{V_{\mathrm{GX}} - V_{\mathrm{FBov}}; \epsilon_1\right\} \tag{6.55}$$

$$\Delta_{\mathrm{ov}}\left\{V_{\mathrm{GX}}\right\} = \phi_{\mathrm{T}} \cdot \left[\exp\left(\frac{Acc_{\mathrm{ov}} \cdot \left[V_{\mathrm{GX}_{\mathrm{eff}}}\left\{V_{\mathrm{GX}}\right\} + \epsilon_1\right]}{\phi_{\mathrm{T}}}\right) - 1\right] \tag{6.56}$$

$$\psi_{\mathrm{sat}_{\mathrm{ov}}}\left\{V_{\mathrm{GX}}\right\} = -\left[\sqrt{\frac{k_{\mathrm{ov}}{}^2}{4} - V_{\mathrm{GX}_{\mathrm{eff}}}\left\{V_{\mathrm{GX}}\right\} + \Delta_{\mathrm{ov}}\left\{V_{\mathrm{GX}}\right\}} - \frac{k_{\mathrm{ov}}}{2}\right]^2 + \Delta_{\mathrm{ov}}\left\{V_{\mathrm{GX}}\right\} \tag{6.57}$$

$$f_1\left\{V_{\mathrm{GX}}\right\} = Acc_{\mathrm{ov}} \cdot \left[V_{\mathrm{GX}} - V_{\mathrm{FBov}} - V_{\mathrm{GX}_{\mathrm{eff}}}\left\{V_{\mathrm{GX}}\right\}\right] \tag{6.58}$$

$$f_2\left\{V_{\mathrm{GX}}\right\} = \frac{f_1\left\{V_{\mathrm{GX}}\right\}}{\sqrt{1 + \frac{\left[f_1\left\{V_{\mathrm{GX}}\right\}\right]^2}{N_{\phi_{\mathrm{T}}} \cdot \phi_{\mathrm{T}}{}^2}}} \tag{6.59}$$

$$f_3\left\{V_{\mathrm{GX}}\right\} = \frac{2 \cdot \left[\frac{f_1\left\{V_{\mathrm{GX}}\right\}}{Acc_{\mathrm{ov}}} - f_2\left\{V_{\mathrm{GX}}\right\}\right]}{1 + \sqrt{1 + 4/k_{\mathrm{P}}{}^2 \cdot \left[\frac{f_1\left\{V_{\mathrm{GX}}\right\}}{Acc_{\mathrm{ov}}} - f_2\left\{V_{\mathrm{GX}}\right\}\right]}} \tag{6.60}$$

$$\psi^*_{\mathrm{s}_{\mathrm{ov}}}\left\{V_{\mathrm{GX}}\right\} = \phi_{\mathrm{T}} \cdot \ln\left[\frac{\left[\frac{f_3\left\{V_{\mathrm{GX}}\right\}}{k_{\mathrm{ov}}}\right]^2 + f_2\left\{V_{\mathrm{GX}}\right\} + \phi_{\mathrm{T}}}{\phi_{\mathrm{T}}}\right] \tag{6.61}$$

$$V_{\text{ov}}\left\{V_{\text{GX}}\right\}=\frac{2\cdot\left[V_{\text{GX}}-V_{\text{FBov}}-\psi^{*}_{\text{sov}}\left\{V_{\text{GX}}\right\}-\psi_{\text{satov}}\left\{V_{\text{GX}}\right\}\right]}{1+\sqrt{1+4/k_{\text{P}}^{2}\cdot\left[f_{1}\left\{V_{\text{GX}}\right\}/Acc_{\text{ov}}-\psi^{*}_{\text{sov}}\left\{V_{\text{GX}}\right\}\right]}} \tag{6.62}$$

$$V_{\text{ov}_0}=V_{\text{ov}}\left\{V_{\text{GS}}\right\} \tag{6.63}$$

$$V_{\text{ov}_\text{L}}=V_{\text{ov}}\left\{V_{\text{GS}}-V_{\text{DS}}\right\} \tag{6.64}$$

Next calculate the gate tunnelling current in both Source and Drain overlap:

$$P_{\text{ov}}\left\{V_{\text{ov}}\right\}=P_{\text{tun}}\left\{V_{\text{ov}};\,\chi_{\text{B}_{\text{inv}}};\,B_{\text{inv}}\right\} \tag{6.65}$$

$$I_{\text{Gov}}\left\{V_{\text{GX}},V_{\text{ov}}\right\}=I_{\text{GOV}}\cdot V_{\text{GX}}\cdot V_{\text{ov}}\cdot\left[P_{\text{ov}}\left\{V_{\text{ov}}\right\}-P_{\text{ov}}\left\{-V_{\text{ov}}\right\}\right] \tag{6.66}$$

$$I_{\text{Gov}_0}=I_{\text{Gov}}\left\{V_{\text{GS}}\;,\;V_{\text{ov}_0}\right\} \tag{6.67}$$

$$I_{\text{Gov}_\text{L}}=I_{\text{Gov}}\left\{V_{\text{GS}}-V_{\text{DS}}\;,\;V_{\text{ov}_\text{L}}\right\} \tag{6.68}$$

Intrinsic Gate Current: The gate tunnelling current in accumulation:

$$P_{\text{acc}}=P_{\text{tun}}\left\{-V_{\text{ox}};\,\chi_{\text{B}_{\text{acc}}};\,B_{\text{acc}}\right\} \tag{6.69}$$

$$V_{\text{acc}}=V_{\text{ox}}-\text{hyp}_1\left\{V_{\text{ox}};\epsilon_5\right\} \tag{6.70}$$

$$I_{\text{GB}}=-I_{\text{GACC}}\cdot\left(V_{\text{GS}}+V_{\text{SB}}\right)\cdot V_{\text{acc}}\cdot P_{\text{acc}} \tag{6.71}$$

The tunnelling current in inversion, including quantum-mechanical barrier lowering $\Delta\chi_{\text{B}}$:

$$\Delta\chi_{\text{B}}=QM_{\psi}\cdot\left[\left(\bar{V}_{\text{G}_\text{T}}\big/3+V_{\text{ox}}-\bar{V}_{\text{G}_\text{T}}\right)^{2}+V_{\text{limit}}{}^{2}\right]^{1/3} \tag{6.72}$$

$$\chi_{\text{B}_{\text{eff}}}=0.7\cdot\chi_{\text{B}_{\text{inv}}}+\text{hyp}_1\left\{0.3\cdot\chi_{\text{B}_{\text{inv}}}-\Delta\chi_{\text{B}};\epsilon_5\right\} \tag{6.73}$$

$$B_{\text{eff}}=B_{\text{inv}}\cdot\left(\chi_{\text{B}_{\text{eff}}}\big/\chi_{\text{B}_{\text{inv}}}\right)^{3/2} \tag{6.74}$$

$$P_{\text{inv}}=P_{\text{tun}}\left\{V_{\text{ox}};\,\chi_{\text{B}_{\text{eff}}};\,B_{\text{eff}}\right\} \tag{6.75}$$

$$B^{*}_{\text{inv}}=\frac{3}{8}\cdot\chi_{\text{B}_{\text{eff}}}{}^{-2}\cdot B_{\text{eff}}\cdot\partial V_{\text{ox}} \tag{6.76}$$

$$\xi^{*}=\frac{\xi}{\phi_{\text{T}}\cdot\bar{V}^{*}_{\text{G}_\text{T}}} \tag{6.77}$$

$$\partial V^{*}_{\text{ox}}=\frac{\partial V_{\text{ox}}}{\sqrt{V_{\text{ox}}{}^{2}+V_{\text{limit}}{}^{2}}} \tag{6.78}$$

$$P_{\mathrm{GC}} = 1 + \frac{\left[B^{*}_{\mathrm{inv}}{}^{2} + 4 \cdot B^{*}_{\mathrm{inv}} \cdot \xi^{*} + 2 \cdot B^{*}_{\mathrm{inv}} \cdot \partial V^{*}_{\mathrm{ox}} + 2 \cdot \xi^{*2} + 4 \cdot \partial V^{*}_{\mathrm{ox}} \cdot \xi^{*}\right] \cdot \Delta\psi^{2}}{24} \tag{6.79}$$

$$\bar{I}_{\mathrm{GC}} = I_{\mathrm{GINV}} \cdot G_{\Delta \mathrm{L}} \cdot \left(V_{\mathrm{GS}} - \frac{1}{2} V_{\mathrm{DS_x}}\right) \cdot P_{\mathrm{inv}} \tag{6.80}$$

$$\bar{V}_{\mathrm{inv}} = \frac{V_{\mathrm{inv_0}} + V_{\mathrm{inv_L}}}{2} \tag{6.81}$$

The total intrinsic gate current I_{GC}:

$$I_{\mathrm{GC}} = \bar{I}_{\mathrm{GC}} \cdot \bar{V}_{\mathrm{inv}} \cdot P_{\mathrm{GC}} \tag{6.82}$$

$$\begin{aligned} P_{\mathrm{GS}} = {} & \left[B^{*}_{\mathrm{inv}} + \partial V^{*}_{\mathrm{ox}}\right] \cdot \frac{\Delta\psi}{12} + \Big[B^{*}_{\mathrm{inv}}{}^{2} \cdot \left(B^{*}_{\mathrm{inv}} + 5 \cdot \xi^{*} + 3 \cdot \partial V^{*}_{\mathrm{ox}}\right) \\ & + 2 \cdot \xi^{*2} \cdot \left(B^{*}_{\mathrm{inv}} - \xi^{*} + \partial V^{*}_{\mathrm{ox}}\right) + 10 \cdot B^{*}_{\mathrm{inv}} \cdot \xi^{*} \cdot \partial V^{*}_{\mathrm{ox}}\Big] \cdot \frac{\Delta\psi^{3}}{480} \end{aligned} \tag{6.83}$$

$$I_{\mathrm{GS}} = \frac{1}{2} \cdot I_{\mathrm{GC}} + \left(P_{\mathrm{GS}} \cdot \bar{V}_{\mathrm{inv}} + \frac{V_{\mathrm{inv_0}} - V_{\mathrm{inv_L}}}{12}\right) \cdot \bar{I}_{\mathrm{GC}} + I_{\mathrm{Gov_0}} \tag{6.84}$$

$$I_{\mathrm{GD}} = I_{\mathrm{GC}} - I_{\mathrm{GS}} + I_{\mathrm{Gov_0}} + I_{\mathrm{Gov_L}} \tag{6.85}$$

6.2.3 Extended Charge Equations

Bias-Dependent Overlap Capacitance:

$$Q_{\mathrm{ov_0}} = C_{\mathrm{GSO}} \cdot V_{\mathrm{ov_0}} \tag{6.86}$$

$$Q_{\mathrm{ov_L}} = C_{\mathrm{GDO}} \cdot V_{\mathrm{ov_L}} \tag{6.87}$$

Intrinsic Charges:

$$C_{\mathrm{ox_{eff}}} = \frac{C_{\mathrm{ox}}}{1 + QM_{\mathrm{tox}} \cdot \left[\left(\frac{V_{\mathrm{eff}}}{\eta_{\mathrm{mob}}}\right)^{2} + (20 \cdot \phi_{\mathrm{T}})^{2}\right]^{-1/6}} \tag{6.88}$$

$$V_{\mathrm{GT_0}} = \mathrm{hyp}_1 \left\{V_{\mathrm{G_T}}\left\{\psi^{*}_{\mathrm{s_0}}\right\}; \epsilon_5\right\} \tag{6.89}$$

$$V_{\mathrm{GT_L}} = \mathrm{hyp}_1 \left\{V_{\mathrm{G_T}}\left\{\psi^{*}_{\mathrm{s_L}}\right\}; \epsilon_5\right\} \tag{6.90}$$

$$\bar{V}^{*}_{\mathrm{G_T}} = \frac{V_{\mathrm{GT_0}} + V_{\mathrm{GT_L}}}{2} + \xi \tag{6.91}$$

$$\Delta V_{\mathrm{G_T}} = \frac{V_{\mathrm{GT_0}} - V_{\mathrm{GT_L}}}{2 \cdot \left(1 + \theta_{\mathrm{R}} \cdot \frac{\bar{V}^{*}_{\mathrm{G_T}}}{G_{\mathrm{tot}}}\right)} \tag{6.92}$$

$$F_{\mathrm{j}} = \frac{\Delta V_{\mathrm{G_T}}}{\bar{V}^*_{\mathrm{G_T}}} \tag{6.93}$$

$$Q_{\mathrm{S}} = -\frac{C_{\mathrm{ox_{eff}}}}{2} \cdot \left[\bar{V}^*_{\mathrm{G_T}} + \frac{\Delta V_{\mathrm{G_T}}}{3} \cdot \left(F_{\mathrm{j}} - \frac{F_{\mathrm{j}}{}^2}{5} + 1 \right) - \xi \right] \tag{6.94}$$

$$Q_{\mathrm{D}} = -\frac{C_{\mathrm{ox_{eff}}}}{2} \cdot \left[\bar{V}^*_{\mathrm{G_T}} + \frac{\Delta V_{\mathrm{G_T}}}{3} \cdot \left(F_{\mathrm{j}} + \frac{F_{\mathrm{j}}{}^2}{5} - 1 \right) - \xi \right] \tag{6.95}$$

$$Q_{\mathrm{B}} = -C_{\mathrm{ox_{eff}}} \cdot \left[V_{\mathrm{ox}} - \bar{V}^*_{\mathrm{G_T}} + \xi \right] \tag{6.96}$$

$$Q_{\mathrm{G}} = -\left[Q_{\mathrm{S}} + Q_{\mathrm{D}} + Q_{\mathrm{B}} \right] \tag{6.97}$$

6.2.4 Extended Noise Equations

In these equations f represents the operation frequency of the transistor.

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}} \tag{6.98}$$

$$T_{\mathrm{sat}} = \begin{cases} \theta_{\mathrm{sat}}{}^2 & \text{for NMOS} \\ \frac{\theta_{\mathrm{sat}}{}^2}{\sqrt{1+\theta_{\mathrm{sat}}{}^2 \cdot \Delta\psi^2}} & \text{for PMOS} \end{cases} \tag{6.99}$$

$$R_{\mathrm{ideal}} = \frac{\beta \cdot G_{\mathrm{vsat}}{}^2}{G_{\mathrm{tot}}} \cdot \left[\bar{V}_{\mathrm{G_T}} + \frac{\frac{\Delta\psi^2}{12} - \xi \cdot \left(\bar{V}_{\mathrm{G_T}} - \frac{V_{\mathrm{inv_0}} + V_{\mathrm{inv_L}}}{2} \right)}{V_{\mathrm{G_T}} + \xi} \right] \tag{6.100}$$

$$S_{\mathrm{th}} = \frac{N_{\mathrm{T}}}{G_{\mathrm{mob}}{}^2} \cdot \left(R_{\mathrm{ideal}} - T_{\mathrm{sat}} \cdot I_{\mathrm{DS}} \cdot \Delta\psi \right) \tag{6.101}$$

$$N_0 = \frac{\epsilon_{ox}}{q t_{ox}} \cdot V_{\mathrm{inv_0}} \tag{6.102}$$

$$N_L = \frac{\epsilon_{ox}}{q t_{ox}} \cdot V_{\mathrm{inv_L}} \tag{6.103}$$

$$N^* = \frac{\epsilon_{ox}}{q t_{ox}} \cdot \xi \tag{6.104}$$

$$S_{\mathrm{fl}} = \frac{q \cdot \phi_{\mathrm{T}}{}^2 \cdot t_{ox} \cdot \beta \cdot I_{\mathrm{DS}}}{f \cdot \epsilon_{ox} \cdot G_{\mathrm{mob}} \cdot N^*} \cdot \left[\left(N_{\mathrm{FA}} - N^* \cdot N_{\mathrm{FB}} + N^{*2} \cdot N_{\mathrm{FC}} \right) \cdot \ln \frac{N_0 + N^*}{N_L + N^*} \right.$$

$$\left. + \left(N_{\mathrm{FB}} - N^* \cdot N_{\mathrm{FC}} \right) \cdot \left(N_0 - N_L \right) + \frac{N_{\mathrm{FC}}}{2} \cdot \left(N_0{}^2 - N_L{}^2 \right) \right] \tag{6.105}$$

$$+\frac{\phi_{\mathrm{T}}\cdot {I_{\mathrm{DS}}}^2}{f}\cdot(1-G_{\Delta L})\cdot\left[\frac{N_{\mathrm{FA}}+N_{\mathrm{FB}}\cdot N_L+N_{\mathrm{FC}}\cdot {N_L}^2}{(N_L+N^*)^2}\right]$$

$$S_{\mathrm{ig}} = \begin{cases} \frac{\frac{1}{3}\cdot N_{\mathrm{T}}\cdot\left(2\cdot\pi\cdot f\cdot C_{\mathrm{ox}}\right)^2/g_{\mathrm{m}}}{1+0.075\cdot\left(2\cdot\pi\cdot f\cdot C_{\mathrm{ox}}/g_{\mathrm{m}}\right)^2} & \text{for:}\quad \mathrm{GATENOISE}=0 \\ 0 & \text{for:}\quad \mathrm{GATENOISE}=1 \end{cases} \tag{6.106}$$

$$\rho_{\mathrm{igth}} = 0.4\mathrm{j} \tag{6.107}$$

$$S_{\mathrm{igth}} = \rho_{\mathrm{igth}}\cdot\sqrt{S_{\mathrm{ig}}\cdot S_{\mathrm{th}}} \tag{6.108}$$

7 Parameter Extraction

7.1 Parameter Extraction Method

The parameter extraction for MOS Model 11 using an **optimization method** is described step–by–step in the scheme below. The equations used for the parameter extraction are the basic equations of section 2. It should be noticed that for the *p*–channel MOSFET all voltage and current values have to change sign upon entering the optimization program as a *p*–MOST is treated as an equivalent *n*–MOST. The bias conditions to be used for the measurements are dependent on the supply voltage of the process. Of course it is advisable to restrict the range of voltages to this supply voltage V_{sup}. Otherwise physical effects, atypical for normal transistor operation and therefore less well described by MOS Model 11, may dominate the characteristics.

The simultaneous determination of all parameters is not advisable, because the value of some parameters can be wrong due to correlation and suboptimization. Therefore it is more practical to split the parameters into several groups, and, for each group, to measure the dc-characteristics according to the indicated conditions and to determine the specific parameters. Although the poly-depletion effect affects the dc-behaviour of a MOSFET, the poly-depletion parameter KPINV can only be determined accurately from C-V-measurements. If the (physical) oxide thickness t_{ox} and the polysilicon impurity concentration N_P are known, the parameter KPINV ($= 1/k_P$) can be calculated from[7]:

$$k_P = \frac{t_{ox} \cdot \sqrt{2 \cdot q \cdot \epsilon_{Si} \cdot N_P}}{\epsilon_{ox}} \tag{7.1}$$

If the polysilicon impurity concentration N_P is not known, as a good first-order estimate one can use $N_P = 1 \cdot 10^{26} \mathrm{m}^{-3}$ for n^+-polysilicon gates and $N_P = 5 \cdot 10^{25} \mathrm{m}^{-3}$ for p^+-polysilicon gates. In the latter case a measured C_{GG}-V_{GS}-characteristic for a long-channel transistor is essential for an accurate determination of KPINV.

Before the optimization is started a parameter set has to be determined which contains a first estimation of the parameters to be extracted and the parameters which remain constant. The value of ϕ_T is calculated from the device temperature T_{KD} according to eq. (5.48). The value of smoothing factor m is calculated from the device length L and from the minimum feature size of the technology L_{min} using eq. (5.23). The above equation is rounded off to an integer value.

The parameter set used as a first-order estimation of the parameters to be extracted is given in Table 7.1. With this parameter set a first optimization following the scheme below, is performed. After this the new parameter set serves as an estimation for the second optimization, which is performed following the same scheme. This method yields a proper set of parameters after the second optimization. Experiments with transistors of different processes show that the parameter set does not change very much after a third optimization.

The parameter extraction routine consists of five different dc-measurements and one (optional) capacitance measurement:

• **Measurement I :** $I_D/g_m/I_G$–V_{GS}-characteristics in linear region:
n–channel : V_{GS} = 0 ... V_{sup} (with steps of maximum 50 mV).
V_{DS} = 50 mV
V_{BS} = 0 ... $-V_{sup}$

[7] For metal gates the poly-depletion effect does not occur and in this case KPINV = 0.

Table 7.1: Starting miniset parameter values for parameter extraction of a typical MOS transistor with channel length L (m), channel width W (m), oxide thickness t_{ox} (m) and polysilicon impurity concentration N_P (m^{-3}) at room temperature. If the polysilicon concentration N_P is not known, one can use $N_P = 1{\cdot}10^{26}m^{-3}$ or $5{\cdot}10^{25}m^{-3}$ for n^+- resp. p^+-polysilicon gates. Parameters C_{ox}, C_{GSO} and C_{GDO} are only important for the charge model, and do not affect the dc-model; they have to be extracted from C-V-characteristics. In order to determine the geometry-scaling of parameters, the last column indicates for which conditions the parameters have to be extracted: L=long-channel device (fixed for short-channel devices), S=short-channel devices, A=all devices and F=fixed parameter.

Parameter	Program Name	Parameter Value		Extracted for
		NMOS	PMOS	
V_{FB}	VFB	-1.1	-0.95	L
k_0	KO	0.25	0.25	A
$1/k_P$	KPINV	$6.0 \cdot 10^3 \big/ \left(t_{ox} \cdot \sqrt{N_P}\right)$	$6.0 \cdot 10^3 \big/ \left(t_{ox} \cdot \sqrt{N_P}\right)$	L
ϕ_B	PHIB	0.95	0.95	A
β	BET	$1.7 \cdot 10^{-12} \big/ t_{ox} \cdot W/L$	$4.5 \cdot 10^{-13} \big/ t_{ox} \cdot W/L$	A
θ_{sr}	THESR	$1.5 \cdot 10^{-9} \big/ t_{ox}$	$2.3 \cdot 10^{-9} \big/ t_{ox}$	L
θ_{ph}	THEPH	$1.3 \cdot 10^{-10} \big/ t_{ox}$	$2.2 \cdot 10^{-10} \big/ t_{ox}$	L
η_{mob}	ETAMOB	1.3	3.0	L
ν	NU	2.0	2.0	L
θ_R	THER	$1.3 \cdot 10^{-7} \big/ L$	$8.0 \cdot 10^{-8} \big/ L$	S
θ_{R1}	THER1	0	0	–
θ_{R2}	THER2	1	1	–
θ_{sat}	THESAT	$4.5 \cdot 10^{-7} \big/ L$	$2.0 \cdot 10^{-7} \big/ L$	A
θ_{Th}	THETH	$1.0 \cdot 10^{-6}$	$1.0 \cdot 10^{-6}$	A
σ_{dibl}	SDIBL	$5.0 \cdot 10^{-2} \cdot \left(L_{min} \big/ L\right)^2$	$5.0 \cdot 10^{-2} \cdot \left(L_{min} \big/ L\right)^2$	S
m_0	MO	$1.0 \cdot 10^{-3}$	$1.0 \cdot 10^{-3}$	A
σ_{sf}	SSF	$6.0 \cdot 10^{-2} \cdot L_{min} \big/ L$	$6.0 \cdot 10^{-2} \cdot L_{min} \big/ L$	A
α	ALP	$6.0 \cdot 10^{-2} \cdot L_{min} \big/ L$	$6.0 \cdot 10^{-2} \cdot L_{min} \big/ L$	A
V_P	VP	$5.0 \cdot 10^{-2}$	$1.0 \cdot 10^{-1}$	F
m	MEXP	use Eq. (5.23)	use Eq. (5.23)	–
ϕ_T	PHIT	use Eq. (5.19)	use Eq. (5.19)	–
a_1	A1	25	100	A
a_2	A2	25	37	A
a_3	A3	1	1	A
I_{GINV}	IGINV	$3.0 \cdot 10^{-5} \cdot W \cdot L \big/ t_{ox}{}^2$	$4.0 \cdot 10^{-5} \cdot W \cdot L \big/ t_{ox}{}^2$	A
B_{INV}	BINV	$2.9 \cdot 10^{+10} \cdot t_{ox}$	$4.3 \cdot 10^{+10} \cdot t_{ox}$	L
I_{GACC}	IGACC	$3.0 \cdot 10^{-5} \cdot W \cdot L \big/ t_{ox}{}^2$	$2.0 \cdot 10^{-5} \cdot W \cdot L \big/ t_{ox}{}^2$	A
B_{ACC}	BACC	B_{INV}	$2.9 \cdot 10^{+10} \cdot t_{ox}$	L
V_{FBov}	VFBOV	0.1	0.1	L
k_{ov}	KOV	$9.3 \cdot 10^{+8} \cdot t_{ox}$	$3.8 \cdot 10^{+8} \cdot t_{ox}$	L
I_{GOV}	IGOV	$5.0 \cdot 10^{-13} \cdot W \big/ t_{ox}{}^2$	$5.0 \cdot 10^{-12} \cdot W \big/ t_{ox}{}^2$	A
C_{ox}	COX	$\epsilon_{ox} \big/ t_{ox} \cdot W \cdot L$	$\epsilon_{ox} \big/ t_{ox} \cdot W \cdot L$	–
C_{GDO}	CGDO	$3.0 \cdot 10^{-10} \cdot W$	$3.0 \cdot 10^{-10} \cdot W$	–
C_{GSO}	CGSO	$3.0 \cdot 10^{-10} \cdot W$	$3.0 \cdot 10^{-10} \cdot W$	–

p–channel : V_{GS} = 0 . . . $-V_{sup}$ (with steps of maximum 50 mV).
V_{DS} = -50 mV
V_{BS} = 0 . . . V_{sup}

• **Measurement II :** Subthreshold I_D–V_{GS}-characteristics:
n–channel : $V_{GS} = V_T - 0.6$ V . . . $V_T + 0.3$ V
V_{DS} = 3 values starting from 100 mV to V_{sup}
V_{BS} = 0 . . . $-V_{sup}$

p–channel : $V_{GS} = V_T + 0.6$ V . . . $V_T - 0.3$ V
V_{DS} = 3 values starting from -100 mV to $-V_{sup}$
V_{BS} = 0 . . . V_{sup}

• **Measurement III :** $I_D/g_{DS}/I_G$–V_{DS}-characteristics:
n–channel : V_{DS} = 0 . . . V_{sup} (with steps of maximum 50 mV)
V_{GS} = 4 values starting from $V_T + 0.1$ V, not above V_{sup}
V_{BS} = 3 values starting from 0 V to $-V_{sup}$

p–channel : V_{DS} = 0 . . . $-V_{sup}$ (with steps of maximum 50 mV)
V_{GS} = 4 values starting from $V_T + 0.1$ V, not below $-V_{sup}$
V_{BS} = 3 values starting from 0 V to V_{sup}

• **Measurement IV :** $I_D/I_S/I_G/I_B$–V_{GS}-characteristics in all operation regions:
n–channel : V_{GS} = -V_{sup} . . . V_{sup} (with steps of maximum 50 mV).
V_{DS} = 4 values starting from 0 V to V_{sup}
V_{BS} = 0 V

p–channel : V_{GS} = -V_{sup} . . . $-V_{sup}$ (with steps of maximum 50 mV).
V_{DS} = 4 values starting from 0 V to -V_{sup}
V_{BS} = 0 V

• **Measurement V :** I_B–V_{GS}-characteristics:
n–channel : V_{GS} = 0 . . . V_{sup} (with steps of maximum 50 mV).
V_{DS} = 3 values not above V_{sup}
V_{BS} = 0 V

p–channel : V_{GS} = 0 . . . $-V_{sup}$ (with steps of maximum 50 mV).
V_{DS} = 3 values not below $-V_{sup}$
V_{BS} = 0 V

• **Measurement VI :** C_{gg}–V_{GS}-characteristic (optional):
n/p-channel : $V_{GS} = -V_{sup}$ . . . V_{sup} (with steps of maximum 50 mV).
V_{DS} = 0 V
V_{BS} = 0 V

The values of transconductance g_m and output conductance g_{DS} are extracted from the I–V-characteristics by calculating in a numerical way the derivative of I_D to V_{GS} and V_{DS}, respectively. In the subthreshold measurements, Measurement II, use is made of threshold voltage V_T, which has to be determined for all the used bulk-source bias values V_{BS}. The determination of V_T is rather arbitrary, and it can be either determined using the linear extrapolation method or the constant current criterion.
For an accurate extraction of parameter values, the parameter set for a long-channel transistor has to

be determined first. In the long-channel case the poly-depletion parameter $1/k_P$, the flat-band voltage V_{FB}, the carrier mobility (i.e. θ_{sr}, θ_{ph} and η_{mob}) and the gate tunnelling probability factors (B_{inv} and B_{acc}) can be determined, and they can subsequently be fixed for the short and narrow-channel devices, see Tab. 7.1. In Table 7.2 the extraction procedure for long-channel transistors is given. Since the

Table 7.2: DC-parameter extraction procedure for an n-type long-channel MOS transistor, where Steps 2 and 12 are optional. For p-type transistors all voltages and currents have to be multiplied by -1. The optimization is either performed on the absolute or relative deviation between model and measurements. Parameter I_{tst} is 2.5 μA for NMOS and 0.8 μA for PMOS. The parameter ν is only determined for temperatures unequal to room temperature. For n-type MOS transistors $B_{acc} = B_{inv}$, and as a result B_{acc} does not have to be extracted. For p-type MOS transistors this is not the case, see Tab. 2.1.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/ Relative	Specific Conditions
1	ϕ_B , k_0 , β , θ_{sr}	I	I_D	Absolute	–
2	V_{FB} , k_0 , k_P , C_{ox}	VI	C_{gg}	Relative	–
3	ϕ_B , k_0 , m_0	II	I_D	Relative	–
4	β , θ_{sr} , θ_{ph} , (ν)	I	$I_D \big/ g_m$	Relative	$V_{SB} = 0$ V $V_{GS} > V_T + 0.3$ V
5	η_{mob}	I	I_D	Absolute	$I_D > W/L \cdot I_{tst}$
6	θ_{sat}	III	I_D	Absolute	–
7	σ_{sf} , α , θ_{Th}	III	g_{DS}	Relative	–
8	θ_{sat}	III	I_D	Absolute	–
9	I_{GINV} , B_{inv}	I	I_G	Absolute	–
10	I_{GOV} , (B_{acc}) , I_{GACC} , k_{ov}	IV	I_G	Absolute	$V_{GS} < 0$ V
11	a_1 , a_2 , a_3	V	I_B	Absolute	–
12	V_{FB} , k_P , C_{ox}	VI	C_{gg}	Relative	–
13	Repeat Steps 3, 4, 5, 6, 7, 8, 9, 10 and 11				

value of body-factor k_0 may change much over geometry and over technology, the first-order estimate in Tab. 7.1 is very crude and a more accurate, preliminary value is obtained using Step 1. In Step 2 (optional) more accurate values of the poly-depletion parameter $1/k_P$ and the flat-band voltage V_{FB} (which determines the onset of accumulation) are extracted. Next the subthreshold parameters ϕ_B, k_0 and m_0 are optimized in Step 3, neglecting short-channel effects such as drain-induced barrier-lowering (DIBL). After that the mobility parameters are optimized using Steps 4 and 5, neglecting the influence of series-resistance. In Step 6 a preliminary value of the velocity saturation parameter is obtained, and subsequently the conductance parameters σ_{sf}, α and θ_{Th} are determined in Step 7. A more accurate value of θ_{sat} can now be obtained using Step 8. The gate current parameters are determined in Steps 9 and 10. Finally the weak-avalanche parameters are optimized in Step 11.

For short-channel devices the values of the poly-depletion parameter $1/k_P$, flat-band voltage V_{FB}, the carrier mobility parameters (θ_{sr}, θ_{ph} and η_{mob}) and the gate tunnelling probability factors (B_{inv} and B_{acc}) of the long-channel device are copied, and next the extraction procedure as given in Table7.3 is executed. In contrast to the long-channel case, the extraction procedure for short-channel devices

Table 7.3: DC-Parameter extraction procedure for an n-type short-channel MOS transistor. For p-type transistors all voltages and currents have to be multiplied by -1. Parameters $1/k_P$, V_{FB}, θ_{sr}, θ_{ph}, η_{mob}, B_{inv}, B_{acc} and k_{ov} are taken from the long-channel case. The optimization is either performed on the absolute or relative deviation between model and measurements.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/ Relative	Specific Conditions
1	ϕ_B , k_0 , β , θ_R	I	I_D	Absolute	–
2	ϕ_B , k_0 , m_0 , σ_{dibl}	II	I_D	Relative	–
3	β , θ_R	I	$I_D \big/ g_m$	Relative	$V_{SB} = 0$ V $V_{GS} > V_T + 0.3$ V
4	θ_{sat}	III	I_D	Absolute	–
5	σ_{sf} , α , θ_{Th} , σ_{dibl}	III	g_{DS}	Relative	–
6	θ_{sat}	III	I_D	Absolute	–
7	I_{GINV} , I_{GOV} , I_{GACC}	IV	I_G	Absolute	–
8	a_1 , a_2 , a_3	V	I_B	Absolute	–
9	Repeat Steps 2, 3, 4, 5, 7 and 8				

also optimizes the parameters for series-resistance[8] and DIBL.

AC-parameters: The AC-parameters C_{ox}, C_{GSO}, C_{GDO}, k_{ov} and V_{FBov} cannot be (accurately) determined from DC-characteristics, and as a consequence they have to be determined from C–V–characteristics. Since normal MOS transistors are symmetrical devices, one can assume that the oxide capacitance of the source and drain extension are identical, which implies that C_{GSO}=C_{GDO}. The oxide capacitance of the intrisic MOSFET C_{ox} can be extracted from Measurement VI. For an accurate determination of the bias-dependent overlap capacitances C_{GSO} (=C_{GDO}), k_{ov} and V_{FBov}, the following C-V-measurements have to be done:

• **Measurement VII :** C_{dg}–V_{GS}-characteristic:
n–channel : $V_{GS} = -V_{sup} \ldots 0$ (with steps of maximum 50 mV)
V_{DS} = 0 V
V_{SB} = 0 V

p–channel : $V_{GS} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV)
V_{DS} = 0 V
V_{SB} = 0 V

• **Measurement VIII :** C_{gd}–V_{DS}-characteristic (optional):
n–channel : V_{GB} = 0 V
V_{DS} = 0 V
$V_{SB} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV)

p–channel : V_{GB} = 0 V

[8] Note that in Table 7.3 parameters θ_{R1} and θ_{R2} are not included, which implies that the series-resistance is assumed to be voltage-independent. This holds true for modern CMOS technologies, where no use is made of LDD-structures.

V_{DS} = 0 V
$V_{SB} = -V_{sup} \ldots 0$ (with steps of maximum 50 mV)

In Table 7.4 the extraction procedure for the AC-parameters is given.

Table 7.4: AC-parameter extraction procedure for a MOS transistor. Here it is assumed that $C_{GSO} = C_{GDO}$. In the first instance flat-band voltage V_{FBov} is not optimised, although it may be optimised during Step 1 in order to obtain more accurate results. The optimization is either performed on the absolute or relative deviation between model and measurements.

Step	Optimised Parameters	Measurement	Fitted On	Absolute/ Relative	Specific Conditions
1	k_{ov} , C_{GSO}	VII / VIII	C_{gd}/C_{dg}	Relative	–
2	C_{ox}	VI	C_{gg}	Relative	–
3	Repeat Steps 1 and 2				

7.2 Scaling of Parameters

Using the scaling relations of Chapter 5 it is possible to calculate a parameter set for a process, given the parameter set of typical transistors of this process. To accomplish this, transistors of different lengths, widths and at different temperatures have to be measured. With the results of these measurements the sensitivities of the parameters on length, width and temperature can be found.

For the determination of a geometry-scaled parameter set a three-step procedure is recommended:

1. determine minisets (ϕ_B, k_0, β, ...) for all measured devices, as explained in Section 7.1.

2. the width and length sensitivity coefficients are optimized by fitting the appropriate geometry scaling rules to these miniset parameters.

3. finally the width and length sensitivity coefficients are optimized by fitting the result of the scaling rules and current equations to the measured currents of all devices simultaneously.

An important part of the above-described parameter extraction is the determination of ΔL and ΔW, see eqs. (5.1) and (5.2), since it affects both the DC- and the AC-model. Traditionally ΔW can be determined from the extrapolated zero-crossing in the β versus mask width W characteristic. In a similar way ΔL can be determined from the $1/\beta$ versus mask length L characteristic. For modern MOS devices with pocket implants, however, it has been found that the above ΔL extraction method is no longer valid [18]. Another, more accurate method is to measure the gate-to-bulk capacitance C_{GB} in accumulation for different channel lengths [19]. In this case the extrapolated zero-crossing in the C_{GB} versus mask length L curve will give ΔL.

For the determination of a temperature-scaled parameter set a three-step procedure is recommended:

1. determine minisets at various temperature values (at least three) for the corner devices, i.e. the long/broad, the long/narrow, the short/broad and the short/narrow channel transistor.

2. the temperature sensitivity coefficients are optimized by fitting the appropriate temperature scaling rules to these miniset parameters.

3. finally the temperature sensitivity coefficients are optimized by fitting the result of the scaling rules and current equations to the measured currents of the corner devices simultaneously.

Parameter sets have been determined for several processes using this parameter extraction strategy and taking care of not exceeding the supply voltage. For all processes good results have been obtained.

8 Pstar Specific Items

8.1 Syntax

n-channel geometrical model	:	MN_n (D,G,S,B)	<parameters>
p-channel geometrical model	:	MP_n (D,G,S,B)	<parameters>
n-channel electrical model	:	MNE_n (D,G,S,B)	<parameters>
p-channel electrical model	:	MPE_n (D,G,S,B)	<parameters>

n	:	occurrence indicator
<parameters>	:	list of model parameters

D, G, S and B are drain, gate, source and bulk terminals respectively.

8.2 Pstar Specific Values

The default values and clipping values as used by **Pstar** for the parameters of the geometrical MOS Model 11 (*n*-**channel**) are listed below.

No.	Parameter	Units	Default	Clip low	Clip high
0	LEVEL	-	1100	-	-
1	LER	m	1.0×10^{-6}	1.0×10^{-10}	-
2	WER	m	1.0×10^{-5}	1.0×10^{-10}	-
3	LVAR	m	0.000	-	-
4	LAP	m	4.0×10^{-8}	-	-
5	WVAR	m	0.000	-	-
6	WOT	m	0.000	-	-
7	TR	^{o}C	21.0	-273.15	-
8	VFBR	V	-1.050	-	-
9	STVFB	VK^{-1}	0.5×10^{-3}	-	-
10	KOR	$V^{1/2}$	0.500	-	-
11	SLKO	$V^{1/2}m$	0.000	-	-
12	SL2KO	$V^{1/2}m^{2}$	0.000	-	-
13	SWKO	$V^{1/2}m$	0.000	-	-
14	KPINV	$V^{-1/2}$	0.000	-	-
15	PHIBR	V	0.950	-	-
16	SLPHIB	Vm	0.000	-	-
17	SL2PHIB	Vm^{2}	0.000	-	-
18	SWPHIB	Vm	0.000	-	-
19	BETSQ	AV^{-2}	3.709×10^{-4}	-	-
20	ETABET	-	1.300	-	-
21	FBET1	-	0.000	-	-
22	LP1	m	0.8×10^{-6}	1.0×10^{-10}	-
23	FBET2	-	0.000	-	-
24	LP2	m	0.8×10^{-6}	1.0×10^{-10}	-

No.	Parameter	Units	Default	Clip low	Clip high
25	THESRR	V^{-1}	0.400	-	-
26	SWTHESR	m	0.000	-	-
27	THEPHR	V^{-1}	1.29×10^{-2}	-	-
28	ETAPH	-	1.750	-	-
29	SWTHEPH	m	0.000	-	-
30	ETAMOBR	-	1.40	-	-
31	STETAMOB	K^{-1}	0.000	-	-
32	SWETAMOB	m	0.000	-	-
33	NUR	-	1.000	-	-
34	NUEXP	-	5.250	-	-
35	THERR	V^{-1}	0.155	1.0×10^{-10}	-
36	ETAR	-	0.950	-	-
37	SWTHER	m	0.000	-	-
38	THER1	V	0.000	-	-
39	THER2	V	1.000	-	-
40	THESATR	V^{-1}	0.500	-	-
41	SLTHESAT	-	1.000	-	-
42	THESATEXP	-	1.000	0.000	-
43	ETASAT	-	1.040	-	-
44	SWTHESAT	m	0.000	-	-
45	THETHR	V^{-3}	1.0×10^{-3}	-	-
46	THETHEXP	-	1.000	0.000	-
47	SWTHETH	m	0.000	-	-
48	SDIBLO	$V^{-1/2}$	2.0×10^{-3}	-	-
49	SDIBLEXP	-	1.350	-	-
50	MOR	-	0.000	-	-
51	MOEXP	-	1.340	-	-
52	SSFR	$V^{-1/2}$	6.25×10^{-3}	-	-

No.	**Parameter**	**Units**	**Default**	**Clip low**	**Clip high**
53	SLSSF	m	1.0×10^{-6}	-	-
54	SWSSF	m	0.000	-	-
55	ALPR	-	1.0×10^{-2}	-	-
56	SLALP	-	1.000	-	-
57	ALPEXP	-	1.000	0.000	-
58	SWALP	m	0.000	-	-
59	VP	V	5.0×10^{-2}	-	-
60	LMIN	m	1.5×10^{-7}	1.0×10^{-10}	-
61	A1R	-	6.000	-	-
62	STA1	K^{-1}	0.000	-	-
63	SLA1	m	0.000	-	-
64	SWA1	m	0.000	-	-
65	A2R	V	38.00	-	-
66	SLA2	Vm	0.000	-	-
67	SWA2	Vm	0.000	-	-
68	A3R	-	1.000	-	-
69	SLA3	m	0.000	-	-
70	SWA3	m	0.000	-	-
71	IGINVR	AV^{-2}	0.000	0.000	-
72	BINV	V	48.00	0.000	-
73	IGACCR	AV^{-2}	0.000	0.000	-
74	BACC	V	48.00	0.000	-
75	VFBOV	V	0.000	-	-
76	KOV	$V^{1/2}$	2.500	1.0×10^{-12}	-
77	IGOVR	AV^{-2}	0.000	0.000	-
78	TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
79	COL	Fm^{-1}	3.2×10^{-10}	-	-
80	GATENOISE	-	0.000	0.000	1.000

No.	Parameter	Units	Default	Clip low	Clip high
81	NTR	J	1.656×10^{-20}	-	-
82	NFAR	$V^{-1}m^{-4}$	1.573×10^{22}	-	-
83	NFBR	$V^{-1}m^{-2}$	4.752×10^{8}	-	-
84	NFCR	V^{-1}	0.000	-	-
85	L	m	2.000×10^{-6}	-	-
86	W	m	1.000×10^{-5}	-	-
87	DTA	K	0.000	-	-
88	MULT	-	1.000	0.000	-

The default values and clipping values as used by **Pstar** for the parameters of the geometrical MOS Model 11 (p-**channel**) are listed below.

No.	**Parameter**	**Units**	**Default**	**Clip low**	**Clip high**
0	LEVEL	-	1100	-	-
1	LER	m	1.0×10^{-6}	1.0×10^{-10}	-
2	WER	m	1.0×10^{-5}	1.0×10^{-10}	-
3	LVAR	m	0.000	-	-
4	LAP	m	4.0×10^{-8}	-	-
5	WVAR	m	0.000	-	-
6	WOT	m	0.000	-	-
7	TR	^{o}C	21.0	-273.15	-
8	VFBR	V	-1.050	-	-
9	STVFB	VK^{-1}	0.5×10^{-3}	-	-
10	KOR	$\mathrm{V}^{1/2}$	0.500	-	-
11	SLKO	$\mathrm{V}^{1/2}\mathrm{m}$	0.000	-	-
12	SL2KO	$\mathrm{V}^{1/2}\mathrm{m}^2$	0.000	-	-
13	SWKO	$\mathrm{V}^{1/2}\mathrm{m}$	0.000	-	-
14	KPINV	$\mathrm{V}^{-1/2}$	0.000	-	-
15	PHIBR	V	0.950	-	-
16	SLPHIB	Vm	0.000	-	-
17	SL2PHIB	Vm^2	0.000	-	-
18	SWPHIB	Vm	0.000	-	-
19	BETSQ	AV^{-2}	1.150×10^{-4}	-	-
20	ETABET	-	0.500	-	-
21	FBET1	-	0.000	-	-
22	LP1	m	0.8×10^{-6}	1.0×10^{-10}	-
23	FBET2	-	0.000	-	-
24	LP2	m	0.8×10^{-6}	1.0×10^{-10}	-

No.	Parameter	Units	Default	Clip low	Clip high
25	THESRR	V^{-1}	0.730	-	-
26	SWTHESR	m	0.000	-	-
27	THEPHR	V^{-1}	1.0×10^{-3}	-	-
28	ETAPH	-	1.750	-	-
29	SWTHEPH	m	0.000	-	-
30	ETAMOBR	-	3.000	-	-
31	STETAMOB	K^{-1}	0.000	-	-
32	SWETAMOB	m	0.000	-	-
33	NUR	-	1.000	-	-
34	NUEXP	-	3.230	-	-
35	THERR	V^{-1}	0.080	1.0×10^{-10}	-
36	ETAR	-	0.400	-	-
37	SWTHER	m	0.000	-	-
38	THER1	V	0.000	-	-
39	THER2	V	1.000	-	-
40	THESATR	V^{-1}	0.200	-	-
41	SLTHESAT	-	1.000	-	-
42	THESATEXP	-	1.000	0.000	-
43	ETASAT	-	0.860	-	-
44	SWTHESAT	m	0.000	-	-
45	THETHR	V^{-3}	0.5×10^{-3}	-	-
46	THETHEXP	-	1.000	0.000	-
47	SWTHETH	m	0.000	-	-
48	SDIBLO	$V^{-1/2}$	1.0×10^{-3}	-	-
49	SDIBLEXP	-	1.350	-	-
50	MOR	-	0.000	-	-
51	MOEXP	-	1.340	-	-
52	SSFR	$V^{-1/2}$	6.25×10^{-3}	-	-

No.	Parameter	Units	Default	Clip low	Clip high
53	SLSSF	m	1.0×10^{-6}	-	-
54	SWSSF	m	0.000	-	-
55	ALPR	-	1.0×10^{-2}	-	-
56	SLALP	-	1.000	-	-
57	ALPEXP	-	1.000	0.000	-
58	SWALP	m	0.000	-	-
59	VP	V	5.0×10^{-2}	-	-
60	LMIN	m	1.5×10^{-7}	1.0×10^{-10}	-
61	A1R	-	6.000	-	-
62	STA1	K^{-1}	0.000	-	-
63	SLA1	m	0.000	-	-
64	SWA1	m	0.000	-	-
65	A2R	V	38.00	-	-
66	SLA2	Vm	0.000	-	-
67	SWA2	Vm	0.000	-	-
68	A3R	-	1.000	-	-
69	SLA3	m	0.000	-	-
70	SWA3	m	0.000	-	-
71	IGINVR	AV^{-2}	0.000	0.000	-
72	BINV	V	87.50	0.000	-
73	IGACCR	AV^{-2}	0.000	0.000	-
74	BACC	V	48.00	0.000	-
75	VFBOV	V	0.000	-	-
76	KOV	$V^{1/2}$	2.500	1.0×10^{-12}	-
77	IGOVR	AV^{-2}	0.000	0.000	-
78	TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
79	COL	Fm^{-1}	3.2×10^{-10}	-	-
80	GATENOISE	-	0.000	0.000	1.000

No.	Parameter	Units	Default	Clip low	Clip high
81	NTR	J	1.656×10^{-20}	-	-
82	NFAR	$V^{-1}m^{-4}$	3.825×10^{23}	-	-
83	NFBR	$V^{-1}m^{-2}$	1.015×10^{8}	-	-
84	NFCR	V^{-1}	7.300×10^{-9}	-	-
85	L	m	2.000×10^{-6}	-	-
86	W	m	1.000×10^{-5}	-	-
87	DTA	K	0.000	-	-
88	MULT	-	1.000	0.000	-

The default values and clipping values as used by **Pstar** for the parameters of the electrical MOS Model 11 (*n*-**channel**) are listed below.

No.	**Parameter**	**Units**	**Default**	**Clip low**	**Clip high**
0	LEVEL	-	1100	-	-
1	VFB	V	-1.0500	-	-
2	KO	$V^{1/2}$	0.5000	1.0×10^{-12}	-
3	KPINV	$V^{-1/2}$	0.0000	0.000	-
4	PHIB	V	0.9500	1.0×10^{-12}	-
5	BET	AV^{-2}	1.9215×10^{-3}	0.000	-
6	THESR	V^{-1}	0.3562	1.0×10^{-12}	-
7	THEPH	V^{-1}	1.29×10^{-2}	1.0×10^{-12}	-
8	ETAMOB	-	1.4000	0.000	-
9	NU	-	2.0000	1.000	-
10	THER	V^{-1}	8.12×10^{-2}	0.000	-
11	THER1	V	0.0000	0.000	-
12	THER2	V	1.0000	0.000	-
13	THESAT	V^{-1}	0.2513	0.000	-
14	THETH	V^{-3}	1.0×10^{-5}	0.000	-
15	SDIBL	$V^{-1/2}$	8.53×10^{-4}	1.0×10^{-12}	-
16	MO	V	0.0000	0.000	0.500
17	SSF	$V^{-1/2}$	0.0120	1.0×10^{-12}	-
18	ALP	-	0.0250	0.000	-
19	VP	V	0.0500	1.0×10^{-12}	-
20	MEXP	-	5.0000	1.000	-
21	PHIT	V	2.663×10^{-2}	1.0×10^{-12}	-
22	A1	-	6.0221	0.000	-
23	A2	V	38.017	1.0×10^{-12}	-
24	A3	-	0.6407	0.000	-

No.	Parameter	Units	Default	Clip low	Clip high
25	IGINV	AV^{-2}	0.0000	0.000	-
26	BINV	V	48.000	0.000	-
27	IGACC	AV^{-2}	0.0000	0.000	-
28	BACC	V	48.000	0.000	-
28	VFBOV	V	0.0000	-	-
29	KOV	$V^{1/2}$	2.5000	1.0×10^{-12}	-
31	IGOV	AV^{-2}	0.0000	0.000	-
32	COX	F	2.98×10^{-14}	0.000	-
23	CGDO	F	6.392×10^{-15}	0.000	-
34	CGSO	F	6.392×10^{-15}	0.000	-
35	GATENOISE	-	0.0000	0.000	1.000
36	NT	J	1.656×10^{-20}	0.000	-
37	NFA	$V^{-1}m^{-4}$	8.323×10^{22}	1.0×10^{-12}	-
38	NFB	$V^{-1}m^{-2}$	2.514×10^{7}	-	-
39	NFC	V^{-1}	0.0000	-	-
40	TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
41	MULT	-	1.0000	0.000	-

The default values and clipping values as used by **Pstar** for the parameters of the electrical MOS Model 11 (p-**channel**) are listed below.

No.	Parameter	Units	Default	Clip low	Clip high
0	LEVEL	-	1100	-	-
1	VFB	V	-1.0500	-	-
2	KO	$V^{1/2}$	0.5000	1.0×10^{-12}	-
3	KPINV	$V^{-1/2}$	0.0000	0.000	-
4	PHIB	V	0.9500	1.0×10^{-12}	-
5	BET	AV^{-2}	3.8140×10^{-4}	0.000	-
6	THESR	V^{-1}	0.7300	1.0×10^{-12}	-
7	THEPH	V^{-1}	0.0010	1.0×10^{-12}	-
8	ETAMOB	-	3.0000	0.000	-
9	NU	-	2.0000	1.000	-
10	THER	V^{-1}	7.90×10^{-2}	0.000	-
11	THER1	V	0.0000	0.000	-
12	THER2	V	1.0000	0.000	-
13	THESAT	V^{-1}	0.1728	0.000	-
14	THETH	V^{-3}	0.000	0.000	-
15	SDIBL	$V^{-1/2}$	3.551×10^{-5}	1.0×10^{-12}	-
16	MO	V	0.0000	0.000	0.500
17	SSF	$V^{-1/2}$	0.0100	1.0×10^{-12}	-
18	ALP	-	0.0250	0.000	-
19	VP	V	0.0500	1.0×10^{-12}	-
20	MEXP	-	5.0000	1.000	-
21	PHIT	V	2.663×10^{-2}	1.0×10^{-12}	-
22	A1	-	6.8583	0.000	-
23	A2	V	57.324	1.0×10^{-12}	-
24	A3	-	0.4254	0.000	-

No.	Parameter	Units	Default	Clip low	Clip high
25	IGINV	AV^{-2}	0.0000	0.000	-
26	BINV	V	87.500	0.000	-
27	IGACC	AV^{-2}	0.0000	0.000	-
28	BACC	V	48.000	0.000	-
28	VFBOV	V	0.0000	-	-
29	KOV	$V^{1/2}$	2.5000	1.0×10^{-12}	-
31	IGOV	AV^{-2}	0.0000	0.000	-
32	COX	F	2.717×10^{-14}	0.000	-
33	CGDO	F	6.358×10^{-15}	0.000	-
34	CGSO	F	6.358×10^{-15}	0.000	-
35	GATENOISE	-	0.0000	0.000	1.000
36	NT	J	1.656×10^{-20}	0.000	-
37	NFA	$V^{-1}m^{-4}$	1.900×10^{22}	1.0×10^{-12}	-
38	NFB	$V^{-1}m^{-2}$	5.043×10^{6}	-	-
39	NFC	V^{-1}	3.627×10^{-10}	-	-
40	TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
41	MULT	-	1.0000	0.000	-

8.3 DC Operating Point Output

The DC operating point output facility gives information on the state of a device at its operation point. Besides terminal currents and voltages, the magnitudes of linearized internal elements are given. In some cases meaningful quantities can be derived which are then also given (e.g. f_T). The objective of the DC operating point facility is twofold:

- Calculate small-signal equivalent circuit element values
- Open a window on the internal bias conditions of the device and its basic capabilities.

Below the printed items are described. Here $C_{x(y)}$ indicates the derivative of the charge Q at terminal x to the voltage at terminal y, when all other terminals remain constant.

No.	Symbol	Program Name	Units	Description
0	$I_{\rm DS}$	IDS	A	Drain current, excl. avalanche and tunnel currents
1	$I_{\rm avl}$	IAVL	A	Substrate current due to weak-avalanche
2	$I_{\rm GS}$	IGS	A	Gate-to-source current due to direct tunnelling
3	$I_{\rm GD}$	IGD	A	Gate-to-drain current due to direct tunnelling
4	$I_{\rm GB}$	IGB	A	Gate-to-bulk current due to direct tunnelling
5	$V_{\rm DS}$	VDS	V	Drain-source voltage
6	$V_{\rm GS}$	VGS	V	Gate-source voltage
7	$V_{\rm SB}$	VSB	V	Source-bulk voltage
8	$V_{\rm TO}$	VTO	V	Zero-bias threshold voltage: $V_{\rm TO} = V_{\rm FB} + P_{\rm D} \cdot (\phi_{\rm B} + 2 \cdot \phi_{\rm T}) + k_0 \cdot \sqrt{\phi_{\rm B} + 2 \cdot \phi_{\rm T}}$
9	$V_{\rm TS}$	VTS	V	Threshold voltage including back-bias effects: $V_{\rm TS} = V_{\rm FB} + P_{\rm D} \cdot \left(V_{\rm SB_t} + 2 \cdot \phi_{\rm T}\right) - \left(V_{\rm SB_t} - \phi_{\rm B}\right) + k_0 \cdot \sqrt{V_{\rm SB_t} + 2 \cdot \phi_{\rm T}}$
10	$V_{\rm TH}$	VTH	V	Threshold voltage including back-bias and drain-bias effects: $V_{\rm TH} = V_{\rm FB} + P_{\rm D} \cdot \left(V_{\rm SB_t} + 2 \cdot \phi_{\rm T}\right) - \left(V_{\rm SB_t} - \phi_{\rm B}\right) + k_0 \cdot \sqrt{V_{\rm SB_t} + 2 \cdot \phi_{\rm T}} - \Delta V_{\rm G}$
11	$V_{\rm GT}$	VGT	V	Effective gate drive voltage including back-bias and drain voltage effects: $V_{\rm GT} = V_{\rm inv_0}$
12	$V_{\rm DSAT}$	VDSS	V	Drain saturation voltage at actual bias
13	$V_{\rm DS_{eff}}$	VSAT	V	Saturation limit: $V_{\rm DS_{eff}} = V_{\rm DS} - V_{\rm DSAT}$
14	$g_{\rm m}$	GM	A/V	Transconductance (assumed $V_{\rm DS} > 0$): $g_{\rm m} = \partial I_{\rm DS} \big/ \partial V_{\rm GS}$
15	$g_{\rm mb}$	GMB	A/V	Substrate-transconductance (assumed $V_{\rm DS} > 0$): $g_{\rm mb} = \partial I_{\rm DS} \big/ \partial V_{BS}$
16	$g_{\rm ds}$	GDS	A/V	Output conductance: $g_{\rm ds} = \partial I_{\rm DS} \big/ \partial V_{\rm DS}$
17	$C_{\rm D(D)}$	CDD	F	$C_{\rm D(D)} = \partial Q_{\rm D} \big/ \partial V_{\rm DS}$

No.	**Symbol**	**Program Name**	**Unit**	**Description**
18	$C_{D(G)}$	CDG	F	$C_{D(G)} = -\partial Q_D / \partial V_{GS}$
19	$C_{D(S)}$	CDS	F	$C_{D(S)} = C_{D(D)} - C_{D(G)} - C_{D(B)}$
20	$C_{D(B)}$	CDB	F	$C_{D(B)} = \partial Q_D / \partial V_{SB}$
21	$C_{G(D)}$	CGD	F	$C_{G(D)} = -\partial Q_G / \partial V_{DS}$
22	$C_{G(G)}$	CGG	F	$C_{G(G)} = \partial Q_G / \partial V_{GS}$
23	$C_{G(S)}$	CGS	F	$C_{G(S)} = C_{G(G)} - C_{G(D)} - C_{G(B)}$
24	$C_{G(B)}$	CGB	F	$C_{G(B)} = \partial Q_G / \partial V_{SB}$
25	$C_{S(D)}$	CSD	F	$C_{S(D)} = -\partial Q_S / \partial V_{DS}$
26	$C_{S(G)}$	CSG	F	$C_{S(G)} = -\partial Q_S / \partial V_{GS}$
27	$C_{S(S)}$	CSS	F	$C_{S(S)} = C_{S(G)} + C_{S(D)} + C_{S(B)}$
28	$C_{S(B)}$	CSB	F	$C_{S(B)} = \partial Q_S / \partial V_{SB}$
29	$C_{B(D)}$	CBD	F	$C_{B(D)} = -\partial Q_B / \partial V_{DS}$
30	$C_{B(G)}$	CBG	F	$C_{B(G)} = -\partial Q_B / \partial V_{GS}$
31	$C_{B(S)}$	CBS	F	$C_{B(S)} = C_{B(B)} - C_{B(D)} - C_{B(G)}$
32	$C_{B(B)}$	CBB	F	$C_{B(B)} = -\partial Q_B / \partial V_{SB}$
33	$C_{GD_{ov}}$	CGDOL	F	Gate-drain overlap capacitance of the actual transistor: $C_{GD_{ov}} = -\partial Q_{ov_L} / \partial V_{DS}$
34	$C_{GS_{ov}}$	CGSOL	F	Gate-source overlap capacitance of the actual transistor: $C_{GS_{ov}} = \partial Q_{ov_0} / \partial V_{GS}$
35	W_E	WEFF	m	Effective channel width for geometrical models
36	L_E	LEFF	m	Effective channel length for geometrical models
37	u	U	-	Transistor gain: $u = g_m / g_{ds}$
38	R_{out}	ROUT	Ω	Small-signal output resistance: $R_{out} = 1 / g_{ds}$
39	V_{Early}	VEARLY	V	Equivalent Early voltage: $V_{Early} = \lvert I_{DS} \rvert / g_{ds}$
40	k_{eff}	KEFF	$\sqrt{V}$	Body effect parameter: $k_{eff} = k_0$
41	β_{eff}	BEFF	A/V^2	Gain factor: $\beta_{eff} = 2 \cdot \lvert I_{DS} \rvert / {V_{inv_0}}^2$
42	f_T	FUG	Hz	Unity gain frequency at actual bias: $f_T = \frac{g_m}{2\pi\left(C_{G(G)}+C_{GS_{ov}}+C_{GD_{ov}}\right)}$
43	$\sqrt{S_{V_{G\,th}}}$	SQRTSFW	$V/\sqrt{Hz}$	Input-referred RMS white noise voltage density: $\sqrt{S_{V_{G\,th}}} = \sqrt{S_{th}} / g_m$
44	$\sqrt{S_{V_{G\,fl}}}$	SQRTSFF	$V/\sqrt{Hz}$	Input-referred RMS white noise voltage density at 1 kHz: $\sqrt{S_{V_{G\,fl}}} = \sqrt{S_{fl}(1\mathrm{kHz})} / g_m$
45	f_{knee}	FKNEE	Hz	Cross-over frequency above which white noise is dominant: $f_{knee} = 1\mathrm{Hz} \cdot S_{fl}(1\mathrm{Hz}) / S_{th}$

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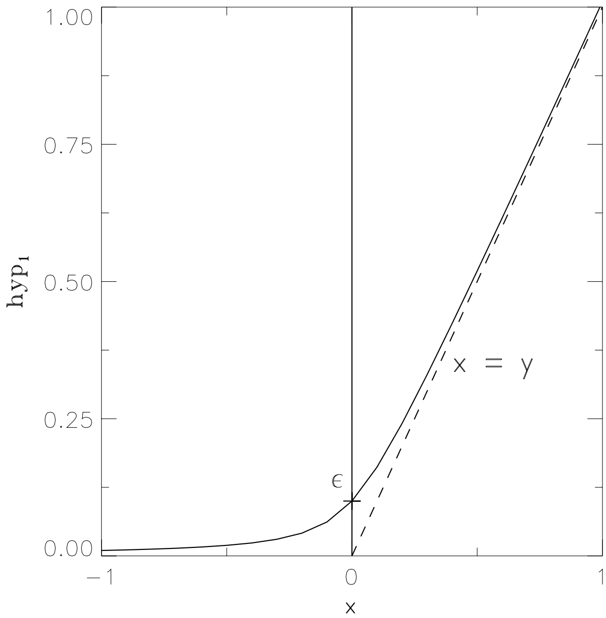
A Auxiliary Equations



$$\mathrm{hyp}_1\left\{x;\epsilon\right\} = \frac{1}{2}\cdot\left(x+\sqrt{x^2+4\cdot\epsilon^2}\right) \tag{A.1}$$