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CMOS Integration using Low Thermal Budget Dopant-Segregated Metallic S/D Junctions on Thin-Body SOI

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As segregated PtSi contacts using implant-through-silicide technique have been studied. A thermal activation at 600°C gives a As pile-up at the PtSi/Si interface of $4x10^{20}$ cm^{-3} resulting in a Schottky barrier to electrons below 0.1 eV. As and B segregated PtSi contacts have been integrated in a low temperature CMOS process and functional 90 nm inverters have been demonstrated. Inverters with nearly ideal DC voltage transfer characteristics and large voltage gains have been obtained down to 0.5V of supply voltage with excellent noise margins ($\sim V_{DD}/2$). This approach provides a low temperature S/D module suitable for a viable and low-cost manufacturing approach for future CMOS technology nodes.

1-Introduction:

As CMOS technology is entering in the decananometre era, the contact resistance associated to the silicide/silicon interface is identified as one of the biggest challenge to solve in order to preserve current drive capabilities. In that context, source/drain (S/D) engineering takes an increasing importance in the development of leading edge CMOS generations because of the increasing impact of S/D series resistances on transistor performance (1). Thin-body MOSFET architectures associated to upcoming technology nodes are expected to deliver a higher current drive at shallower junction depth and reduced silicide thickness. As a result, extremely severe constraints are placed on the junction and contact technologies. In order to address these challenges (i.e. low specific contact resistance, abrupt highly doped junction), one alternative is to operate on lowly doped silicon and to use silicide contacts that present a very low Schottky barrier height (SBH) to electrons and holes for n-type and p-types MOSFETs, respectively. Considering that the equivalent SBH should not exceed 0.1 eV in order to position SB-MOSFETs advantageously with respect to conventional technology (2), low temperature dopant segregation (DS) at the Schottky interface has emerged as a sound technological solution, for digital and high frequency applications (3-5). The most advantageous methodology is to combine a band-edge silicide to its appropriate dopant type. In that way, p-type MOSFETs with boron segregated PtSi contacts have been demonstrated (6-7). Conversely, a conduction band-edge silicide coupled to segregated donor impurities is desirable for n-MOSFETs (8). However, this last approach faces two major obstacles: i) the integration of a second silicide material and ii) difficulties to process high quality rare-earth silicides layers (9-10). Although, a material like PtSi that presents a large SBH

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to electrons is theoretically not attractive for n-MOS devices, it proved to produce a near 0.1eV when combined to As segregation (11-12). Although dopant segregated contacts in complementary MOS were previously published based on midgap silicides (13-14), *implantation-before-silicidation* (IBS) and high temperature activation suppressed the advantage of low temperature processing. In this paper, As segregated PtSi contacts are studied through a material approach and their impacts on the electrical properties at the device level are shown based on the so-called *implant-through-silicide* (ITS) flavour down to sub-100nm gate length. Functional elementary inverters based on As and B segregated PtSi contacts are demonstrated in both DC and transient modes using a single low temperature activation approach (15).

2- SB height modulation: experiments and characterization:

After a 1% HF dip to de-oxidize the silicon surface (n-type (100) Si wafers), a 15 nm thick Pt layer was deposited using e-beam evaporation and the subsequent silicidation reaction was activated by rapid thermal annealing (RTA) at 350°C for 3 min before As^+ implantation at 20 keV with a dose of 10^{15} cm^{-2}. A RTA post-anneal activates the mechanism of As segregation. The advantage associated to the ITS technique is to confine dopants in the silicide without the generation of defects, thus enhancing the segregation effect governed by solid solubility and diffusion mechanisms. It is speculated that dopants can be incorporated in substitutional sites in an extremely localized silicon slice that greatly enhances current injection by tunneling. Fig. 1-a) shows the arsenic profiles obtained by top-SIMS on the ITS samples. The as-implanted sample features a peak of arsenic concentration located in the upper part of the silicide layer and almost all the dose is confined in the silicide layer. The segregation has been activated with a post RTA annealed during 5 min in N_2 at various temperatures from 400°C to 700°C. At 400°C, the As species are diffusing in the layer and are beginning to accumulate at the PtSi/Si interface. At 500°C, the dopant pile-up is visible. This is all the more true up to 500°C, but without an exponential effect. Fig. 1-b) shows the evolution of the As concentration at the PtSi/Si interface and the total dose as function of activation temperature. A post annealing activation, even at a moderate temperature (i.e 400°C) leads to a drastic increase of the As peak at the silicide/silicon interface, from $1x10^{18}$ cm^{-3}, without activation to $6x10^{19}$ cm^{-3} at 400°C. The accumulation is better with activation at 500°C, with a concentration around $3x10^{20}$ cm^{-3}. Up to 500°C, the maximum peak at the interface saturates around $4x10^{20}$ cm^{-3}. The total dose implanted remained in the sample until the temperature of 500°C. Higher temperatures lead to a slight loss of dose (18% at 600°C and 34 % at 700°C) due to outdiffussion outside the top surface enhanced with the temperature.

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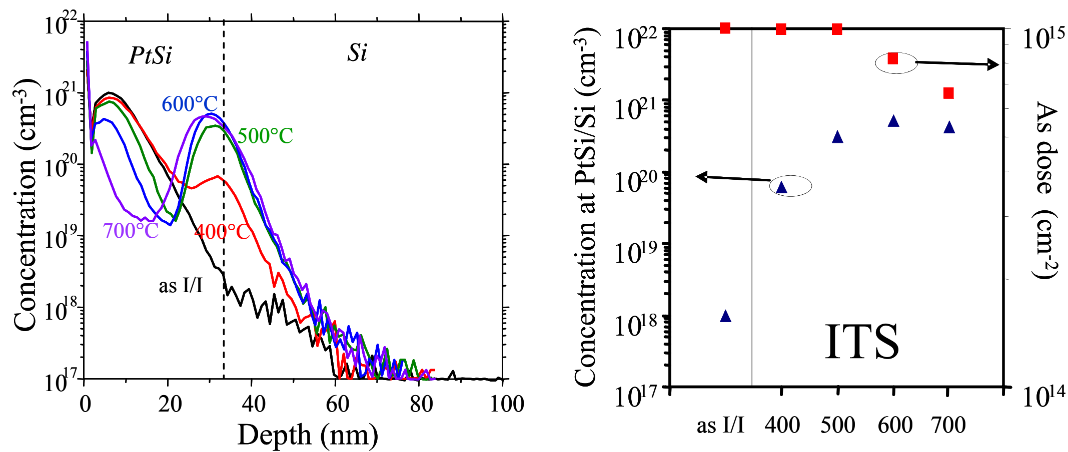

Figure 1: Top SIMS profiles of arsenic concentration: a) Effect of the post annealing activation b) Evolution of the As concentration at the PtSi/Si interface and the total dose in the sample for ITS scheme (function of activation temperature).

For the sake of Schottky barrier measurement, simple metallic junctions were fabricated on lowly doped (10 Ω.cm) n-type (100) Si wafers. The dedicated test structures consisted in 1000µm^2 square silicided contacts separated by a micrometer gap defined by lithography to produce back-to-back junctions. Based on this configuration, Schottky barrier heights were determined using an extraction procedure that couples experimental data to a transport model that accounts for thermionic and tunnel emission as well as barrier lowering due to image charge induction (16). Fig. 2-a) presents an example of Arrhenius plots representative of the lowest Schottky barriers to electrons (Φ_{bn}) obtained with ITS approach activated at 700°C. The high temperature section of the Arrhenius characteristics is governed by the series resistance of the silicon gap between contacts. The I/T^2 vs 1/T characteristics exhibit a maximum that demarcates the regime governed by the silicon series resistance at high temperature from the regime driven by the contact resistance at low temperature (77°K), consistent with the extraction of a very low SBH (70 meV). In order to get a better overview, Fig. 2-b) proposes the different extracted barrier heights obtained from the different activation conditions. As expected, a large SBH for electrons (0.87 eV) is measured for a dopant-free PtSi control sample. The impact of post-annealing temperature of the ITS technique is very significant. While the ITS technique post-annealed at 300°C exhibits a barrier height of 0.61 eV, this barrier is reduced by 50% with an annealing 100°C higher. However, as the annealing temperature increases, the SBH decreases down to 80 meV for an annealing temperature of 600°C and 70 meV for an annealing temperature of 700°C. Although the mechanisms of dopant redistribution and of partial activation are not yet fully clarified, it is speculated that arsenic can be incorporated in substitutional sites in an extremely localized silicon slice. From the electrical transport standpoint, the above mechanism can be viewed as the activation of a quasi-Dirac distribution of dopants that greatly enhances current injection through a tunneling mechanism.

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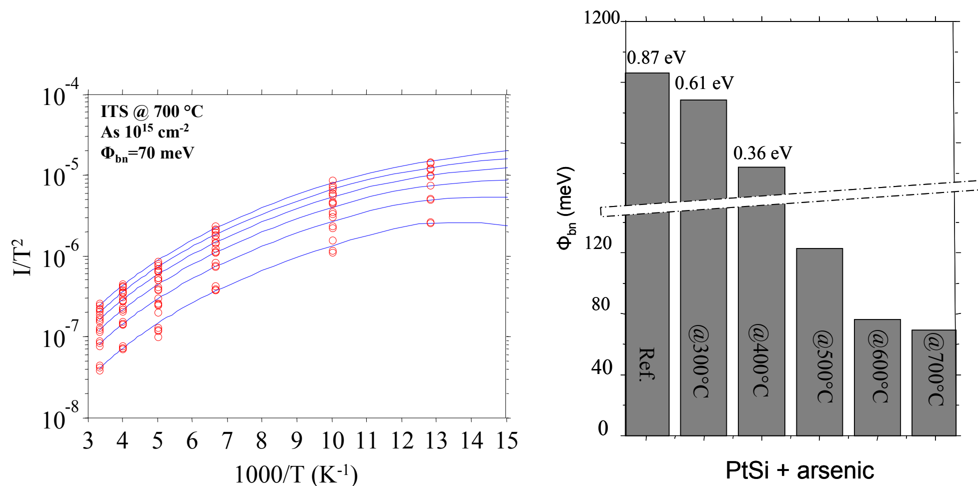

Figure 2: a) Arrhenius plots representative of the lowest Schottky barriers to electrons (Φ_{bn}) obtained with ITS implementation activated at 700°C b) Summary of SB heights to electrons with As segregation on PtSi contacts using ITS scheme activated with temperatures from 300°C to 700°C.

3- n-MOS performance:

First, the (100)-oriented SOI substrates (p-type doped 4-10 Ω.cm) were thinned from 50 nm down to 15 nm by chemical etching (17). The active part of the device is isolated by a classical MESA technique that generates a trench in the silicon film down to the buried silicon oxide using an anisotropic fluorine RIE etching step. A gate oxide of 2.4 nm was subsequently formed by dry oxidation at 725°C followed by tungsten deposition using e-beam evaporation. The gate was defined by e-beam lithography using an inorganic negative tone resist (Hydrogen Silsesquioxane - HSQ). After exposure and hard bake, HSQ holds the remarkable property to evolve from a cage-like monomer to a network-like polymer that approaches the structure of SiO_2. Therefore, after patterning the gate by RIE etching using a SF_6/N_2 chemistry (18), the residual HSQ covering the tungsten gate was not removed but used as a capping layer. A 15 nm thick nitride layer was then deposited by PECVD to ensure a conformal coverage over the gate. An anisotropic RIE etching step was subsequently used to define 15 nm wide spacers. According to this process sequence, the two sidewall nitride spacers and the residual HSQ resist on the top ensure a complete encapsulation of the metal gate. Lastly, S/D metal junctions were realized using a self-aligned silicide process. A thin platinum layer (5 to 10 nm thick) was evaporated after an HF dip used to remove the residual gate oxide. Pt was deposited only on the active part of the device using a conventional lift-off process step. The silicidation reaction was activated by rapid thermal annealing at 350°C during 3 min under N_2/H_2. The unreacted Pt layer covering the gate perimeter was removed in a diluted hot aqua-reggia solution. At this stage of the process sequence, several options have been evaluated, based on implant-to-silicide (ITS) with several activation conditions in order to further reduce the Schottky barrier height. Finally, HSQ covering the gate pads was removed by an HF dip and a 500 nm Al thick layer was patterned on the source/drain and on the gate regions. The following part of the section reports on the implementation of the dopant segregation technique in n-type SB-MOSFETs and on the evaluation of its impact on the device performance. To obtain a fair comparison and to evaluate the

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benefit of the annealing step on SBH reduction, electrical measurements have been performed by probing directly on the S/D silicided regions. Fig. 3-a) presents the I_d-V_g curves, obtained on devices with gate lengths of 240 nm. After As implantation, RTA activation at 500°C was realized. I_d-V_g characteristic exhibits a strong influence of a high Schottky barrier height that limits the injection of carriers at the source/channel junction. Such a behavior associated to a 240 nm gate length is the clear signature of an excessive SBH. The off-state current is high (~90 nA/µm) with a strong ambipolar behavior in the negative gate voltage branch. Consistently, the current drive is very limited (~4 µA/µm at V_g=V_d=2V). The characteristic of the same device is proposed after an additional RTA activation at 600°C. Quasi ideal characteristics are obtained, revealing that the decrease of the Schottky barrier height is very efficient. In particular, current flattening on the I_d-V_g characteristics at the transition between the subthreshold and the weak accumulation regime is not detected, regardless of the channel length. The current is not limited by the contact resistance and the channel resistance tends to dominate the total conductance of the device. As a result, the current drive is improved: with a maximum saturation I_{on} of 286 µA/µm at V_g=V_d=2V. The off-state current is also reduced (8 nA/µm) but an ambipolar behavior is still noticeable. Lastly, no additional benefit on the transfer characteristic is observed with a higher activation temperature.

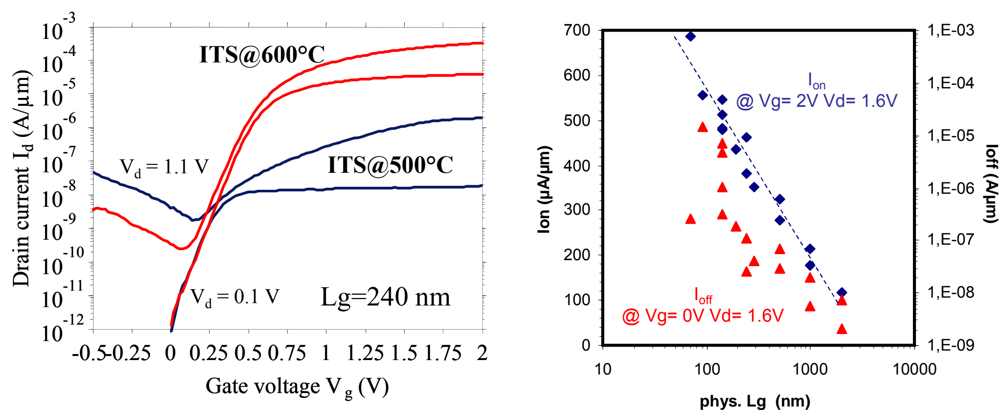

Figure 3: a) I-V characteristics of 240 nm gate long n-type SB-MOSFETs, with As dopant segregated (ITS) PtSi S/D contacts activated at 500°C or 600°C b) Electrical performance (I_{on} and I_{off}) of SB-nMOSFETs with As DS on PtSi contacts fabricated on a moderately doped SOI channel as a function of the gate length.

Fig. 3-b) shows the on-state saturation current and off-state leakage current as a function of the physical gate length. I_{on} is found inversely proportional to the gate length, indicating that the S/D series resistances do not exert an overwhelming current limitation. The average I_{on} at L_g=100 nm is 580 µA/µm for V_d=1.6V and V_g=2V. The channel resistance tends to dominate the total resistance and the current is not limited by the contact resistance. The off-state current seems to increase with gate length reduction starting from the nA/µm range. The As-DS junctions do not degrade the immunity against short channel effects (not shown). The subthreshold swing remains close to the 80 mV/dec regardless the considered gate length, from long channel to 70 nm gate length.

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The DIBL is very well controlled for gate lengths above 100 nm (~40mV/V) and remains in the acceptable range of 100 mV/V below 100 nm.

4 - CMOS integration:

Finally, SB-CMOS devices with dopant segregation using a low temperature budget have been performed. This approach overcomes the two major blocks to the implementation of Schottky source / drain region in large scale: the use of a unique silicide for both types with barrier height less than 0.1eV. One single silicide coupled to a low temperature S/D module offers an effective, viable and low-cost manufacturing approach for future technology nodes of complementary MOSFETs: (i) low cost and simple procedure using a low thermal budget process (no high temperature activation of dopants) compatible with the introduction of new thermally sensitive materials (ii) performance: thanks to its very low barrier heights for holes and electrons, contact resistance is minimized.
The main process steps are schematized in Fig. 4-a), which begins with the formation of isolation areas and the gate of transistors that includes a thin thermal oxide with a tungsten metal gate. Thin dielectric spacers are subsequently integrated on each side of the gate. Platinum silicide is formed on S/D regions of n-type and p-type transistors. Then group III dopants (e.g. boron) are confined into the silicide by ion implantation to achieve p-type contacts, the complementary transistor (n-type) being protected by an isolated layer. The reciprocal approach is followed for the n-type transistor using group V elements (e.g. arsenic). Finally, a unique annealing step at low temperature (<700°C) is used to segregate dopants at the interface between the silicide and the semiconductor. Indeed, the evolution of the Schottky barrier height with the annealing temperature, presented in Fig. 2-b) for n-type and in (6) for p-type, shows that activation at 600°C is enough to provide a SBH below 0.1 eV for both p- and n-type.

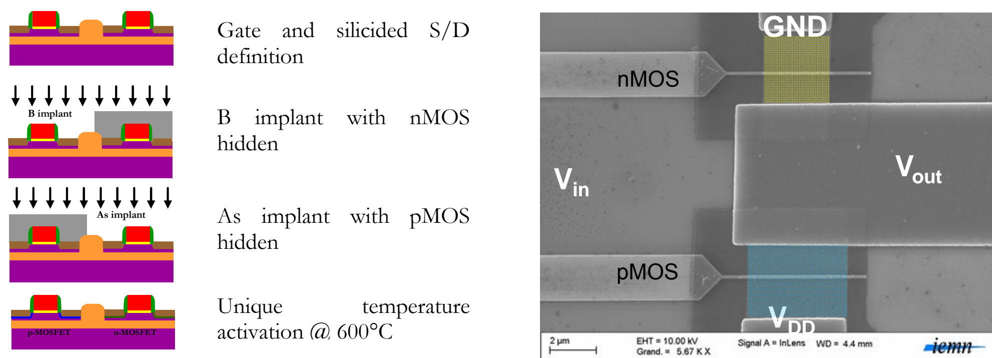

Figure 4: a) Process flow and b) aerial SEM picture of DS-SB CMOS using a single silicide and a unique activation step at low temperature. Device architecture features a 16 nm thick SOI channel, a 2.4 nm SiO_2 gate oxide, a metallic tungsten gate 15 nm wide SiN spacers and 12 nm PtSi metallic S/D junctions.

Fig. 4-b) presents an aerial SEM view of a DS SB-CMOSFETs, composed of n-MOS on the top and p-MOS at the bottom. The yellow and blue regions are the implantation windows for arsenic and boron implants, respectively. It is worth noting that a mesa separate the two transistors in order to prevent the diffusion of dopants in the wrong device. Fig. 5-a) shows the static I_d-V_g of a typical 90 nm gate long transistor where the

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current drives for n- and p-type devices is 501/316µA/µm at V_{DD}=1.1V (with $|V_g|$=2V to account for the 2.4 nm gate oxide thickness) have been obtained.. In conventional CMOS circuitry, the width W of p-MOS transistor is typically 2-2.5X larger than for n-MOSFETs. In the present case, the gate widths of the n-MOS and p-MOS are 3µm and 4.5µm respectively to obtain symmetry in basic circuit operation.
Fig. 5-b) presents the static transfer characteristics V_{out}-V_{in} of the inverter for V_{DD} from 0.5V to 2.5V with a step of 0.25V. A very good behavior is obtained with perfectly defined high state and low state separated by a narrow transition zone down to 0.5V of supply voltage. The noise margins have been evaluated by plotting V_{in} and V_{out} interchangeably on the x- and y-axes as shown in Fig. 5-c) at various V_{DD} (0.5V, 1.25V and 2.5V). The high level noise margin (NM_H= V_{OH}-V_{IH}) and the low level noise margin (NM_L= V_{OL}-V_{IL}) are close to V_{DD}/2. Finally, the dynamic response at 10 MHz of a 90nm CMOS inverter (Fig. 5-d) shows excellent regenerative properties.

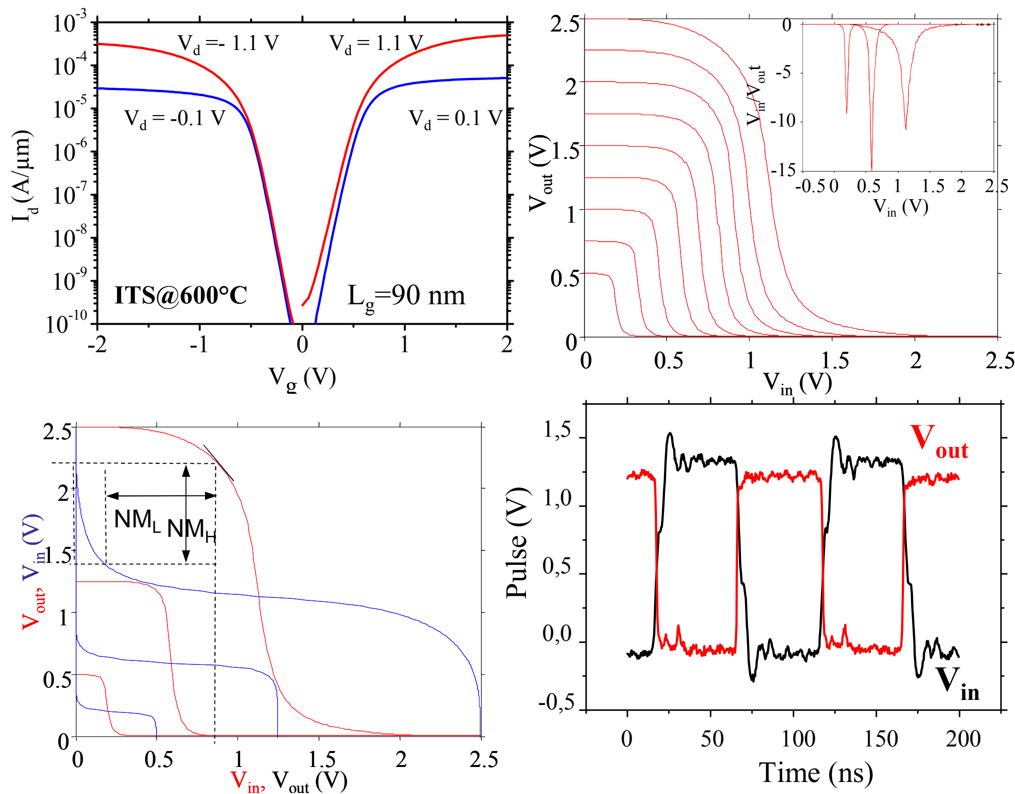

Figure 5: (a) Static I_d-V_g characteristics of 90 nm gate long SB-MOSFET. (b) Transfer static characteristics of a 90 nm gate long inverter at different V_{DD} (from 0.5V to 2.5V with a step of 0.25 V). In inset, the voltage gain at 3 different V_{DD} (0.5V, 1.25V and 2.5V). (c) Transfer static characteristics at 3 different V_{DD} (0.5V, 1.25V and 2.5V) with the evaluation of the noise margins. (d) Dynamic (pulse) response of 90 nm gate length SB-MOSFET inverter at V_{DD}=1.2V.

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5 - Conclusion:

This approach provides a low temperature S/D module suitable for a viable and low-cost manufacturing approach for future CMOS technology nodes. In summary, one major improvement compared to the conventional ohmic contact is to reach similar performance with a huge process simplification. Conventional transistor architectures in the sub-22nm regime require junctions with ultrasharp doping concentration gradient. This imposes the development of very sophisticated annealing techniques and also leads to tight thermal constraints on constituent materials. Conversely, the proposed integration scheme can be qualified as a cold process, without high temperature dopants activation, that leverages many constraints associated to the integration of innovative gate stacks comprising high-k dielectric and metal gate.

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