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Impact of Localized Channel and Field Implantation on Data Retention Time for Gigabit Density DRAM Technology

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As the density of dynamic random access memories (DRAMs) enters into giga-bit regime with deep sub-quarter-micrometer feature size, the control of junction leakage current at storage node becomes much more important because of increased channel doping concentration. In this paper, we analyzed the junction leakage current of cell transistor and suggested effective cell structure to improve the data retention time for mass-produced 512 Mb DRAM with 0.12 μm. This cell structure, which is based on localized channel and field implantation, reduces the junction leakage current by relaxing junction doping profile and implantation damages at source and drain regions. The relaxed junction profile can reduce the electric field strength of a junction and thus improve data retention time in DRAMs. In addition, subthreshold characteristics of a cell transistor are improved dramatically with this scheme by increasing threshold voltage of corner transistor that is generally lowered by boron segregation and field crowding at the shallow trench isolation boundary in the conventional cell transistor. The proposed approach reduced the cumulative fail-bit probability by about 80% at the data retention time of 128 ms and possibly, can be applied to future high density DRAMs with feature size down to 0.1 μm range.
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Improvement of data retention time is one of the most serious issues for practical realization of giga-bit density dynamic random access memory (DRAM), affecting the performance of power consumption and speed of DRAM. As the memory density continues to increase, the data retention time has nearly doubled for each generation due to the requirement of high speed and low power consumption, as shown in Fig. 1.[1] For example, refresh time of 256M DRAM is about twice as long as that of 64M DRAM to keep constant refresh interval 15.6 μs. Many challenges have been attempted to improve DRAM data retention characteristics. As the cell isolation pitch and cell transistor dimension continue to decrease, doping concentration at Si substrate should be increased to suppress short channel effect including punch through between neighboring cell node and subthreshold leakage current in cell transistor. When the channel length of cell transistor is scaled down to less than 0.13 μm, the substrate doping concentration should be increased more than 1×10^{18} cm^{-3} to obtain a threshold voltage of around 1.0 V.[2] High doping level leads to the increase of junction leakage current, which inevitably degrades the data retention time.[3] Recently, the leakage mechanism in DRAM cells has been experimentally and theoretically studied by several authors, and it has been reported that the major failure in the refresh operation of DRAM cells is due to extremely large junction leakage current from locally enhanced electric field and trap-assisted anomalous current in depletion region.[4-7] Hence, in order to improve the data retention time via the reduction of junction leakage current, it is necessary to reduce the generation of interface state and maximum electric field strength at cell junction. However, it is very difficult to decrease the electric field and to control the process induced trap generation without sacrificing the performance of cell transistor.

Trend of device scaling predicts that the isolation space for future generation will be down to about 0.13 and 0.1 μm for 1 Gb and 4 Gb DRAM, respectively.[8] This progressive scaling tells us that the shallow trench isolation (STI) process will be even more critical for good device characteristics. It has been reported that STI processing may induce silicon defects in an STI boundary[9] and that these defects can enhance boron segregation, which degrades the subthreshold characteristics of cell transistors.[10] To achieve good refresh characteristics, the leakage current through cell transistor as well as the leakage current through cell node junction must be reduced.

In this paper, we analyze the measured leakage current into several cell junction leakage components using the designed test structures to find out where the leakage current is coming from and how much the portion of each component is. Taking the results for the junction leakage components into consideration, we fabricate a cell transistor using localized channel and field implantation (LOCFI) technology, which can improve the data retention time by the suppression of the ion implantation damage at the storage node. The results for device simulations and experiments for a 512 Mb DRAM adopting proposed cell transistor with 0.12 μm design rule are also discussed.

Classification of Junction Leakage Components at the Storage Node

The leakage currents at cell node consist of source/drain junction leakage (I_J), transistor subthreshold leakage (I_{OFF}), capacitor dielectric leakage (I_{CAP}), and interlayer leakage current (I_{IL}) as shown in Fig. 2a. Among the components of leakage currents at the storage node, the junction leakage current is the major one as shown

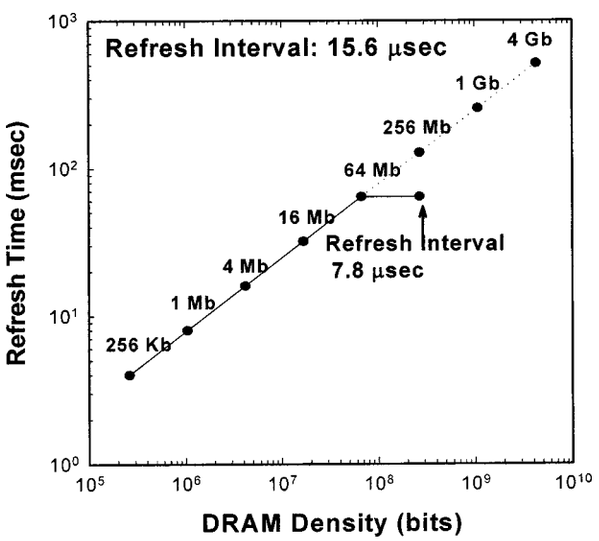

Figure 1. Variation of refresh time to keep a constant refresh interval. The refresh time for 256 Mb and 1 Gb DRAM will be 128 ms and 256 ms, respectively, if the refresh interval of 15.6 μs is maintained. Otherwise, the refresh interval should be decreased.

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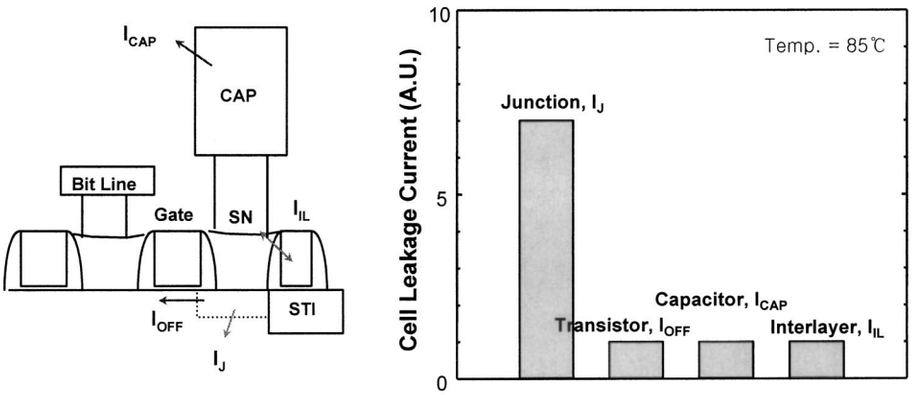

Figure 2. (a) Cross-sectional diagram showing the possible leakage mechanisms and (b) relative portion of each leakage current at the storage node in DRAM cells. Among the leakage mechanisms of junction leakage, leakage through the transfer transistor, capacitor dielectric leakage, and interlayer dielectric leakage, the junction current is a dominant factor in the leakage mechanism. SN and CAP in the Fig. 2a represent storage node and capacitor, respectively.

in Fig. 2b and will be much more important for higher density DRAM. In order to reduce the junction leakage current that acts as an obstacle in extending data retention time, it is very important to find out where the leakage is coming from (bulk, active edge etc.) and how much the portion of each current is.

Figure 3 is the vertical SEM image of DRAM cells with shallow trench isolation (STI) using a 0.12 μm design rule. As shown in the Fig. 3, cell junction leakage current can be divided into five components, which are listed as gate/active border line current (I_{GA}), storage node area current (I_{SN}), gate/field border line current (I_{GF}), and two self-aligned contact, SAC/field border line currents (I_{SF1},I_{SF2}), respectively. We established four test patterns to investigate each component, which are area-type active pattern without gate (type I), peripheral-type active without gate (type II), area-type active with gate (type III), and peripheral-type active with gate (type IV) as shown in Fig. 4.

From these test patterns, respective leakage components can be extracted. For example, the I_{SN} can be estimated from type I as illustrated in Fig. 5. With additional phosphorus implantation, the surface of type I became fully inverted to n-type region as shown in Fig. 5b and the measured leakage current was decreased significantly. Because SAC/active border line current was not affecting total junction leakage current any more, only storage node area current, I_{SN}, contributed to the junction leakage current. The amount of reduced leakage current is inferred to be defect-site or deep-trap assisted tunneling[11,12] or thermionic field emission assisted by deep traps.[1] By analogy, each unit area of type II, type III, and type IV approximately contained the ($I_{SN} + 2I_{SF}$), ($I_{SN} + 2I_{GA}$), and ($I_{SN} + 2I_{GA} + 2I_{SF}$), respectively. Keeping this relationship in mind, we evaluated the relative portion of each component to total junction leakage current. Figure 6 shows the cell junction leakage current reduced to its component. As shown in the figure, the relative portions of I_{GA}, I_{SN}, I_{GF}, and $2I_{SF}$ to total junction leakage current amounted to 24, 12, 14, and 50%, respectively, which implies that the peripheral junction leakage current at STI corner and gate border line on the active has a dominant influence on the data retention time rather than the areal storage node junction leakage current. Therefore, it is strongly recommended to reduce the electric field in the depletion region and the process damage during the formation of STI, gate, and SAC.

Experimental

From the viewpoint of reducing the aforementioned junction leakage components, a 512 Mb DRAM based on a LOCFI cell transistor and capacitor-over-bit line (COB) structure has been fabricated using 0.12 μm process technology. The key process feature is listed in Table I: 0.25 μm deep STI with Si_3N_4 liner and high-density-plasma (HDP) oxide filling, retrograde triple well, W-polycide gate stack, self-aligned contact etching for the formation of bit-line and storage node contact pad, and Al_2O_3-based cell capacitor.[13]

Figure 7 illustrates the process flow of LOCFI transistors. Silicon trench with 0.25 μm depth and controlled slope was formed by reactive ion etching using the predeposited pad oxide and Si_3N_4 hard mask. After the pull-back of Si_3N_4 until the silicon active top region was exposed, 20 keV boron was implanted vertically on both the active edge and STI bottom as shown in Fig. 7a. The pull-back of Si_3N_4 was performed by slight wet etching in H_3PO_4 etchant.

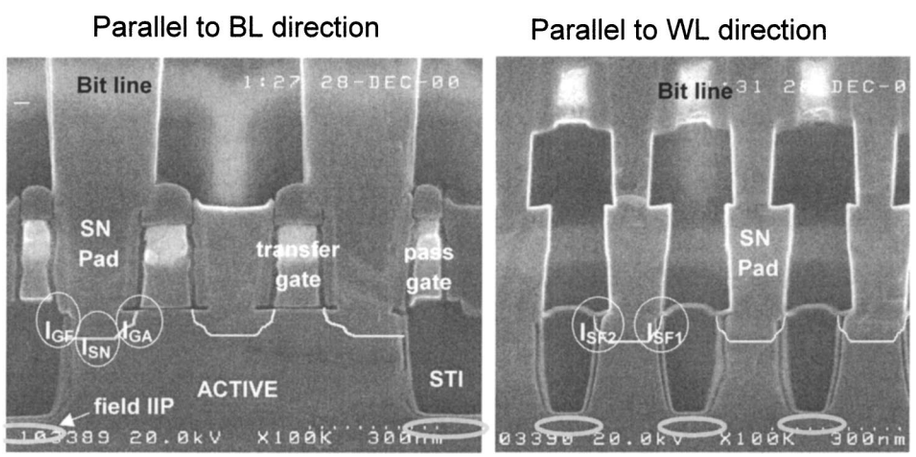

Figure 3. SEM photograph showing vertical structure of the cell array with STI, tungsten polycide gate, and self-aligned poly-Si plugged storage node pad, and so on. Cell junction leakage components of gate/active border line current (I_{GA}), storage node area current (I_{SN}), gate/field border line current (I_{GF}), and two SAC/field border line currents (I_{SF1},I_{SF2}), respectively, are marked on the photograph.

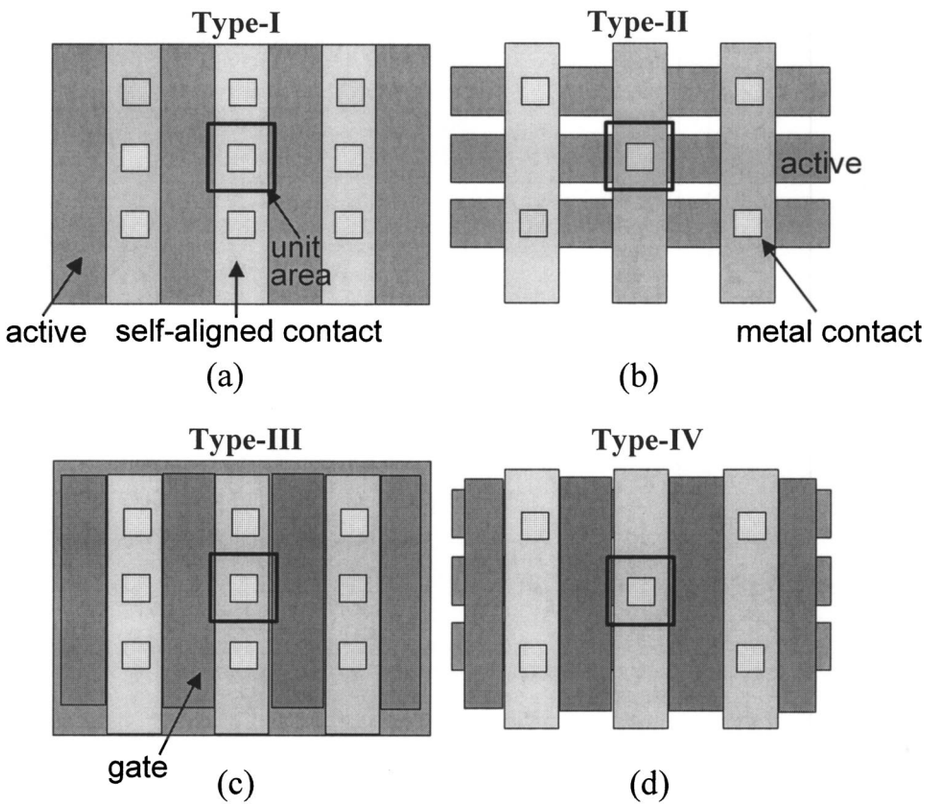

Figure 4. Test device structures used for the cell junction leakage measurements: (a) area-type active pattern without gate, (b) peripheral-type active pattern without gate, (c) area-type active pattern with gate, and (d) peripheral-type active pattern with gate. Because each test pattern contains different junction leakage components, comparison of junction leakage current measured from these patterns enabled the total leakage current to be classified into respective components.

Since active region was fully masked by an Si_3N_4 layer, high doping was localized only along the active boundary including corner transistor and bottom of STI. Owing to this beneficial feature of local field implantation, threshold voltages of both parasitic cell edge transistor and field transistor could be increased, which resulted in improved inverse narrow width effect (INWE) and STI isolation characteristics. In addition, it lessened defect generation caused by high energy implantation damage. After 5 nm thick oxide and Si_3N_4 liner were grown on the trench sidewall, the trench was filled with HDP oxide. The Si_3N_4 liner prevented sidewall oxidation during the following oxidation process steps such as gate oxidation, gate reoxidation, and sidewall reoxidation which are understood to generate considerable amount of stress due to volume expansion caused by thermal oxidation. Thus, the Si_3N_4 liner suppressesed mechanical stress of the silicon sidewall. Then, chemical-mechanical-polishing (CMP) planarization and the removal of nitride stack in a hot H_3PO_4 wet etchant were sequentially performed (Fig. 7b). Next, the localized channel implantation was performed through the open window (Fig. 7c). Because the channel implantation in the storage node was blocked by thick photoresist (PR) as shown in Fig. 8, the implantation damage in the region can be suppressed while maintaining the channel doping concentration equal to that of a conventional cell transistor. After the channel implantation, W-polycide gate, memory cell contact pad using self-aligned contact scheme, W bit-line, Al_2O_3 capacitor, and metallization processes were followed sequentially (Fig. 7d). Figure 9 shows the final cross section of fabricated 512M DRAM with proposed LOCFI cell transistors.

Results and Discussion

In order to predict the effect of localized channel and field implantation on a cell transistor, process and device simulations were performed using TSUPREM4 and DAVINCI simulators,

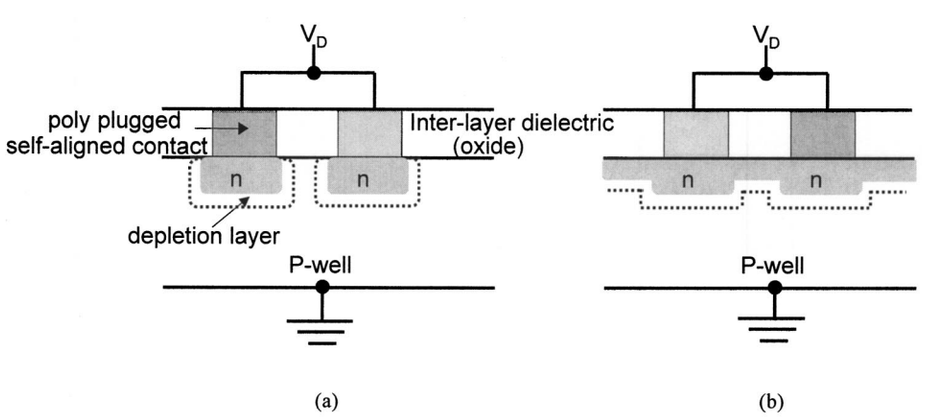

Figure 5. Cross-sectional view of type I (a) without phosphorous implantation and (b) with additional phosphorous implantation before interlayer dielectric deposition. With phosphorous implantation at the dose of 1×10^{13} cm^{-2}, the Si surface became fully inverted to n-type region and only storage node area current contributed to total leakage current.

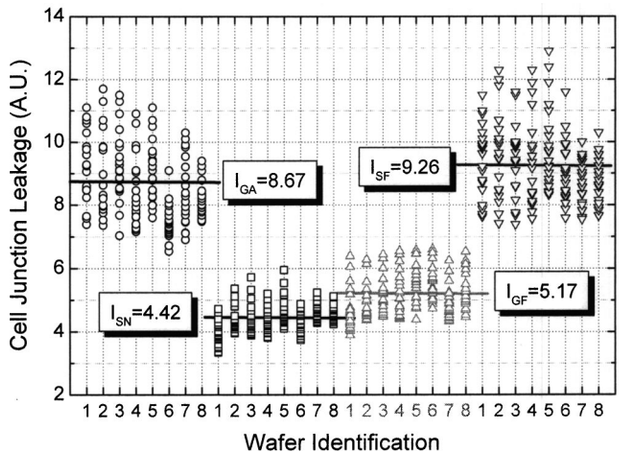

Figure 6. Cell junction leakage reduced to its components. Since the peripheral junction leakage current at STI edge and gate border line has a larger effect on total leakage current than areal storage node junction leakage current, decrease of electric field in depletion region and reduction of process induced damage during STI, gate, and SAC formation are highly recommended to improve data retention time.

respectively.[14,15] While the device equation solver of DAVINCI makes possible 3-dimensional (3-D) analysis, TSUPREM4 can simulate a just 2-D profile. We accordingly simulated the cell transistor along channel length and channel width direction, respectively, using TSUPREM4 at first. Then we constructed the 3-D doping profile with the help of the simulation results and performed 3-D device analysis using DAVINCI. On the basis of secondary ion mass spectroscopy profile data for dopant distribution and electrical measurements, all essential simulation parameters were calibrated.

In the conventional cell transistors adopting overall channel and field implantation on the cell region, the extension of the depletion region from STI edge reduced the gate controllability over channel width and resulted in the INWE as the channel width of cell transistor decreases. INWE was also accelerated by boron segregation and field crowding the STI edge. Therefore, an efficient way suppress INWE is to dope active edge high enough to compensate for the boron segregation because boron impurities at the edge can easily diffuse out during the subsequent thermal process. In the proposed LOCFI scheme, boron implantation for field stop at the pre-exposed active edge formed by Si_3N_4 pull-back would make the STI edge a highly doped region.

Figure 10 shows the roll-off characteristics of threshold voltage as a function of channel width for the conventional and the proposed LOCFI cell transistors using 3-D device simulation. As active width decreased from 0.4 to 0.06 μm, the threshold voltage decreased by about 0.45 V in the conventional cell transistor. On the other hand, only 0.15 V change of threshold voltage was induced in the proposed cell transistor. This means that the channel implantation dose can be reduced in the proposed LOCFI structure meanwhile the same threshold voltage is maintained.[16-19] By reducing cell channel implantation, source/drain junction electric field and lightly-doped-drain (LDD) series resistance can be reduced. The decrease of electric field strength reduced cell junction leakage and thus improved DRAM data retention time. In addition, saturation current of cell transistor can be increased due to the reduced LDD resistance and low doping concentration in channel.

With a view to investigating the effect of LOCFI scheme on DRAM data retention time, we prepared two 512 Mb DRAM samples using 0.12 μm technology; One was adopting cell transistors with conventional field and channel implantation, and the other with localized field and channel implantation. In both samples, the field implantation dose was identical to 4×10^{12} cm^{-2}. The channel of both samples was implanted with boron (B) and boron

Table I. Summary of key process feature for 512 Mb DRAM using 0.12 μm technology.

Cell size	0.2852×0.5952 μm^2
Cell structure	COB
STI	0.25 μm depth with HDP oxide gap fill
Well structure	retrograde triple well
Cell transistor	LOCFI scheme
Gate stack	N^+ poly/WSi_x with Si_3N_4 spacer
Pad contact	SAC scheme with phosphorus doped poly-Si plugging
Cell capacitor	poly-Si storage node/Al_2O_3/TiN plate node
Planarization	5 CMP step
Metalization	2 Al

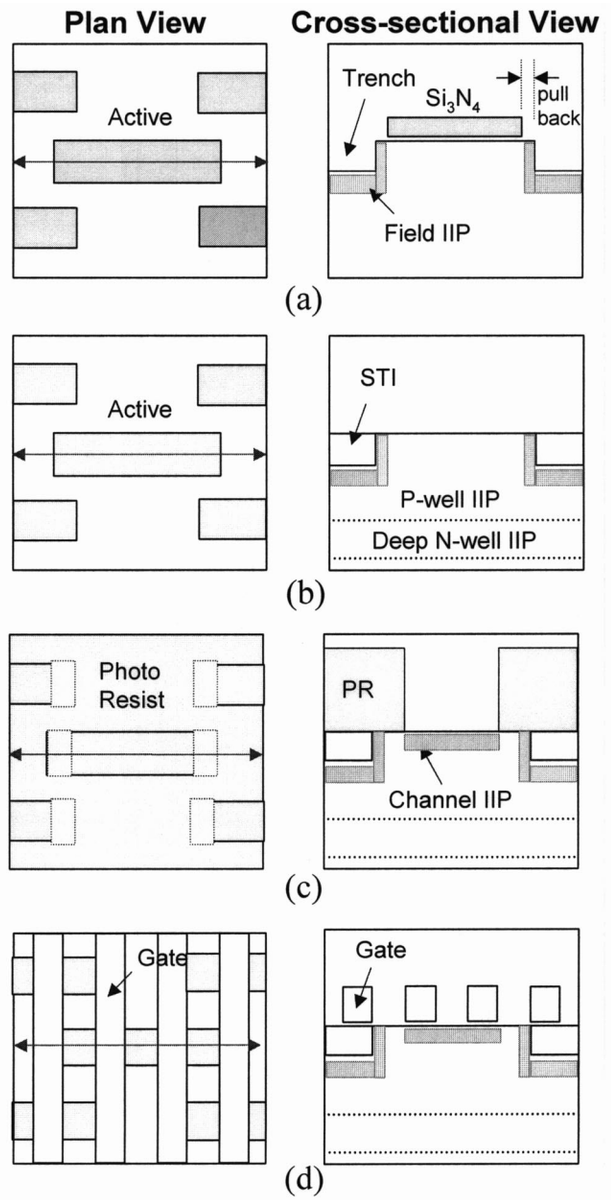

Figure 7. Schematic process sequence for LOCFI cell transistors: (a) localized field implantation, (b) STI formation CMP planarization, (c) localized channel implantation, and (d) gate formation.

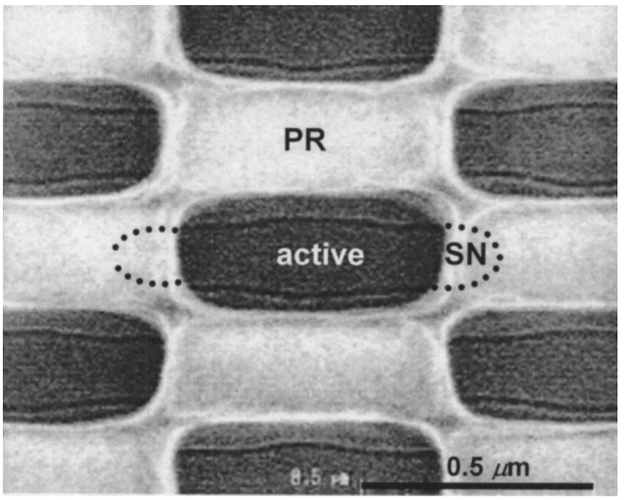

Figure 8. SEM photograph showing PR pattern for localized channel implantation. Since the channel implantation in storage node (SN) is completely blocked by 1.2 μm thick PR, the implantation damage in storage node is suppressed.

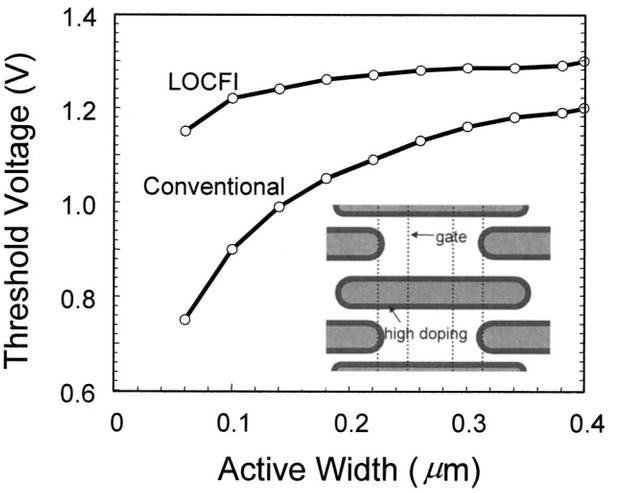

Figure 10. Roll-off characteristics of the threshold voltage as a function of the active width for the conventional and the proposed LOCFI cell transistors using 3-D device simulation.

fluoride (BF_2) that have different projected range to suppress short channel effect and bulk punch-through. The doses of B and BF_2 were identical in both samples as 6×10^{12} and 1×10^{13} cm^{-2}, respectively. Electrical measurement of fabricated devices was performed at the temperature of 85°C and substrate bias of −0.8 V.

Figure 11 shows the effect of local channel and field implantation in view of junction breakdown voltage (V_{BD}) as a function of threshold voltage of cell transistor (V_{TH}). As V_{TH} or substrate doping concentration increased, V_{BD} in the conventional cell transistor decreased because of the undesirable leakage current caused by ion implantation damage and higher electric field. On the other hand, in case of the LOCFI cell transistor, V_{BD} was nearly constant regardless of the change of V_{TH}. For example, at the same V_{TH} of 1.2 V, V_{BD} of LOCFI cell transistor was higher by about 0.4 V than that of conventional one. This is largely due to the decreased electric field and trap density in the depletion region caused by reduced ion implantation damage.[4] Reduced ion implantation damage is achieved by localized channel implantation because the implantation damage in the storage node can be suppressed.

Figure 12 shows the subthreshold slope as a function of cell transistor threshold voltage. If the threshold voltage of parasitic corner transistor becomes equal to that of center transistor, subthreshold slope has the minimum value because a double hump characteristic is eliminated. This implies that the LOCFI cell transistor can have smaller off-state leakage current without aggravating subthreshold characteristics. Furthermore, since boron impurities are locally implanted into bottom of STI region, a doping profile at cell node junction would not be abrupt compared to that of conventional scheme. Reducing maximum electric field at a cell node junction clearly illustrates the reduction of thermionic junction leakage current in space charge region and hence DRAM refresh time would become longer. Figure 13 shows the distribution of reverse junction breakdown voltage V_{BD} as a function of off state leakage current of cell transistor I_{OFF}. As I_{OFF} is increased, V_{BD} is inclined to increase

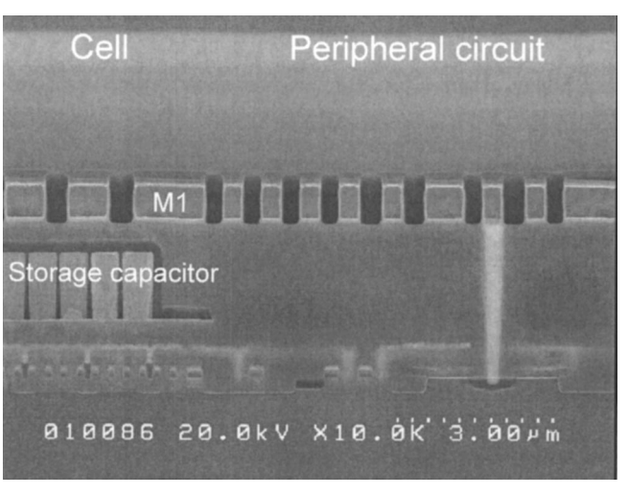

Figure 9. Cross-sectional SEM image of a completed 512 Mb DRAM using 0.12 μm technology.

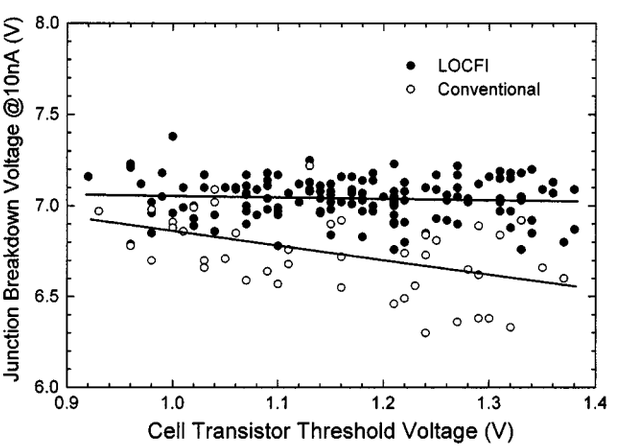

Figure 11. Correlation of junction breakdown voltage at storage node and threshold voltage of cell transistor. As the threshold voltage increased, the junction breakdown voltage decreased in the conventional cell transistor because of increased substrate doping concentration. On the other hand, the junction breakdown voltage in the LOCFI cell transistor was nearly constant irrespective of the threshold voltage of cell transistors owing to the localized channel and field implantation.

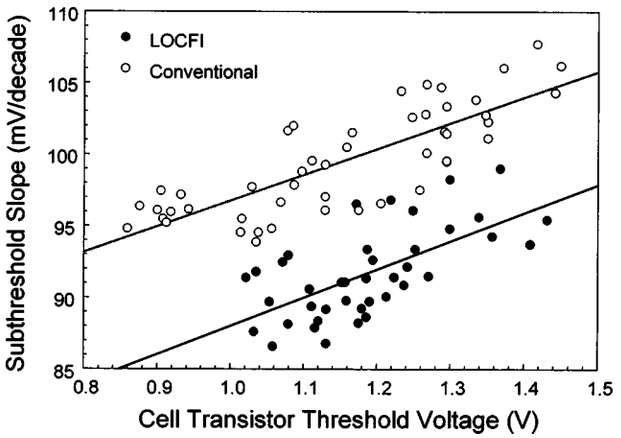

Figure 12. Correlation of subthreshold slope and threshold voltage of cell transistor. The proposed LOCFI cell transistor has smaller subthreshold slope by about 10 mV/decade than the conventional one at the same threshold voltage, which implies that the LOCFI cell transistor can have smaller channel implantation dose than conventional one while maintaining the same subthreshold leakage current. This eventually improves data retention characteristics.

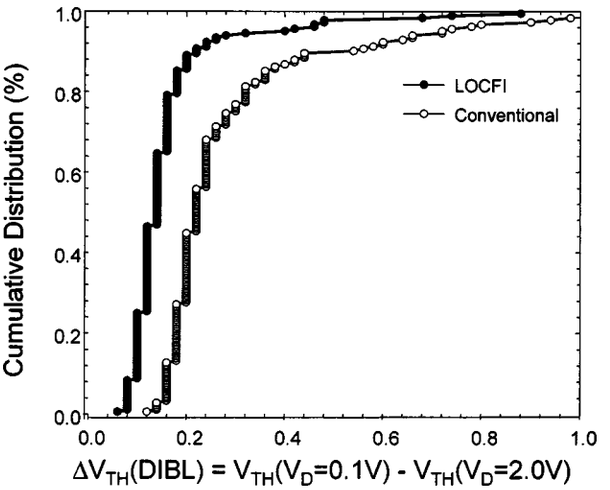

Figure 14. Cumulative distribution of DIBL effect in the LOCFI and the conventional cell transistors.

for both cell transistors due to the reduced substrate doping concentration. However, in case of LOCFI cell transistor, V_{BD} is higher by about 0.6 V than that of conventional one at the same I_{OFF}. Figure 14 compares the drain-induced-barrier-lowering (DIBL) effect of conventional and LOCFI cell transistors. The DIBL of the LOCFI cell transistor is reduced by about 40% compared with that of the conventional one. The reduction in subthreshold slope and DIBL provides good chance to improve dynamic refresh characteristics.

Data retention curves of 512 Mb DRAMs adopting the conventional and the LOCFI cell transistors, respectively, are presented in Fig. 15. The data retention characteristics in the case of LOCFI cell transistor are superior to those in the case of the conventional one. For example, when the data retention time is set to 128 ms, the cumulative fail-bit-probability in the case of LOCFI cell transistor is reduced by about 80% compared with the value in the case of the conventional one.

Although the LOCFI cell transistor has many advantages, the opening size of PR for the localized channel implantation should be optimized from the viewpoint of the process tolerance such as misalignment and variation of critical dimension. Figure 16 is the simulation results showing the change of V_{TH} and DIBL as a function of misalignment (α) between each edge of the PR and the localized channel implantation region beneath the gate, when the drain voltage (V_{DS}) is 0.1 and 4.0 V, respectively. If α is decreased from 0 to -30 nm, the V_{TH} is reduced by about 100 mV and the DIBL is increased to about 35 mV. This represents the case in which the localized channel region is partly blocked by PR. On the hand, if α is larger than 40 nm, V_{TH} is increased by about 70 mV, and in that case, localized channel implantation seems to be less effectual.

Conclusions

In the present work, a cell transistor using localized channel and field implantation was proposed to improve the refresh characteristics for low power and reliable operation of giga-bit density DRAMs. Utilizing the specially designed test patterns, we quantitatively analyzed the cell junction leakage current. Since it was found that the main components of the junction leakage current were originated from gate/active border region and SAC/field border region, the proposed cell structure was expected to have longer data reten-

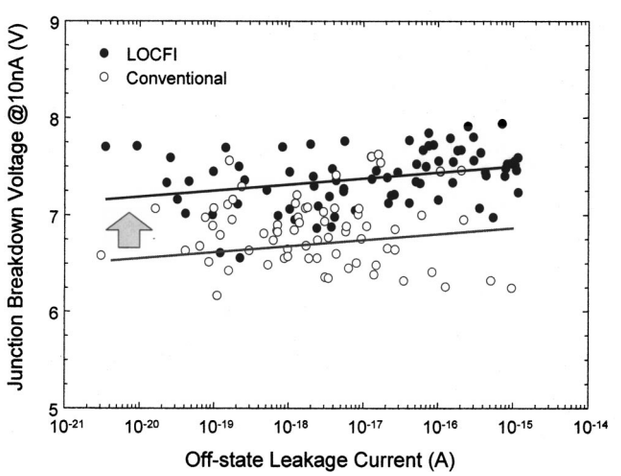

Figure 13. Measured breakdown voltage V_{BD} as a function of the off-state leakage current I_{OFF}. The LOCFI cell transistor has higher V_{BD} by about 0.6 V than conventional one at the same I_{OFF}.

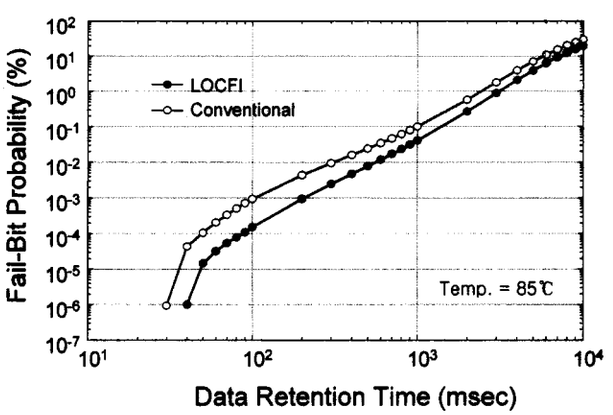

Figure 15. Data retention characteristics of 512 Mb DRAM with 0.12 μm technology adopting the conventional and the LOCFI cell transistors, respectively. The measurement temperature, operation voltage (V_{CC}), and substrate bias (V_{BB}), are 85°C, 3.5 V, and -0.8 V, respectively.

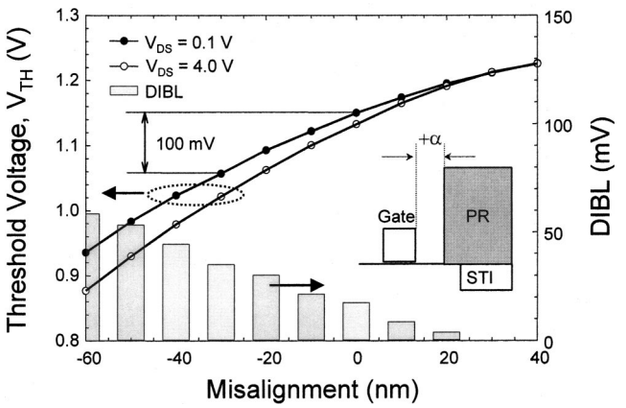

Figure 16. Simulation results showing the trend of the cell transistor threshold voltage and DIBL as a function of misalignment. In order to make the most of advantages of localized channel implantation, misalignment and variation of critical dimension for open window should be tightly controlled. In our fabrication process, the misalignment tolerance was confined to ±30 nm, so that the localized channel implantation could be effective.

tion time. In LOCFI cell transistor, the ion implantation damage, which can induce the locally enhanced electric field and traps in the depletion region, was mostly suppressed at the storage node. As a result, the data retention time and the device yield were greatly increased. Cell transistor performances such as subthreshold slope, INWE, and junction leakage currents, were also improved. We expect that the proposed methodology can provide a promising candidate for realizing the future giga-bit density DRAMs and beyond.

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