Maskless Fron-Side Bulk Micromachining Compatible to Standard GaAs IC Technology

by

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ABSTRACT

The increasing interest in microelectromechanical systems (MEMS) nowadays is due to the same reasons that guaranteed the digital integrated circuit (IC) success in the last decade, such as miniaturization, design flexibility, volume manufacturability, reliability and reproducibility. Besides the low cost and mature silicon technologies, alternative materials have also been targeted to applications where silicon is outperformed. Particularly, gallium arsenide (GaAs) seems to be very promising since piezoelectric, piezoresistive and optical effects can be exploited, as well as high-temperature and high-speed electronic circuit operation are possible.

In this thesis, a front-side bulk micromachining approach compatible with standard GaAs microelectronics technologies is investigated for collective fabrication of low cost, high volume microsystem applications. Free-standing structures are easily released through a maskless post-process wet chemical etching, with no modification in the IC fabrication, no damage in pad metallization and passivation layers, and no influence on the unconcerned electronic parts.

Initially, several etching solutions have been studied and characterized for micromachining purposes in terms of preferential or anisotropic etching, selectivity of GaAs with respect to AlGaAs layers, possible damage on substrate surface layers, and the different etch rates for specific crystallographic directions. Next, potential micromachined devices compatible with such approach are evaluated for sensors, actuators, and microwave applications. Special attention is given to GaAs thermocouple-based devices, e.g., microwave power sensors, and suspended planar spiral inductors and transformers, which present numerous advantages with respect to standard structures because of a significant reduction in parasitic capacitive effects and associated losses. Finally, a set of CAD tools related to layout level design, such as cross-section and three-dimensional layout viewers, layout generators, bulk etching simulator for vertical profile, and an open area converter have been developed within the Mentor Graphics environment.

Keywords : microsystem, gallium arsenide, micromachining, thermocouple, planar spiral inductor, CAD tools.

"A science is driven by people's excitement about learning..."

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ABSTRACT

The increasing interest in microelectromechanical systems (MEMS) nowadays is due to the same reasons that guaranteed the digital integrated circuit (IC) success in the last decade, such as miniaturization, design flexibility, volume manufacturability, reliability and reproducibility. Besides the low cost and mature silicon technologies, alternative materials have also been targeted to applications where silicon is outperformed. Particularly, gallium arsenide (GaAs) seems to be very promising since piezoelectric, piezoresistive and optical effects can be exploited, as well as high-temperature and high-speed electronic circuit operation are possible.

In this thesis, a front-side bulk micromachining approach compatible with standard GaAs microelectronics technologies is investigated for collective fabrication of low cost, high volume microsystem applications. Free-standing structures are easily released through a maskless post-process wet chemical etching, with no modification in the IC fabrication, no damage in pad metallization and passivation layers, and no influence on the unconcerned electronic parts.

Initially, several etching solutions have been studied and characterized for micromachining purposes in terms of preferential or anisotropic etching, selectivity of GaAs with respect to AlGaAs layers, possible damage on substrate surface layers, and the different etch rates for specific crystallographic directions. Next, potential micromachined devices compatible with such approach are evaluated for sensors, actuators, and microwave applications. Special attention is given to GaAs thermocouple-based devices, e.g., microwave power sensors, and suspended planar spiral inductors and transformers, which present numerous advantages with respect to standard structures because of a significant reduction in parasitic capacitive effects and associated losses. Finally, a set of CAD tools related to layout level design, such as cross-section and three-dimensional layout viewers, layout generators, bulk etching simulator for vertical profile, and an open area converter have been developed within the Mentor Graphics environment.

Keywords : microsystem, gallium arsenide, micromachining, thermocouple, planar inductor, CAD tools.

Chapter 1
INTRODUCTION

"Do small things have a grand future?... Ten years ago, a colleague at Bell Laboratories looked me in the eye, and said 'Your microthings will never amount to anything. Large objects will always do a better job at a lower cost'. This was very strongly the feeling at this time... Things insignificant in size do have a grand purpose..." W. Trimmer [1]

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1.1 MEMS TECHNOLOGY

The increasing interest in microelectromechanical systems (MEMS) nowadays is due to the same reasons that guaranteed the digital IC success in the last years, that is, reliability, reproducibility, design flexibility, miniaturization, performance, fabrication cost at large volume, and so on. Moreover, monolithic approaches that integrate electronic and mechanical blocks on the same chip are preferable rather than hybrid ones mainly in order to reduce interfacing losses.

The successful fabrication and operation of microactuators and micromechanical parts by IC-based micromachining technology enabled the realization of MEMS. Although the small size of mechanical components of a system is a very distinctive feature of this emerging technology, it has other, maybe even more attractive, features such as multiplicity and integration of microelectronics [2].

According to Ernst & Young studies [3], the world microsystems market, that represented U$ 12 billion and 1.3 billion of units in 1996, is expected to grow to U$ 34 billion and 5.4 billion of units until 2002. The pressure sensor and accelerometer sensor (1 axis) markets present today a growth of 18% and 15% per year, respectively. Moreover, the market of new micromachined devices, such as micro-optics, projection valves, anti-collision systems, airbag inflator and switches, linear and ultra-sonic micromotors, injection nozzles, and others, will grow from 60 million of units (U$ 310 billion), in 1996, to one billion of units (U$ 1.6 billion), in 2002. The main areas of interest are the automotive industry, telecommunications, medical and biomedical applications, although instrumentation, process control, aeronautic, and many other sectors may also profit of this revolutionary technology.

Silicon is the most commonly used material for micromachining because the process is well established, it has good mechanical properties, and integration of electronic and sensor (actuator) is possible. However, alternative and promising materials have also been investigated for specific purposes where silicon is outperformed.

1.2 GALLIUM ARSENIDE SEMICONDUCTOR

Gallium arsenide (GaAs) semiconductor has recently risen from obscurity to technological wonder. Since the first MESFET (MEtal Semiconductor Field Effect Transistor) was proposed in 1966 and the first HEMT (High Electron Mobility Transistor) was demonstrated in 1978 by Bell Laboratories, the industry has evolved and changed over the last 30 years and has finally escaped

from its designation as the ‘technology of the future’ [4].

The emergence of the digital cellular phone market because of the GSM standard marked the advent of widespread use of GaAs semiconductors. Since 1994, the GaAs industry has grown at least 25% each year, reaching over U$ 1 billion in 1996. By far the most rapid growth area in GaAs has been the analog sector, which includes discrete, IC and hybrid modules.

In terms of the GaAs substrate, the market of semi-insulating GaAs wafers for wireless applications has grown from 3 million square inches (MSI) in 1994 to over 5 MSI in 1996, a compound annual growth rate (CAGR) of 29%. The GaAs wafer industry is expected to produce 8 MSI by the year 2000, a CAGR of 32% since 1995 [5]. The biggest issue concerning the worldwide production of GaAs substrates is the availability of raw materials, namely gallium metal and pure arsenic. The monopoly that Rhone-Poulenc has for gallium metal production and the fact that it is trying to reduce availability and drive prices up by mothballing its Australian operation is one of the main reasons for the high cost of GaAs technology.

Analog GaAs devices will continue to play a significant role in digital communications systems because of the peak power, supply voltage and signal distortion requirements. On the other hand, it is quite obvious that digital GaAs circuits have also made a comeback from the depths of obscurity, in the form of one company that has emerged as the market leader : Vitesse Semiconductor. The three major areas of opportunity for digital GaAs are SONET, Gigabit Ethernet and Fibre Channel.

In the case of competing technologies, some new materials and IC processes, such as silicon-germanium (SiGe), graded-channel CMOS (GCMOS) and ‘double polysilicon’ processes, will start to carve away at the GaAs market, especially for low-tier applications such as cordless handsets in the 1 to 2 GHz frequency spectrum [6]-[9]. However, each successive wireless communication application increases in frequency, which creates more opportunity for GaAs and less for silicon. Moreover, supply voltages will continue to decrease to 3 volts and eventually down to 1.5 volts, making also GaAs transistors even more interesting than silicon ones.

1.3 MOTIVATION AND OBJECTIVES

As a sensor material, GaAs possesses many interesting properties. These include well known properties such as direct band gap transition and high mobility of electrons. GaAs also has piezoelectric properties comparable with those of quartz, and it exhibits a strong photoelastic effect leading to birefringing and consequently, for example, an optomechanical polarization effect.

Moreover, various physical effects give higher piezoresistive values than those of silicon. Furthermore, the maximum value of the thermal resistance in the closely related AlGaAs system is much higher than that of silicon. Finally, GaAs is considered to be a good material for high-temperature electronics due to its large band gap.

Another important feature of the III-V technologies is the possibility of forming compatible ternary and quaternary compounds by alloying. Using GaAs as the substrate material, the formation of $Al_xGa_{1-x}As$ is especially attractive, since their lattice constants are nearly equal, and aluminum and gallium atoms are easily substituted in the lattice without causing too much strain in the film. Today the epitaxy techniques have matured and both high-quality MOCVD and MBE epitaxy are commercially available.

In this work, a GaAs micromachining approach compatible with microelectronics processes is investigated. Commercial technologies have been used to build suspended structures through a maskless front-side bulk micromachining technique. A post-process wet etching is added to the conventional IC process, without modifying the standard fabrication procedure and with no influence on the unconcerned electronic parts. It seems to be the fastest and cheapest way to develop MEMS, since electronic and mechanical devices are allowed on the same die, and they can be fabricated through multi-project wafer services beside purely electronic ICs [10].

In terms of GaAs MEMS, little has been done in the world even if its attractive and promising features seem to be obvious. This work represents a pioneering research with respect to GaAs micromachining based on commercial IC processes. The main goal is to provide a comprehensive description of GaAs MEMS design, including the characterization of suitable etching solutions, the study of related potential micromachined devices and applications, the development of micromachining design rules and CAD tools for layout construction.

1.4 THESIS STRUCTURE

At the beginning, Chapter 2 outlines some used definitions. A brief review of GaAs electronic and mechanical properties as well as the GaAs micromachining techniques are given, before introducing the approach adopted herein. Chapter 3 describes the characterization of the post-process etching. Selective and preferential solutions have been taken into account in order to obtain the different structures proposed in this work.

In Chapter 4, thermal based micromachined devices are investigated in order to demonstrate the advantages of the intrinsic GaAs properties and characteristics with respect to related

technologies. Among them, thermopile structures, to build, e.g., microwave power sensors, seem to be very promising due to the high Seebeck coefficient and thermal resistivity of GaAs material. Next, in Chapter 5, suspended microwave passive devices are evaluated by theoretical analysis and experimental results. Microstrip transmission lines, planar spiral inductors, transformers, interdigited capacitors, Lange-couplers and many others show a significant improvement in performance by using this technique.

Chapter 6 presents some CAD tools related to the layout level design and developed on the Mentor Graphics environment, extending it to MEMS design. Such set of tools includes layout generators, cross section and three-dimensional layout viewers, converters from open area to real layers and *vice-versa*, and two-dimensional etching simulators for surface and vertical profiles. Finally, in Chapter 7, the conclusions and future perspectives are presented.

1.5 SUMMARY

In summary, the increasing interest in MEMS is leading researchers towards the study of alternative materials which can show an improved performance with respect to silicon for some application. GaAs is nowadays a mature technology and appears to be very useful for MEMS design due to its particular micromachining characteristics and physical features, such as piezoelectricity and large band gap. This thesis includes the characterization of GaAs etching, the investigation of micromachined devices and the development of CAD tools in order to provide the basis for future developments in GaAs MEMS design using industrial IC production lines.

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Chapter 2
GaAs MICROSYSTEMS TECHNOLOGY

The nomenclature used in this work is defined. Moreover, a brief review of the GaAs physical properties and the response mechanisms associated with micromechanical structures is also outlined. Special attention is given to particular GaAs features and comparison to silicon in order to emphasize the real interest in such alternative material. Furthermore, the state-of-the-art of GaAs micromachining techniques is also described, before introducing the microelectronics compatible micromachining approach investigated herein, which seems to be the most efficient way to MEMS design in terms of time-to-market, fabrication cost, volume manufacturability and electronic compatibility.

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2.1 DEFINITIONS

What one means by ‘emerging’ technologies depends on the viewpoint and MEMS are not really all that new. MEMS pressure sensors appeared before 1960. In Asia, the term used is ‘micromachines’, while in Europe, it tends to be ‘microsystems’. In the USA, what began as an acronym for ‘MicroElectroMechanical Systems’ (MEMS) remains the dominant term. It is not even frequently capitalized anymore, nor is it restricted to microelectromechanical applications. In fact, the term MEMS also denotes the process by which the actual device is fabricated. ‘Microsystems Technology’ (MST) is the overall discipline, and is now considered a subset of conventional integrated circuit (IC) manufacturing since most often current MEMS processes are compatible with IC fabrication [1].

The increasingly eclectic field of MST can combine any number of device functions including optical, chemical and biological, as well as mechanical and electrical. One should be aware of the fact that the differences in nomenclature can result in market projections. MEMS is the most restrictive term (i.e., the process of creating the devices), ‘microsystems’ is the broadest term, and ‘micromachining’ is considered the most elemental word, but also the most inclusive. Whatever they are called, the devices produced by the discipline are very small, with critical dimensions of less than 1 mm, and they tend to be amazingly complex, including ‘intelligent’ features.

By definition, herein, ‘micromachining’ corresponds to the fabrication method used to build free-standing structures, while ‘microsystems’ and MEMS refer to the integration of micromachining and microelectronics. It could be represented by a hybrid system, that is commonly composed by different dies containing separately micromachined and electronic parts, or by a monolithic version, where all the system is implemented on the same die. Nowadays, monolithic solutions have been widely investigated in order to reduce even more the final system dimensions and the associated interfacing problems, resulting, consequently, in a better compromise between design and fabrication costs, performance and reliability.

As in IC processes, silicon also represents the most typical material for monolithic MEMS design [2]. However, the wide bandgaps, piezoelectric effects, optoelectronic compatibility and other features of some alternative materials, like GaAs, quartz, InP, SiC and diamond, will also play a critical role in the future of MEMS as the processes and device designs become more popular, since the intended operational environments for MEMS devices are considerably more harsh and demanding than silicon can properly service. Particularly, in this work, GaAs is presented

as a microelectromechanical technology and investigated in terms of etching characteristics and potential applications.

2.2 GaAs MATERIAL PROPERTIES

Before describing the micromachining techniques and in particular the approach adopted at TIMA laboratory, the GaAs properties are briefly reviewed. The use of a more expensive material, as GaAs with respect to silicon, is only justified for applications which profit f its advantages. Thus, special attention is given to such features and characteristics, and a comparison to silicon properties is also outlined. Additional information about the basic physical properties of GaAs and AlGaAs ternary can be found in the reviews published by J.S. Blakemore [3] and S. Adachi [4].

2.2.1 Structural and Electrical Characteristics

GaAs and many other III-V compounds present the zinc blende (or sphalerite) crystallographic structure which is made up of two face-centered cubic (FCC) sublattices displaced by a vector (1/4, 1/4, 1/4), as illustrated in Fig. 2.1. One FCC lattice is made up entirely of Ga atoms, and the other entirely of As atoms. Unlike the crystal structure of elemental semiconductors, the compounds III-V semiconductors exhibit a certain deviation from inversion symmetry. In the case of GaAs, this can be seen as a tendency of the electron clouds to shift towards the As atoms, resulting in a dipole moment along the [111] axis. Consequently, a non-vanishing piezoelectric coefficient, a fracture toughening of {111} planes yielding {110} as the primary cleavage planes, and the opposite pairs of “Ga-rich” and “As-rich” planes formed by the eight {111} planes are observed.

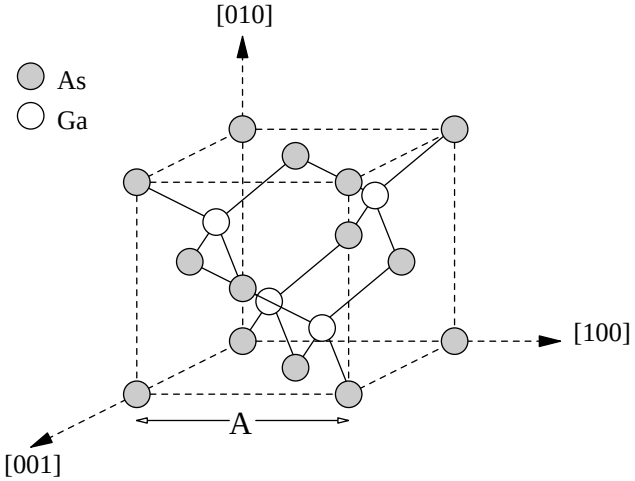


Fig. 2.1 - Conventional unit cube for GaAs (zinc blende crystal structure).

Because of higher electron mobility and higher peak electron velocity than silicon, and due

to the semi-insulating substrate characteristics, GaAs has for a long time been considered for high-frequency electronics, such as monolithic microwave integrated circuits (MMIC). Moreover, its large and direct bandgap is useful to high-temperature operation and opto-electronic circuits, respectively. However, although commercial GaAs IC processes are already available for digital and microwave applications, such more expensive material still presents higher defect densities than silicon.

Table 2.1 summarizes some structural and electrical characteristics. Note that, the crystal density of GaAs is twice higher than the density of silicon. It is of great importance for mechanical behavior of devices in, for example,. acceleration and resonant applications.

TABLE 2.1 - Structural and electrical characteristics.

	GaAs	silicon
Crystal structure (space group)	zinc blende ($\bar{4}$ 3m)	diamond (m3m)
Lattice constant a (Å)	5.6533	5.4311
Crystal density ρ (g/cm^3)	5.3165	2.3290
Bandgap energy Eg (eV)	1.424 (direct)	1.12 (indirect)
Low-field electron drift mobility (cm^2/V.s)	5000 *	800 *
Peak electron velocity (cm/s)	1.7 x 10^7 **	6.5 x 10^6 ***
Dielectric constant	12.6	11.8
Substrate resistivity (Ω.cm)	10^6 to 10^8	low

* $N_D = 10^{17}/cm^{-3}$, ** E = 3.5 kV/cm and $N_D = 10^{17}/cm^{-3}$, *** E >> 10 kV/cm.

2.2.2 Mechanical Endurance and Elastic Properties

Though the defect densities are still higher for GaAs than for silicon, from a mechanical viewpoint they have reached acceptable levels for many applications. Since GaAs is a single crystalline material, it exhibits an elastic anisotropy, described by the stiffness matrix c_{ij} (see Table 2.2). Many of the basic mechanic equations include the elastic modulus (the Young's modulus) and the Poisson ratio, which are both orientation dependent. The elastic modulus is about 30% lower for GaAs than for silicon, which for example means a rod of otherwise the same dimensions needs an 11% increase in thickness for the same bending stiffness. The resonant frequency is directly proportional to the elastic modulus.

Moreover, being GaAs a brittle material at normal operating temperature, it will deform elastically until brittle fracture. The fracture strength σ_f is proportional to the material constant critical fracture toughness K_{Ic}, and limited by the largest stress concentration, i.e., often the largest defect. Consequently, the risk of a large defect is reduced and the chance to build a strong structure is risen by reducing the mechanical active volumes. The shape of a defect is of minor importance if

the size of the defect is as small as comparable to the fracture process region.

The average fracture strengths for the GaAs and silicon micromechanical cantilever beam structures are 2.7 and 7 GPa, respectively, showing that silicon is a stronger material. However, since construction steels normally fracture bellow 1 GPa and deform at even lower stresses, properly micromechanical structures of GaAs may still be considered as high-strength structures.

Furthermore, a brittle material may deform plastically at the surface due to surface contacts. At high loads, this will lead to fracture and shattering of the material. The hardness of GaAs is 7, and at temperatures above 0.35 *Tm* (melting point) both silicon and GaAs become somewhat ductile. This cause a rapid decrease of the hardness for GaAs above 250°C, and this may be of importance in high-temperature applications.

Finally, in very thin structures the internal stresses in heterostructures, due to thermal mismatch of high-temperature processes, may cause some buckling, but generally this should not be a big problem. If the buckling is too severe in any case, it is possible to create heterostructures with hardly any buckling, combining different layers of AlGaAs and GaAs.

2.2.3 Thermal Characteristics

The Debye temperature θ_D is a useful parameter in solid-state problems because of its inherent relationship to lattice vibration. The parameter θ_D can be used in characterizing the excitation of phonons and to describe various thermal phenomena, such as specific heat and lattice thermal conductivity. The heat capacity or specific heat of the solid is one of the most essential thermal parameters. The heat capacity C_p for GaAs is 0.35 J/(g.K), while for silicon is 0.71 J/(g.K).

On the other hand, the thermal resistivity of III-V compounds has been thoroughly studied, being an important property to consider in the design of power dissipating devices, such as transistors, diodes, and semiconductor lasers. Moreover, it is also necessary in calculating the figure of merit for thermoelectric devices, e.g., Peltier and Seebeck devices. In principle, when a large number of foreign atoms is added to a host crystal by, for example, alloying, the thermal resistivity increases significantly.

The thermal resistivity *W* as a function of composition in the $Al_xGa_{x-1}As$ ternary system is given by the equation :

$$W(x) = 2.27 + 28.83x - 30x^2 \qquad (2.1)$$

Thus, the maximum value is 9.2°C.cm/W at a composition of x=0.48, as shown in Fig. 2.2a. This is more than 14 times higher than that of silicon. Also, the thermal resistivity for GaAs increases rapidly with temperature.

The cubic nature of the sphalerite structures endows GaAs with an isotropic expansivity. The volume expansion coefficient and the linear expansion coefficient vary in sign and magnitude with temperature in a complicate way, not discussed herein [3]. The linear thermal expansion of GaAs is 6.0 ppm/K. From linear interpolation of known data on the thermal expansion for $Al_xGa_{x-1}As$, a linear relationship with the composition is suggested with 4.2 ppm/K for AlAs.

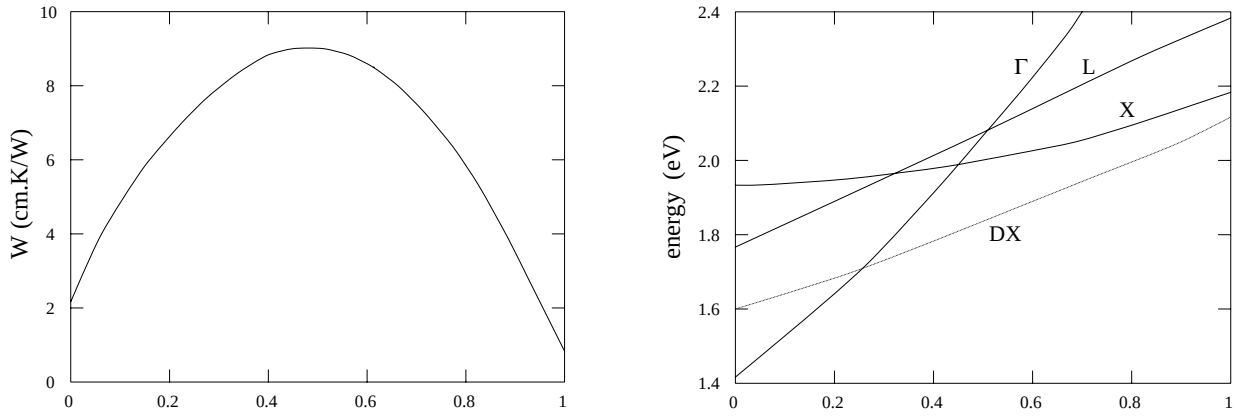
TABLE 2.2 - Thermal, mechanical and optical properties.

	GaAs	silicon
Melting point T_m (°C)	1238	1413
Specific heat Cp (J/g.K)	0.35	0.71
Thermal resistivity W (K.cm/W)	0.64	2.27
Thermal expansion coefficient α_{11} (10^{-6}/K)	6.4	2.6
Debye temperature θ_D (K)	370	463
Seebeck coefficient α (μV/K)	– 300	± 100-1000
Young's modulus for <100> (GPa)	85	190
Fracture toughness K_{Ic} (MPa.$m^{1/2}$)	0.44	0.9
Fracture strength σ_f (GPa)	2.7	7.0
Hardness Hv(100) (GPa)	7	10
Stiffness constants (GPa)		
c_{11}	118.8	165.6
c_{12}	53.8	63.98
c_{44}	58.9	79.51
Elastic compliance constants (10^{-12}/Pa)		
s_{11}	11.7	7.7
s_{12}	– 3.7	– 2.1
s_{44}	16.8	12.6
Piezoelectric coefficient d_{14} (pm/V)	– 2.69	0
Electrooptic coefficient r (pm/V)	1.4	0
Photoelastic constants (GPa)		
p_{11}	– 0.165	– 0.1
p_{12}	– 0.14	0.009
p_{44}	– 0.072	– 0.11

The change of elasticity with temperature changes the output of most sensors and actuators. For example, the change in resonance frequency of a device follows directly from the change of elasticity and dimension. This is one of the main reason why quartz is used as a reference resonator

with extremely low temperature dependence, since in some crystal directions the change of elasticity and dimension cancel each other influence. In silicon and GaAs this is not possible.

Finally, the Seebeck coefficient is responsible for the thermocouple generated voltage, applied as a basic element in several micromachined devices. The Seebeck coefficient of GaAs is S=–300 µV/K, while for n-doped $Al_xGa_{x-1}As$ the maximum value is close to S=–670 µm/K (x=0.45) at the change of direct to indirect bandgap. Additionally, the Seebeck coefficient is higher at reduced doping. Polysilicon and the Bi-Sb-Te alloy, commonly used to implement micromachined thermopiles, are weaker from this point of view.



(a) (b)

Fig. 2.2 - The lattice thermal resistivity (a) and bandgap energies (b)as a function of composition in the $Al_XGa_{X-1}As$ alloy [5].

2.2.4 Response Mechanisms

GaAs offers several means for detecting various external stimuli such as temperature, pressure, acceleration, etc. Compared with silicon, among the interesting features of GaAs as a mechanical material, one can list the possibility of integrating optical active elements monolithically and its piezoelectricity. Some of the most promising response mechanisms for micromechanical sensors are briefly described below [5].

Piezoelectric response — Though not frequently used, the piezoelectric response of GaAs is an attractive feature. It gives the possibility of activating motion using an electrical field and of detecting motion by bound charges generated by mechanical stress. The piezoelectric effect of GaAs is close to that of quartz, and may excite any vibration mode used in quartz if the proper crystal orientation is observed. Other advantages with piezoelectricity are negligible thermal gradients due to the low activation power (of the order of µW), and the possibility of detecting very small mechanical amplitudes.

Piezoresistive response — In GaAs, the physical mechanisms that change the resistance due to an applied stress are different from those of silicon. One response mechanism is the observed mobility change due to the change of the electron effective mass with pressure, in direct bandgap III-V compounds. Another is a pressure induced transfer of electrons from the high-mobility bandgap minimum Γ to low-mobility minima X or L, due to a change of their relative energy (see Fig. 2.2b). A third response mechanism is the pressure induced freezing of electrons to deep level impurity states, DX. The fourth one is somewhat different from the others, using the stress gradient induced piezoelectric bound charges to change the resistivity in a diffused resistor. Piezoresistive gauge factors up to 500 are obtainable in the $Al_xGa_{x-1}As$ system, while typical values in silicon microsensors are 50-90.

Thermoresistive response — The thermoresistive response is coupled to the charge mobility. Therefore, it is very sensitive to how the semiconductor is alloyed, and the resulting change of band structure. If dopants are used, the response is very dependent on the degree of doping. For undoped semi-insulating material, a resistivity change of $\Delta\rho = 1.7x10^8\ e^{-T/12}\ \Omega.cm$ for T in the temperature range 10-70°C, indicates a resistivity drop about 75 times larger than that for Cr compensated over the temperature range 20-200°C ($\Delta\rho = 2x10^8\ e^{-T/17}\ \Omega.cm$). This may be essential for piezoelectric applications.

Piezooptic and direct bandgap responses — The piezooptic response is due to the fact that externally applied asymmetric stress changes the crystal symmetry, and thereby the refractive indices of the crystal. For example, if the otherwise optically isotropic GaAs is exposed to an uniaxial stress, the crystal becomes birefringent. On the other hand, the dependence of the direct bandgap to external stimuli may be directly measured in terms of the wavelength shift of the photoluminescence. To obtain a high photoluminescence activity, the crystal should be highly doped, and preferably be designed with confinement layers of, for example, $Al_xGa_{x-1}As$ to gain a high quantum efficiency.

2.3 GaAs-BASED MICROMACHINING

A great number of micromachining techniques have already been developed for GaAs, such as selective etch stops for hetero- and homostructures of varying electrical properties, sacrificial layer techniques with etch rate selectivities above 10^8, and dry and wet etching for isotropic and anisotropic shaping. These process techniques make GaAs a possible material of choice for micromachined structures, and together with its mechanical and physical features, an interesting

possibility for micromechanical applications. Basically, the micromachining techniques are based on two factors, that is, the selective characteristic of etching solutions associated with heterostructures and damaged layers, due to different etch rates of GaAs and its alloys, and the unique profile presented by III-V compounds (zinc blende crystals), when preferential etching solutions are applied :

Selectivity — Selectivity is defined as the ratio between the structural material (slower etching) and the sacrificial material etch rate (faster etching) for a specific etchant. For a few systems, complete selective etching can be achieved, allowing real etch-stop materials. The most frequently sacrificial wet and dry etch systems used for III-V compound heterostructures are presented in the literature, as the review papers of K. Hjort [6] and S. D. Collins [7]. Note that, not only different materials but different dopant concentrations and damaged regions could also act as stop and sacrificial layers, as described below in some microsystem fabrication techniques.

Anisotropic or preferential etching — The term anisotropic (preferential) etching is usually reserved for the selective wet/dry chemical etching of single crystalline material along particular crystallographic directions. Due to the zinc blende structure of GaAs, the etching of (111) crystal planes proceeds much more slowly than all others. Therefore, specific geometries depend on the orientation of these (111) planes with respect to the surface and pattern orientations. For example, the triangular prism-shaped bridge can be obtained through anisotropic etching by placing appropriately the etch masks [8]. This unique profile, not possible in silicon, is formed because of the crystallographic polarity in some axial directions, and the differences between the etch rates of the A{111} planes and the other low-index planes. On the other hand, GaAs does not present real etch stop planes, as observed in silicon by using, e.g., KOH-based solutions, whose the {111} planes present etch rates up to 400 times lower than the other ones [9].

In terms of micromachining technologies, there are two ways to manufacture microsystems : to develop specific processes to microsystems, hence suited to its special requirements, or to use processes that have been developed for microelectronics. In the second group, some processes can be targeted to microsystems, again to meet specific requirements, while for others, it is possible to add special process steps to accommodate microsystems within the electronic circuitry.

2.3.1 Microsystems Specific Fabrication Methods

The LIGA techniques and quartz micromachining are classical examples of microsystems specific fabrication methods. The LIGA (in German, *Lithographie, Galvanoformung, Adformung*) process utilizes deep X-ray lithography, electroplating and molding to make thick microstructures

with high aspect ratio [10]. In contrast to orientation dependent etching of monocrystalline silicon, there are no restrictions in the cross-sectional shape of the microstructures. Micromachining techniques for quartz, in turn, are derived from conventional methods used in optical engineering. These techniques, diamond saw cutting, lapping and polishing techniques, offer a high degree of accuracy and finishing quality, but they are not adapted for the design of the three-dimensioned micromechanical devices, built using techniques suitable for high-quality mass production [11].

In GaAs micromachining, some new technologies have also been developed, such as the process named SCREAM II (Single Crystal Reactive Etching And Metallization II), which includes chemically assisted ion beam etching (CAIBE) and reactive ion etching (RIE) for vertical and undercut dry etches, respectively [12]. Suspended and movable structures are produced with up to 25:1 aspect ratio of vertical depth (10 µm) to lateral width (400 nm). Si_3N_4 is used as the etch mask, structural stiffener and electrical insulator, while integrated actuators with predominantly vertical sidewall (PVS) aluminum electrodes are used to move the structure (see Fig. 2.3). However, the integration of electronic devices, required for monolithic integration of MEMS, is somewhat compromised.

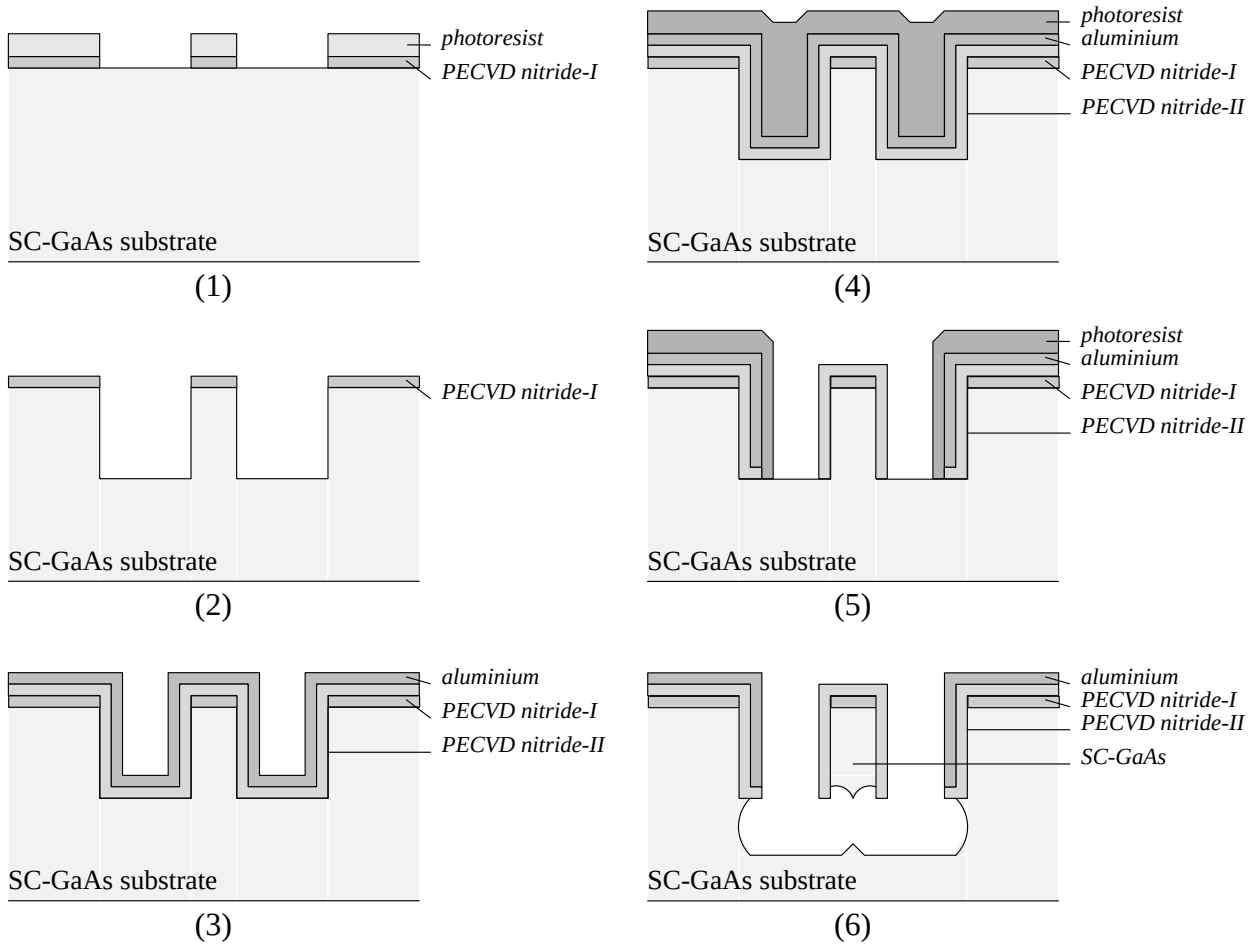


Fig. 2.3 - Fabrication steps of SCREAM-II process [12].

2.3.2 Microelectronics Compatible Fabrication Methods

The fabrication of microelectronics compatible micromechanical structures, both silicon- and GaAs-based micromachining, consists of adding selective and/or anisotropic etching steps (maskless or with supplementary masking) to the IC fabrication flow in order to remove sacrificial layers from the surface or some portions of the substrate material, keeping others suspended. Therefore, two main methods can be listed : bulk micromachining, whose structures are etched in the substrate, and surface micromachining, whose micromechanical layers are formed from layers deposited onto the surface. VLSI circuit integration, low cost and rapid delivery are some of the numerous advantages of these microelectronics compatible micromachining approaches.

2.3.2.1 Bulk micromachining

Bulk micromachining relies on the substrate etching wells, leaving suspended structures.

Using this technique, devices like micro-hotplates, infrared sources, thermal flat-panel displays, thermopiles, channels for fibres and force sensors can be developed. In bulk micromachining two approaches have been considered, that is, to realize the etching from the front side and from the back side of the wafer.

a) Front-side approach

In this case, the substrate is attacked from the surface of the die or wafer, either using intermetallic and passivation layers as the mask for post-process etching, or with additional masking adapted to the IC fabrication to create damaged or implanted layers for selective etching.

In the first example, the implantation of nitrogen into GaAs followed by subsequent annealing produces buried $GaAs_{1-x}N_y$ ($y<x<1$) layers, which are used as sacrificial layers for selective etching of GaAs [13][14]. As illustrated in Fig. 2.4a, a SiO_2 mask defines the implanted region and the buried N-containing is formed at a depth determined by the energy of the implantation, which recrystallizes to a $GaAs_{1-x}N_y$ layer after annealing. Next, another SiO_2 layer is deposed to determine the geometry of the structure, and then a non-selective etching is performed down to the implanted layer. Finally, the sacrificial layer of $GaAs_{1-x}N_y$ is etched selectively with 1N NaOH solution, leaving a free-standing structure of GaAs.

The second example also uses ion implantation to create damaged substrate regions. But, unlike the firstly described technique, no annealing is performed and a selective etching is possible since the selectivity increases with the degree of damage. This technique has been applied by Miao et al. [13] to suspend Si_3N_4 structures by using $KI:I_2:H_2O$ (see Fig. 2.4b).

In the third example, Uenishi et al. [15] fabricates AlGaAs microbeams by removing GaAs substrate material through a selective etching, as shown in Fig. 2.5. In the last example, front-side bulk micromachining is realized through preferential or anisotropic etching. Free-standing triangular prism-shaped bridges have been built for GaAs thermocouple applications by using H_2SO_4-based etchant [16]. Such kind of structure is discussed in detail in the next chapter, since it represents one of the target structures investigated in this thesis.

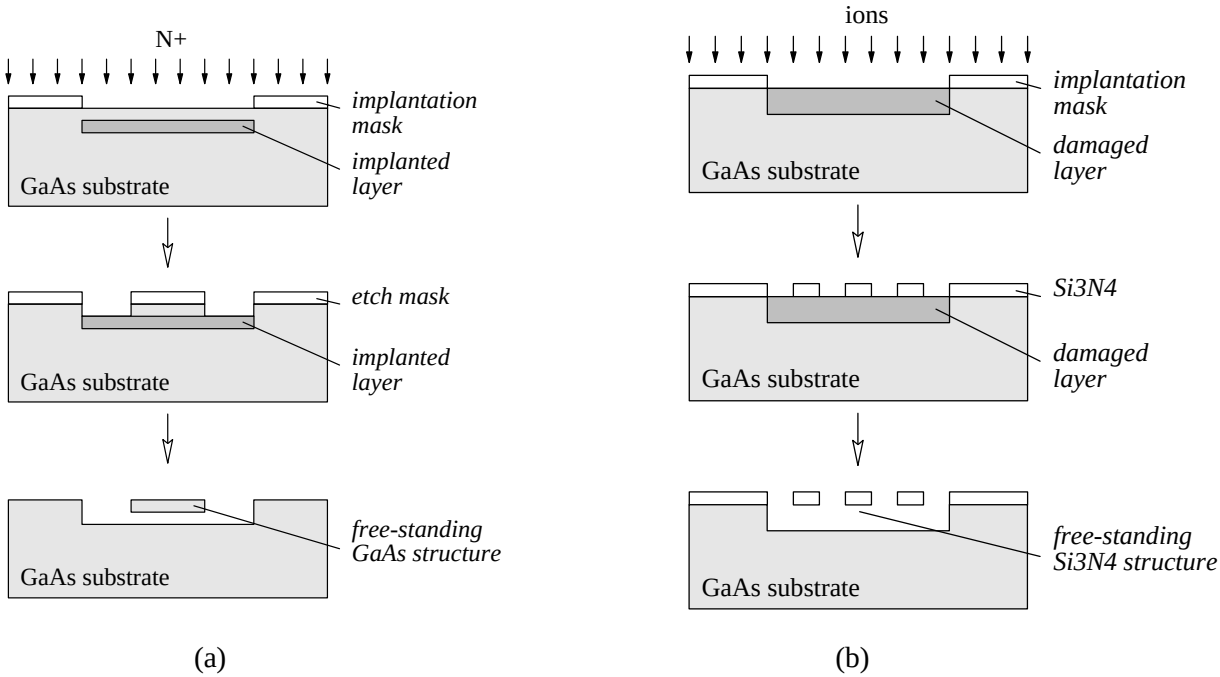


Fig. 2.4 - GaAs bulk micromachining using implanted (a) and damaged (b) sacrificial layers [13].

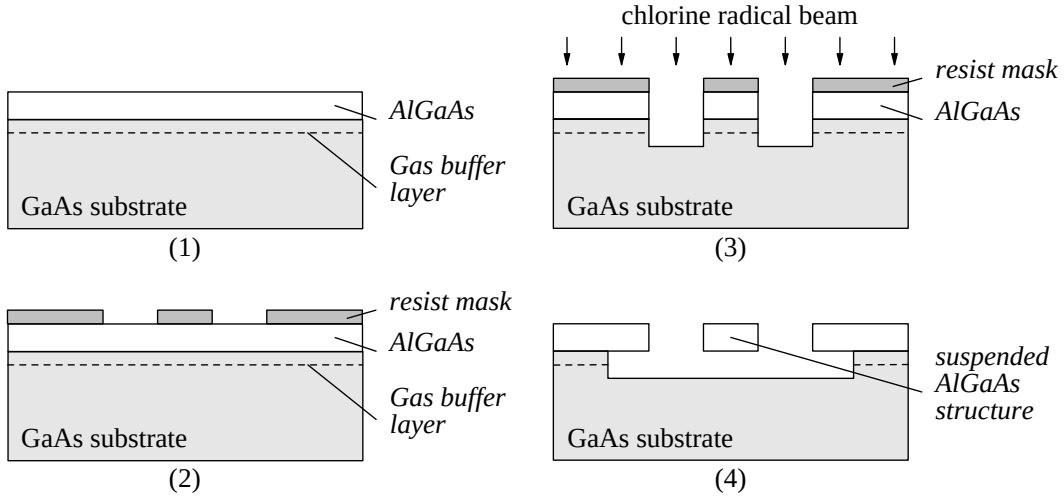


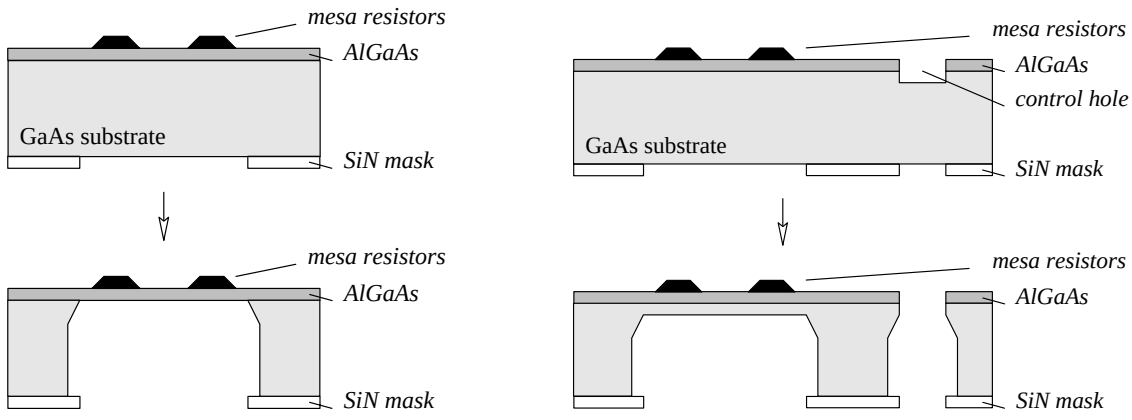
Fig. 2.5 - Fabrication of AlGaAs microstructure using GaAs as sacrificial layer [15].

b) Back-side approach

The back-side bulk micromachining commonly involves stopping on an epitaxial layer. Additional masking on the back side and special alignment techniques are required. Moreover, structures as small as such realized by front-side approaches are not possible. Because of the high selectivity of the GaAs/AlGaAs system, it is possible to etch several hundred micrometers of GaAs stopping at an exact depth, defined by a stop layer of AlGaAs. This technique has been widely used to build GaAs membranes for pressure sensors [17][18]. A simplified description of such a process

is depicted in Fig. 2.6a. The back side is covered by an etch mask. Then, a fast unselective etching is performed, followed by a slower selective etching, stopping at the AlGaAs layer.

Another method of constructing membranes from the back side consists in using control holes that have been etched initially from the front side, being as deep as the required membrane thickness. The back-side etching of the membrane is stopped when the front-side holes become visible, as illustrated in Fig. 2.6b. As a result, the membrane can be thicker than that one obtained by selective etch stop technique, but the homogeneity of this etching is not as good as in the first case [18].



(a) (b)

Fig. 2.6 - GaAs back-side bulk micromachining: (a) using AlGaAs as stop layer and (b) using control hole technique [18].

c) Combined front- and back-side approach

A combined approach using front- and back-side micromachining has been presented by Miao et al. [14] to build a capacitive pressure sensor. Ion implantation is applied to create the suspended Si_3N_4 diaphragm, while the GaAs membrane is realized through a back-side selective etching using AlGaAs as stop layer, according to the technique described above (see Fig. 2.7). The AlGaAs layer acts also as the dynamic electrode for this particular application. The chromium evaporated on Si_3N_4 is used as the static electrode of capacitive sensors and as the etching mask for structuring 1 µm thick Si_3N_4 at the same time. The air gap between the Si_3N_4 diaphragm and the GaAs substrate amounts to about 2 µm.

2.3.2.2 Surface micromachining

Surface micromachining is based on the deposition of thin films onto the surface of the

wafer and the removal of one or more of these layers to release the structures. Therefore, a surface micromachining process requires a sacrificial layer which is removed at a later step, in a post-process operation, to release the mechanical part. Many materials are used as a sacrificial layer, such as SiO_2, GaAs, AlGaAs, aluminium and others, knowing that each one requires its appropriate etchant.

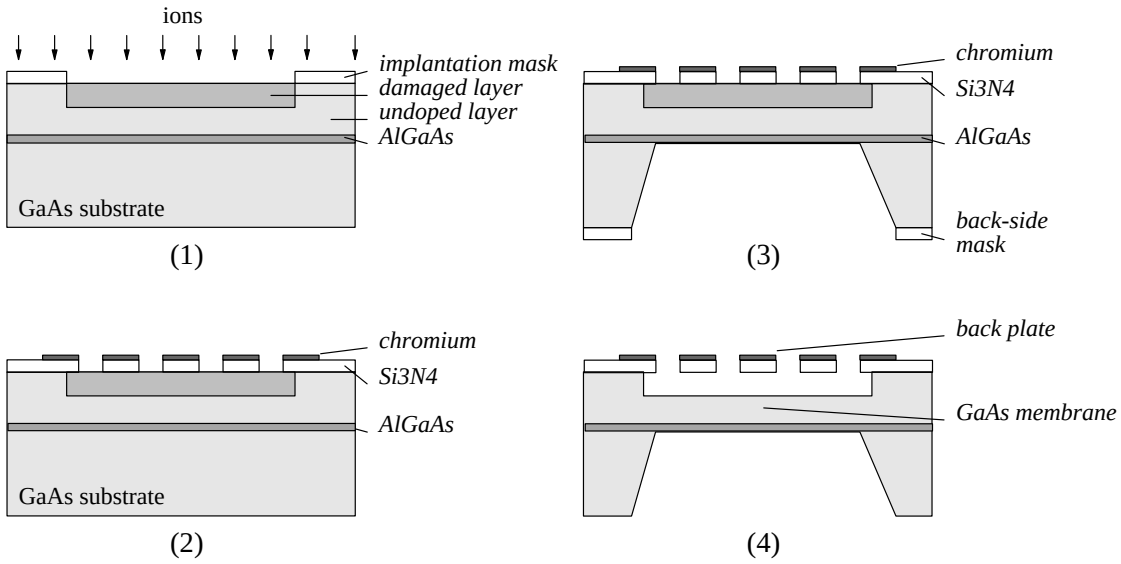


Fig. 2.7 - Fabrication of capacitive pressure sensor combining front- and back-side bulk micromachining techniques [14].

A technique, presented by Vail et al. [19], considers an AlGaAs epitaxial layer as an etch-stop layer and GaAs as sacrificial layer. As depicted in Fig. 2.8a, a layer of GaAs is sandwiched between two layers of AlGaAs. After photolithographic patterning, anisotropic dry etching is used to etch down to the sacrificial GaAs layer. Isotropic and selective dry etching with a $SF_6/SiCl_4$ mixture are then used to etch away such sacrificial layer. It is verified that the contact pad support of the proposed device is much larger than the underetching necessary to free the cantilevers, so contact pads remain supported. Furthermore, the use of dry etching eliminates the problems of surface tension which causes stiction, commonly observed with wet etching.

Another technique used to build GaAs suspended beams uses $Al_xGa_{1-x}As$, with x=0.5 or higher, as sacrificial layer [20][21]. The wafer used has two epitaxial layers, AlGaAs and GaAs, and after the openings defining the width of the beam, the sacrificial AlGaAs layer is accessed and selectively etched by using, e.g. HF (see Fig. 2.8b). In the last example, photoresists are used to suspend structures. This technique, widely applied to make air bridges in MMIC, has been used by Choi and Polla [22] to build piezoelectric pressure sensors and pyroelectric infrared detectors, integrating ZnO thin films in a GaAs MESFET process, as shown in Fig. 2.9.

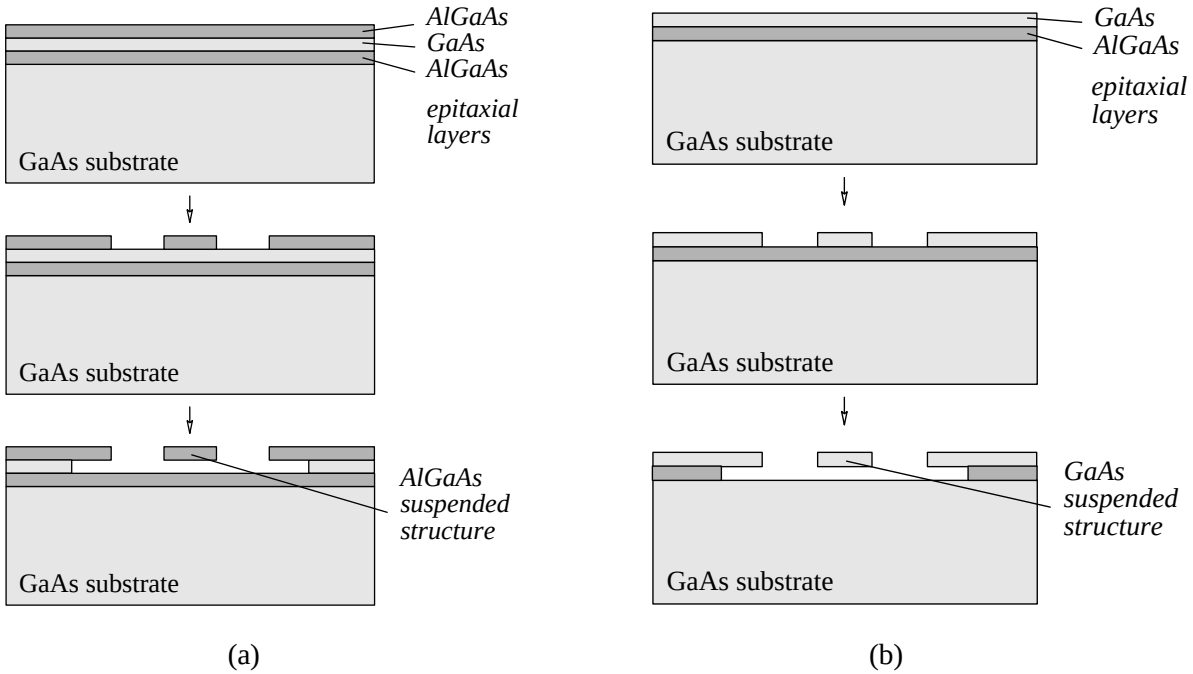


Fig. 2.8 - GaAs surface micromachining using GaAs (a) and AlGaAs (b) as sacrificial layers.

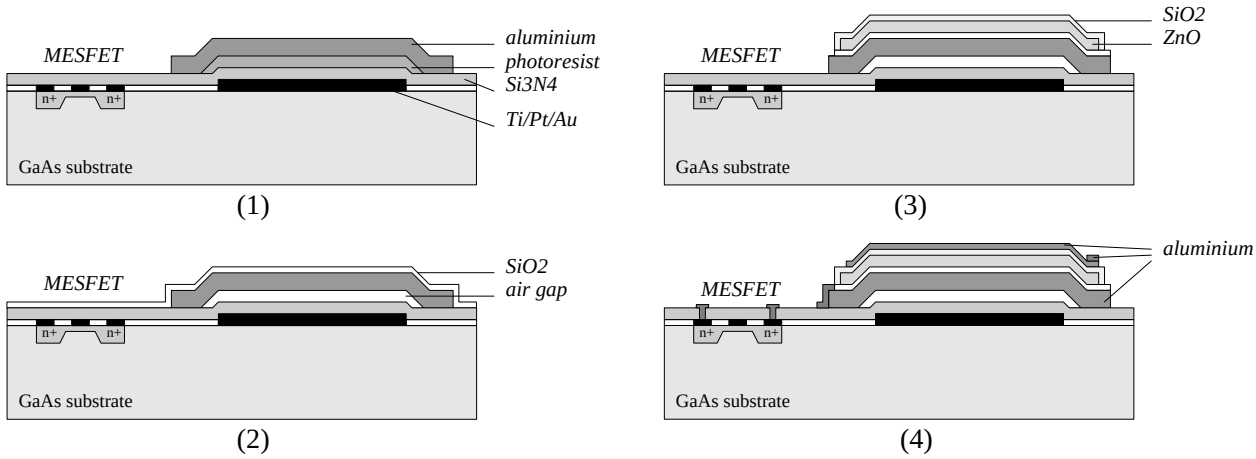


Fig. 2.9 - Fabrication of integrated sensor in MESFET process using photoresist as sacrificial layer [22].

2.4 TIMA-CMP MICROMACHINING APPROACH

The strategy adopted at TIMA-CMP laboratory consists in applying the front-side bulk micromachining in standard IC processes, keeping superposed opening regions in the dielectric layers to access the substrate surface. The structures are then released through an additional post-process wet etching, as illustrated in Fig. 2.10.

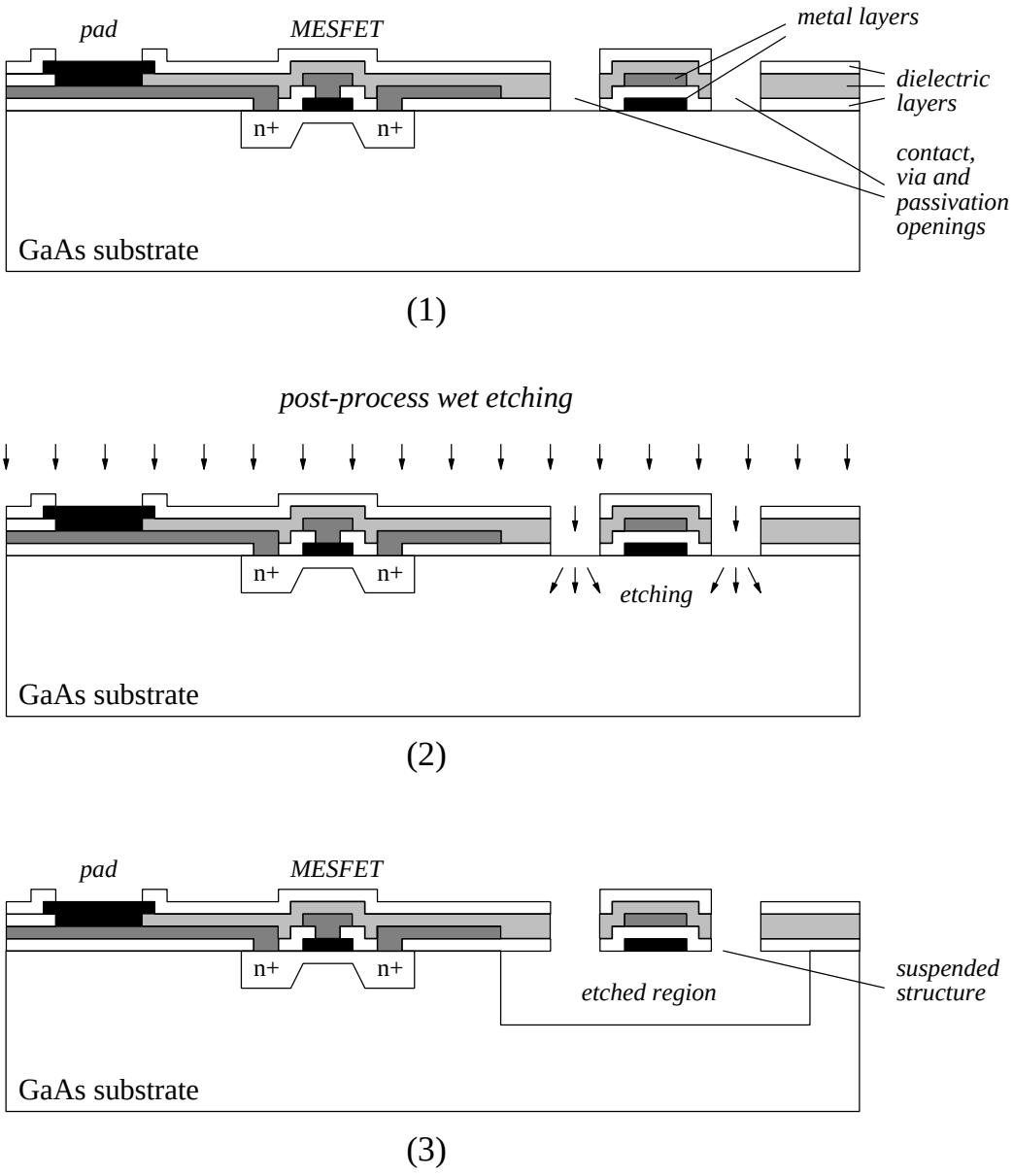


Fig. 2.10 - Maskless front-side bulk micromachining using standard IC process.

The principal advantage of such maskless micromachining approach is the fabrication of microsystems using microelectronics production lines, without modifying the standard IC fabrication procedure. It seems to be the most efficient way to implement monolithic MEMS in terms of time-to-market, fabrication cost and electronic compatibility. The original process parameters, on the other hand, such as dopant concentration, number of layers and masks, layer thickness and others normally cannot be changed. As a consequence, the potential applications for each particular IC process must be carefully studied, since to optimize the process characteristics

for specific micromachined devices in order to improve their performances is not possible in this approach.

CMOS processes have been widely considered for such a micromachining technique [23]-[24]. Useful results have been obtained by the Microsystems Group (MCS), at TIMA laboratory, using 1.2 µm and 1.0 µm CMOS double metal layer technology from ES2 foundry, and 1.2 µm CMOS double metal layer and double polysilicon layer technology from AMS foundry [9]. As a result, a microsystem multi-project wafer service for prototyping and low volume production has been provided by CMP, using these CMOS IC processes [25].

In order to extend the CMP service to alternative MEMS technologies, asimilar strategy has been applied to commercial GaAs technologies, and the related results are presented in the following chapters of this thesis. To our knowledge, this is the first time that such a strategy has been applied commercially. GaAs IC processes available through the CMP, at this moment, MESFET from Vitesse Corp. and HEMT from Philips Microwave Limeil - PML have been investigated for this purpose [26][27]. Nevertheless, the scientific contribution and results obtained in this work, in terms of suitable etching solutions, potential micromachined devices and CAD tools for MEMS, can be easily extended to other GaAs process.

2.5 SUMMARY

In summary, GaAs material seems to be very attractive for MEMS design due to its particular electrical and mechanical characteristics. Hereterojunctions (GaAs and its ternary alloys) are also readily available as sacrificial and stop layers for selective etching. Moreover, preferential etching leads to a unique triangular prism-shaped bridge, not possible in silicon. The microelectronics compatible micromachining approach adopted at TIMA laboratory represents the cheapest and fastest way to implement monolithic MEMS, since the use of an additional maskless post-process wet etching, with no influence on the unconcerned electronic parts, is enough for releasing microstructures. Therefore, microsystems can be fabricated using industrial IC production lines. As a result, multi-project wafer services, such as those provided by CMP since the early 80's, where many projects share the fabrication cost, are easily extended to MEMS design, providing access and capabilities to fabless groups.

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Chapter 3
MICROMACHINING CHARACTERIZATION

GaAs IC-compatible front-side bulk micromachining has been investigated on two technologies : Vitesse MESFET H-GaAs III and PML HEMT D02AH. Since the open areas required in such micromachining approaches are commonly nor expected neither accepted by microelectronics foundries, eventual residual layers have been observed over these openings before the post-process etching. A pre-cleaning procedure is not always enough to solve this problem. For GaAs IC processes where the residual layers are not present or they do not represent a real trouble, three different structures, presenting particular vertical profiles and suspended materials, are proposed for specific applications with special features. Suitable etching solutions have been studied for each kind of structure in terms of undercutting rates, vertical depth rate and profile, as well as possible damage in the passivation and metallization layers. The functionality of electronic devices has also been verified after the post-process wet etching to validate the compatibility with microelectronics blocks.

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3.1 INTRODUCTION

As mentioned in the previous chapter, the front-side bulk micromachining technique compatible with microelectronics processes consists of the use of dielectric layers from IC fabrication, that is, a stack of contact, via and passivation openings is used to create the uncovered substrate regions for the etchant attack. Therefore, the etching solutions are expected to act only or at a very high etch rate on the unprotected surface areas, without influencing the behavior of the devices covered by the passivation and placed far from suspended structures. As a result, no modifications are required in the standard IC fabrication and the micromachined devices are easily constructed as well as the electronic compounds (transistors, diodes, resistors, etc.), resulting on monolithic microsystems at low cost and high yield.

However, it is clear that no improvement or modification on the microelectronics processes for micromachining purposes is allowed. This includes even small changes such as the doping concentration of materials to create more efficient etching stop layers, the thickness of the layers for micromechanical actuator performance, or the addition of new layers and masking steps to the conventional IC fabrication procedure. Others, such as the use of a post-fabrication layer for pad metallization protection and black layers for radiation absorption could be envisaged, but they represent a delicate task. Thus, the technologies targeted for this kind of micromachining technique must be carefully studied in terms of potential applications and their performance limitations.

3.1.1 Target Technologies

The Circuits Multi-Projects (CMP) service provides today the collective fabrication of microsystems using standard IC production lines [1]. CMOS compatible micromachining represents nowadays a reality to the CMP users, which can develop their prototypes with affordable prices and high flexibility. In order to extend such facilities to GaAs technologies, two processes, available through the CMP service at the moment that this work was being realized, were investigated : the 0.6 µm MESFET H-GaAs III from Vitesse Semiconductor Corp. and the 0.2 µm HEMT D02AH from Philips Microwave Limeil (PML) [2][3].

In fact, since IC technologies are constantly in progress, CMP processes are also frequently updated. For example, the Vitesse MESFET is represented nowadays by the H-GaAs IV process, while the ED02AH process corresponds to the PML HEMT technology available in CMP . This is a very important point mainly when microelectronics compatible micromachining approaches are addressed. Even if only a scaling of the dimensions of the layers has been realized, without

changing drastically the fabrication steps and materials, a new micromachining characterization is required to verify the minimum open area dimensions. Otherwise, not only etching parameters, such as temperature and concentration dependence, etch rates, reproducibility and surface damage, but also new mechanical and thermal properties of layers must be obtained.

The Vitesse H-GaAs III process is used for high speed digital circuits and presents both depletion and enhancement mode MESFETs with 0.6 μm effective gate length [2]. The four metal layers available for interconnection provide high levels of integration at a great yield. Therefore, for micromachining applications, the stack of six dielectric openings is necessary, that is, opening in the dielectric cap window (substrate access), intermetallic layer openings (via_1, via_2, via_3 and via_4), and passivation opening, as illustrated in Fig. 3.1. In fact, the superposition of consecutive vias is not allowed by the foundry, and such openings require the presence of the respective metal layers. Moreover, the minimum passivation opening width in the pad structure is 75 μm. As a consequence, these electronic design rules must be violated to obtain the opening regions. Furthermore, an [100]-oriented GaAs wafer is used by Vitesse, and the [010] and [001] crystallographic directions correspond to X (horizontal) and Y (vertical) layout axes, respectively. Such a kind of information is necessary when preferential etching is considered.

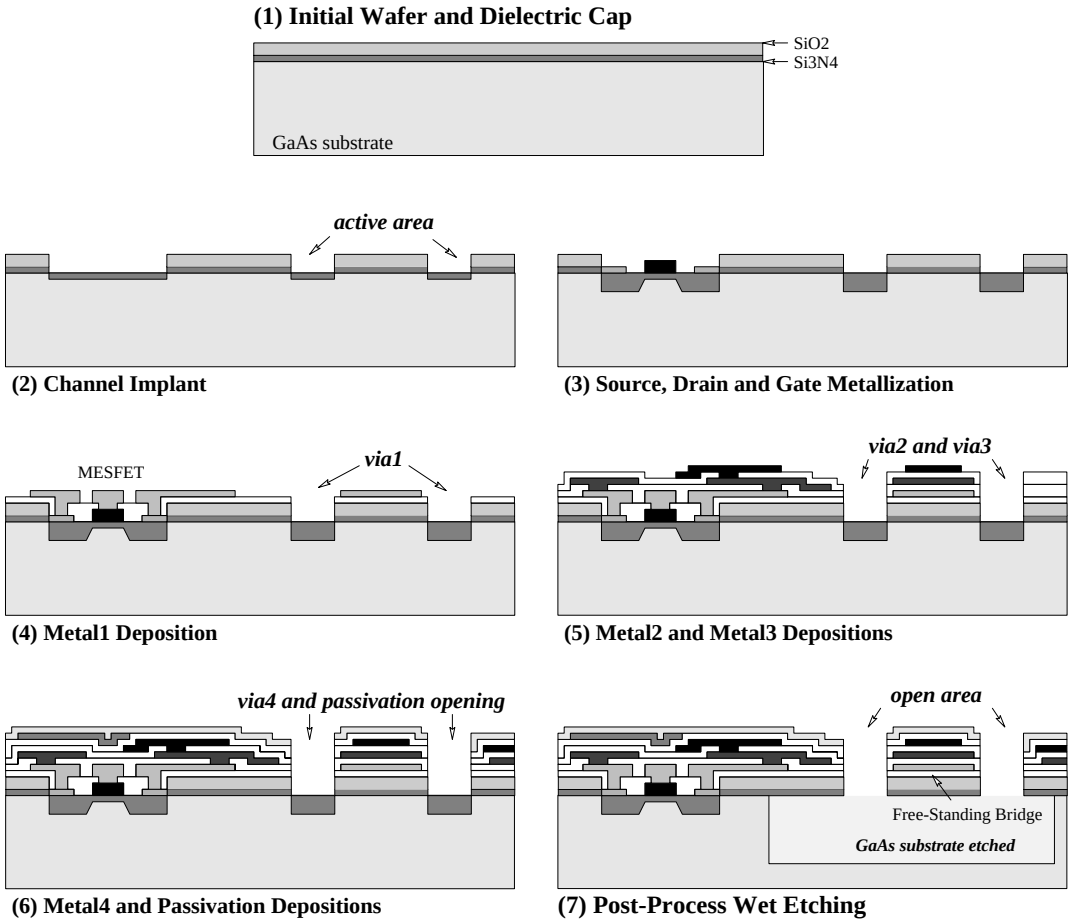


Fig. 3.1 - Front-side bulk micromachining using Vitesse MESFET H-GaAs III process.

On the other hand, the PML D02AH process is provided for microwave and millimeter wave applications up to 70 GHz. The main features of this technology are the depletion mode 0.2 µm recessed gate pseudomorphic HEMT, back-side metal plate (ground) for microstrip transmission line construction, via holes through the 100 µm-thick substrate to reduce parasitic inductances to ground, and passive compounds (GaAs resistors, MIM capacitors and planar spiral inductors) [3]. Four metal layers are available for gate, capacitors and interconnections. However, to obtain the micromachining open regions on the substrate surface, stacking of only two layout layers, contact opening (CO) and contact bonding (CB), is demanded (see Fig. 3.2). Like in Vitesse, such superposition is not expected by the foundry, except for logo design, representing consequently a design rule violation. PML also uses an [100]-oriented wafer, but in this case, the horizontal (X-axis) and vertical (Y-axis) layout directions correspond, respectively, to the [011] and $[01\bar{1}]$ directions.

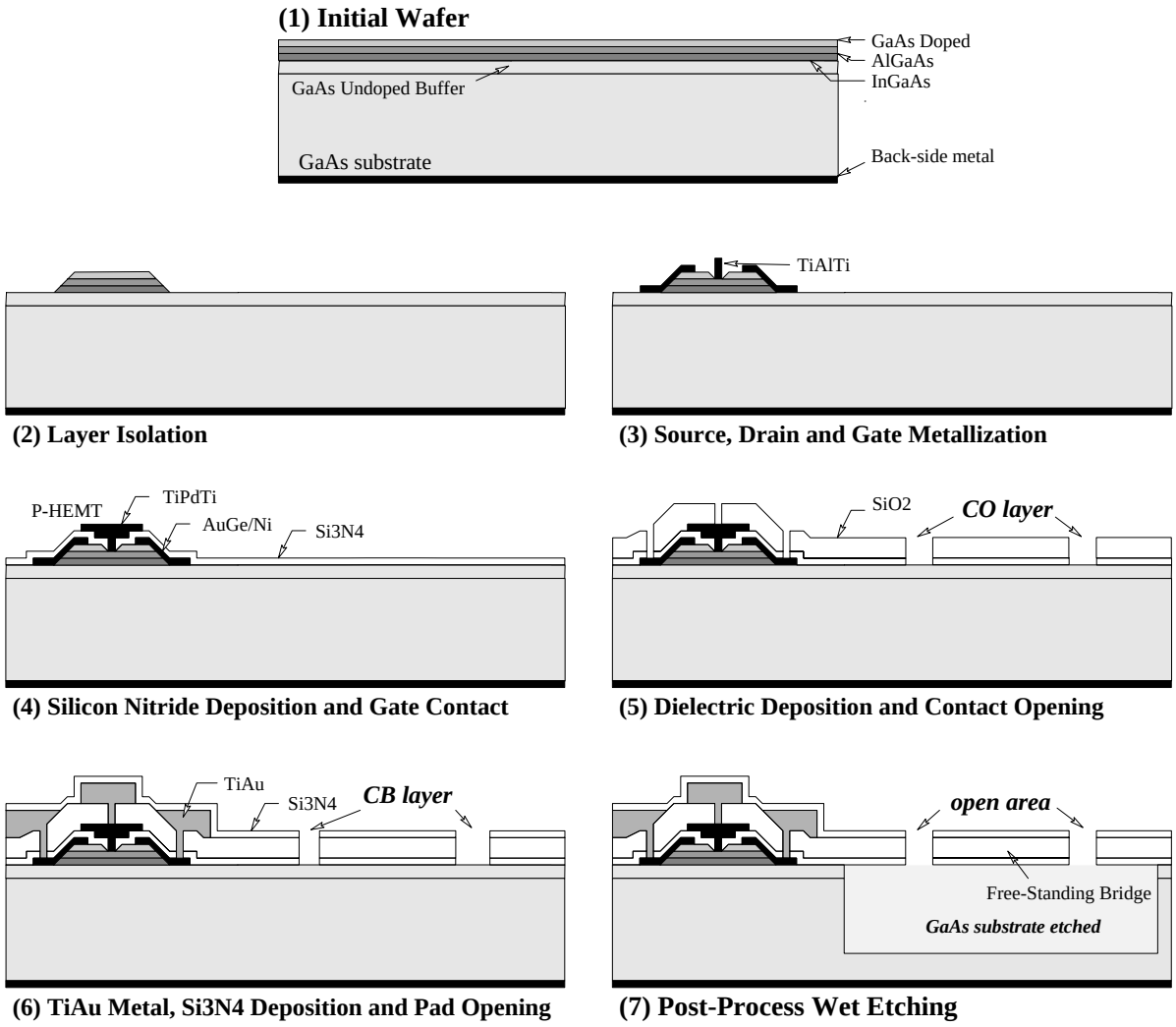
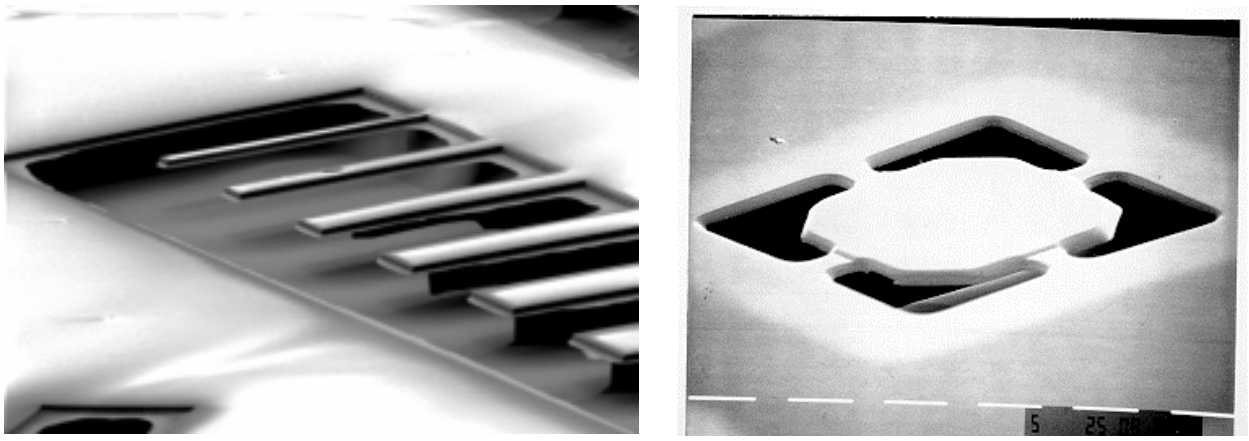


Fig. 3.2 - Front-side bulk micromachining using PML HEMT D02AH process.

3.1.2 Residual Layer

The first studies, carried out by Karam et al. [4], aimed to demonstrate the feasibility of such approach. Test structures were implemented with a wide range of open area widths in order to obtain the exposed substrate surface regions, after IC fabrication. Next, such structures were released using well-known GaAs etching solutions. Although suspended structures were successfully built in this preliminary experiments, as shown in Fig. 3.3, problems of residual layers over the uncovered regions were eventually observed, even with large open areas. These problems are supposed to be caused by inadequate dielectric openings during IC fabrication, giving a significant increase of dielectric thicknesses over the open areas. This was mainly observed when the number of metal and intermetallic layers available in the process increased.



(a) (b)

Fig. 3.3 - GaAs micromachining using Vitesse H-GaAs III (a) and PML D02AH (b) processes.

Moreover, the contact between air and GaAs material, in unprotected regions, could result in surface oxide layers during the period between the end of the IC fabrication and the post-process etching procedure, commonly not carried out in the same environment. Numerous methods for removing such residual layers are discussed in the literature [5]. Among Ga and As oxides, all oxides of arsenic, such as As_2O_3 and As_2O_5 are highly soluble in water, alcohols and acids; As_2O_3 dissolves in alkaline solutions as well. In contrast, Ga_2O_3, Ga_2O_3 (H_2O), and Ga_2O (suboxide) are insoluble in water, slightly soluble in acids, and readily soluble in alkaline solutions.

In fact, residual layers were observed to be more critical in Vitesse MESFET dies than in the PML HEMT ones, whose minimum open area width was determined to be equal to 4 µm (after discussions with the foundry) even if smaller openings are obtainable with test patterns. On the other hand, in Vitesse MESFET, open area widths up to 200 µm were designed, but residual layers are almost always present mainly at the borders of the openings, as illustrated in Fig. 3.4. Note that such a trouble is not particular to GaAs technologies, but an actual drawback for front-side bulk micromachining using certain IC processes. For instance, similar residual layers were observed in CMOS compatible micromachining using the ATMEL-ES2 ECPD10 process, while thery were not so critical in the AMS CAE process [6].

Therefore, a pre-cleaning step is applied on the dies in order to remove the residual layers and to avoid eventual problems and/or irregularities in the micromachining task. This is made by dipping them in HCl:H_2O (1:10) - 20 sec, then rinsing in deionized water - 10 sec, dipping in NH_4OH:H_2O (1:1) - 20 sec, and, finally, drying with nitrogen. Next, the dies are dipped in specific etching solutions, taking into account parameters such as concentration, temperature and stirring dependence. Such procedure has been successfully realized on the PML dies, but in the case of the

Vitesse dies the residual layers could not be removed, probably because the residual materials are not only Ga and As oxides, but also interconnection metals and particular dielectrics, not specified by the foundry.

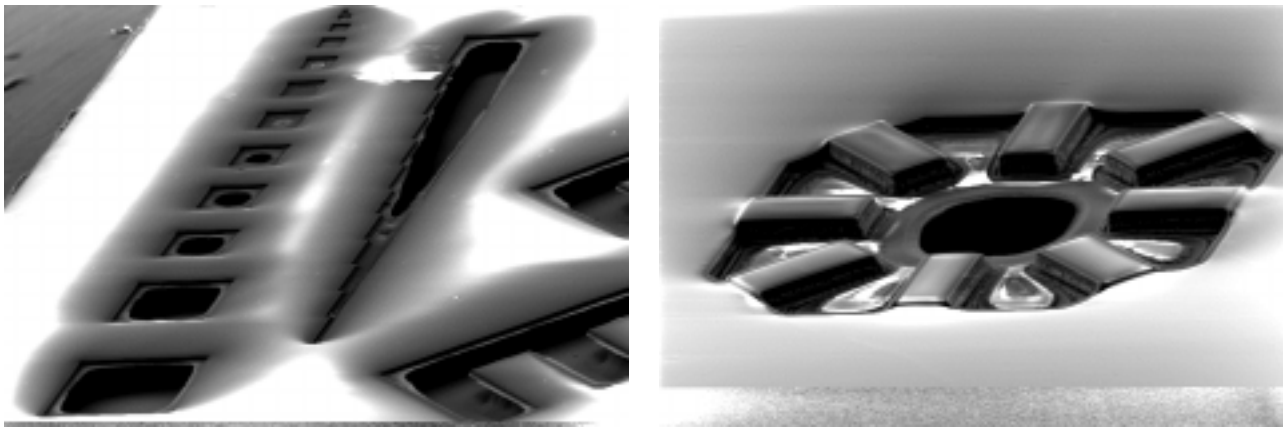


Fig. 3.4 - Residual layers over open areas, after IC fabrication using Vitesse H-GaAs III process.

3.2 WET ETCHING MECHANISM AND ETCH RATE DIAGRAM

Before presenting the different kind of suspended structures which are firstly proposed in this work and their related etchants, the general mechanisms of GaAs wet etching and the generation of etch rate polar diagrams are briefly reviewed next. It must be remembered that the word 'preferential' is used to describe a process in which the etching of certain crystallographic planes occurs faster than others, and the slowest etching crystal planes dictate next the final shape of the etched groove. Etching is then anisotropic with respect to crystal directions. In contrast, the word 'selective' is reserved to etches that remove one material significantly faster than another. The differences in etch rates could be caused by either different etch mechanisms or differences in contact potentials with respect to the etch solution.

Chemical etching of most III-V semiconductor materials usually proceeds by an oxidation-reduction reaction at the semiconductor surface, followed by dissolution of the oxide material. The chemical etchant usually contains two separate components, one which acts as the oxidizing agent (commonly H_2O_2) and the other which dissolves the resulting oxide (usually an acid) [5][7]. Two classes of etchants can be defined: diffusion-limited etchants and reaction-rate-limited etchants. In diffusion-limited etching, the material dissolution depends on the transport of active etching components by diffusion to the material surface or of the reaction products away from the surface. In the reaction-rate-limited, the material dissolution is a function of the chemical reaction rate between the etchant and the semiconductor (or oxide). Some characteristics of such mechanisms are discussed bellow, while a more detailed study about wet etching in GaAs substrates can be found in [8] :

• *Agitation dependence* — In a reaction-rate-limited etching process the agitation does not change the surface absorption rate significantly, while for a diffusion-limited etching condition the etch rate increases with stirring or agitation of the liquid etchant.

• *Mask edge trenching* — For diffusion-limited etchants, the etch rate for GaAs through a small opening in a mask is found to be considerably higher than that for a GaAs wafer with no masking. For reaction-rate-limited etching, the etch rate is independent of the mask opening dimensions.

• *Anisotropic etching* — In GaAs, due to its crystallographic polarity, a free {111}Ga surface has Ga atoms attached firmly to three As atoms underneath and the valency of 3 of Ga is completely satisfied [9]. The {111}As plane, on the other hand, contains As atoms that have two extra unbound electrons per atom owing to its valency of 5. Since oxidation involves loss of electrons, the As atoms present on a {111} As surface react much more readily with the oxidizer than Ga atoms present on a {111}Ga surface do. Once an As atom from an {111}As surface is removed by oxidation, the Ga atoms in the plan underneath, which are each connected to the other underlying As atoms by a single bond, are dislodged relatively easily by the oxidation process. Consequently, {111}As etch rate is found to be by far the highest in GaAs for reaction-rate-limited etching processes. For diffusion-limited processes, the etch rate dependence on orientation almost disappears.

• *Temperature dependence* — Etch rates always increase with etchant temperature because the rates of all the participating physical and chemical phenomena increase as $e^{-\Delta E/kT}$, where T is temperature and ΔE is the relevant activation energy. In fact, reaction-rate-limited etching processes generally show a stronger temperature dependence than diffusion-limited etching processes.

• *Time dependence* — The reaction-rate-limited etching process presents etch rates linearly proportional with the etching time, while in the diffusion-limited process etch rates are proportional to the square root of the etching time.

• *Galvanic effect* — A reaction-rate-limited etching mechanism depends on the availability of electrons for oxidation to occur. A material having an electronegativity that is different from the electron affinity for GaAs, when immersed in the etch solution, would form a galvanic cell. The galvanic action would then supply electrons for the etching reactions to progress at a faster rate. Such an etch rate increase would be smaller for diffusion-limited etching processes provided that the physical separation of this dissimilar material from GaAs is much larger than the diffusion layer

thickness.

• *Doping type and concentration dependence* — Reaction-rate-limited etching is much more dependent on the doping concentration and type, owing to its dependence on the availability of electrons and holes.

• *Chemical polishing effects* — If the surface has a protusion, the tip would be exposed to a higher diffusion current of reacting agents and therefore a diffusion-limited etchant tends to make the surface smoother. A reaction-rate-limited etchant, however, would maintain the original surface topography, unless of course its anisotropy takes over. In such a case, it would etch the fast etching planes quickly and stop at the slowest etching planes, creating characteristic patterns.

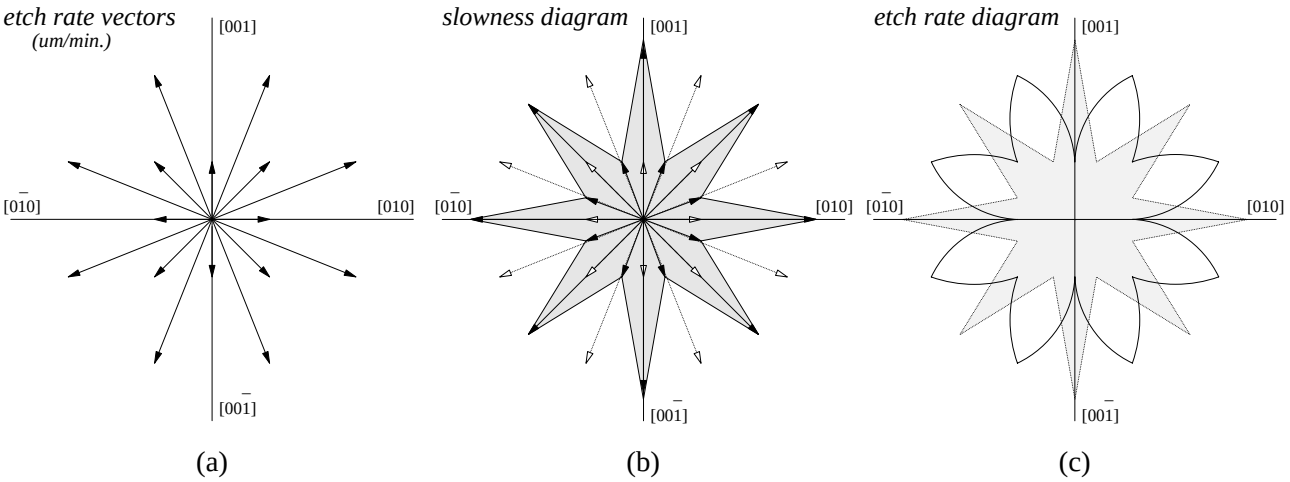
• *Etch rate magnitudes* — The reaction-rate-controlled etching condition occurs when the surface reaction rate, e.g., oxidation, is low due to the small concentration of the oxidizer in the solution. As the oxidizer concentration is increased, the etch rate increases and the complexing action keeps up with the oxidation rate, producing an almost linear relationship between the etch rate and the oxidizer concentration. Eventually, the etch rate dependence on oxidizer concentration becomes sublinear, as the complexing action fails to keep up with oxide growth. Consequently, one has to increase the concentration of the complexing agent as well in order to have an increased etch rate. However, the solution becomes viscous and the etching process becomes diffusion-limited. The etch rate flattens out and starts dropping owing to the inability of the oxidizer (H_2O_2 molecules) to reach the GaAs surface freely.

Generally, the etch rates, measured normal to the actual crystal surface, are described in a polar plot in which the distance from the origin to the plot surface (or curve in two dimensions) indicates the etch rate for that particular normal direction. The extraction of experimental etch rates for all directions represents a lot of work, and it is rarely found in literature. However, for a determined crystallographic plane, a two-dimensional etch rate diagram can be accurately predicted or generated from known minimum and maximum rates that correspond, respectively, to the etch stop planes and planes easily etched away by the solution. This procedure can be represented through a simple computing algorithm, as following :

a) assume hypothetical etch rates, given in Fig. 3.5a;

b) the inverse of etch rate values are used to build the slowness diagram, shown in Fig. 3.5b;

c) then, the inverse of each straight line equation between two slowness vectors is used to construct the etch rate diagram, illustrated in Fig. 3.5c.



(a) (b) (c)

Fig. 3.5 - Generation of etch rate polar plot from available minimum and maximum values.

As in two dimensions, the analysis of what happens to three-dimensional crystal etching is most conveniently carried out with the help of the etch rate or slowness diagrams. Now the slowness diagram is a 4π polar diagram that contains the necessary information for all possible directions. Around the skeleton formed by the extreme rate values expected and additional intermediate directions based on available data, the complete slowness surface is then approximated with a triangulated polyhedron that uses the given values as corners [10]. In fact, the generation of a 3D etch rate diagram is a somewhat complex computing task which is beyond the scope of this work [11][12].

3.3 MICROMACHINED STRUCTURES PROPOSED

The surface geometry of suspended structures is easily defined by placing appropriately the open areas on the layout. Certainly, undercutting rates and anisotropic etching behavior contribute to the releasing feasibility of particular geometries since large structures could be limited by the maximum etching time allowed. In terms of the suspended materials and vertical profile, three kinds of free-standing structures have been investigated :

- GaAs/AlGaAs mesa-shaped structure,
- GaAs triangular prism-shaped bridge and
- suspended metal / intermetallic layer structure without GaAs material.

In this section, these structures are described and evaluated considering the PML HEMT technology. Note that, in the case of Vitesse MESFET, the absence of heterostructures discards the possibility of building the suspended GaAs/AlGaAs mesa-shaped structure or similar because it relies on the selective etching property.

The manufacturing of the microstructures relies on the use of selective etching solutions (GaAs over AlGaAs) and crystallographic preferential (anisotropic) etching systems. For both selective and preferential etchants, the etch rates were determined by observing the undercutting distances around the opening areas (etch mask) and cross section profiles. By considering the well-known III-V semiconductor compound-based etching systems previously presented in the literature, particular selective and preferential etching systems for the suspended GaAs/AlGaAs mesa-shaped structure and triangular prism-shaped bridge have been chosen. Note that the goal is not to develop new etchants, but to adapt existing solutions to these requirements.

3.3.1 Suspended GaAs/AlGaAs Mesa-Shaped Structure

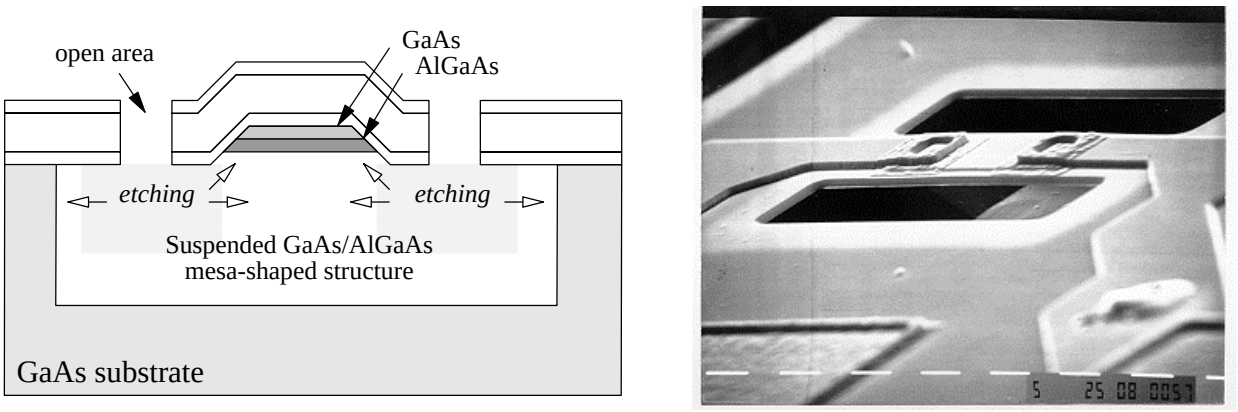
3.3.1.1 Structure description

The suspended GaAs/AlGaAs mesa-shaped structure, depicted in Fig. 3.6a, consists of placing a mesa structure, commonly used to fabricate resistors and HEMTs, between open areas for selective releasing. During the post-process etching, AlGaAs acts as a stop layer to maintain the top GaAs epitaxial layer, while the GaAs substrate material as well as the InGaAs layer are etched away. Therefore, the etching selectivity of GaAs with respect to AlGaAs represents the principal parameter to be controlled. InGaAs could also be considered as stop layer due to its selectivity with respect to GaAs [7][13]. However, due to its very small thickness, etching solution selectivity higher than 10^4 should be available to obtain reasonable microstructure dimensions. Thus, such possibility was temporarily discarded.

In the PML HEMT D02AH process, InGaAs, AlGaAs and GaAs doped layers, depicted in Fig. 3.2, present thickness of approximately 100Å, 500Å and 550Å, respectively. As a result, to build, for instance, a 10 µm-width GaAs bridge a selectivity of more than 100 must be applied, before starting an etching attack on the GaAs doped layer. Generally, higher selectivity could be obtained using dry etching [14][15], however in the case of microelectronics compatible micromachining based on a post-process etching such possibility has not been considered due to the risk of surface layers contamination and influence on the electronic active devices.

Note that the undercutting rate is the principal responsible for releasing the structure. Therefore, it is more interesting to consider isotropic etching, for design flexibility, rather than anisotropic behavior, which usually imposes the open area orientation because of the presence of stop etching crystallographic planes, without forgetting the selective property. In terms of potential applications, this kind of suspended structure could be efficiently used to create free-standing GaAs resistors, as shown in Fig. 3.6b, useful to realize bolometers, piezoresistive-based sensors and

metal-semiconductor thermocouples.



(a) (b)

Fig. 3.6 - Suspended GaAs/AlGaAs mesa-shaped structure: (a) illustration and (b) GaAs resistor.

3.3.1.2 Selective etchants

As mentioned, the suitable chemical etching solution has to be capable of rapid selective removal of a part of the crystal or specific material(s), with a given chemical composition, without damaging or removing the rest of the crystal or etching stop material(s). This leads to the definition of the selectivity coefficient *S* of the solution :

$$S = \frac{R_1}{R_2} = \frac{etching\ rate\ of\ GaAs}{etching\ rate\ of\ Al_xGa_{1-x}As} \tag{3.1}$$

observing that the optimal solution exhibits a maximum in R_1 and *S*, while R_2 should remain very small. Moreover, assuming that the etch rates are independent of the etching time, they are calculated simply by dividing the etched depth and undercutting distances by the etching time.

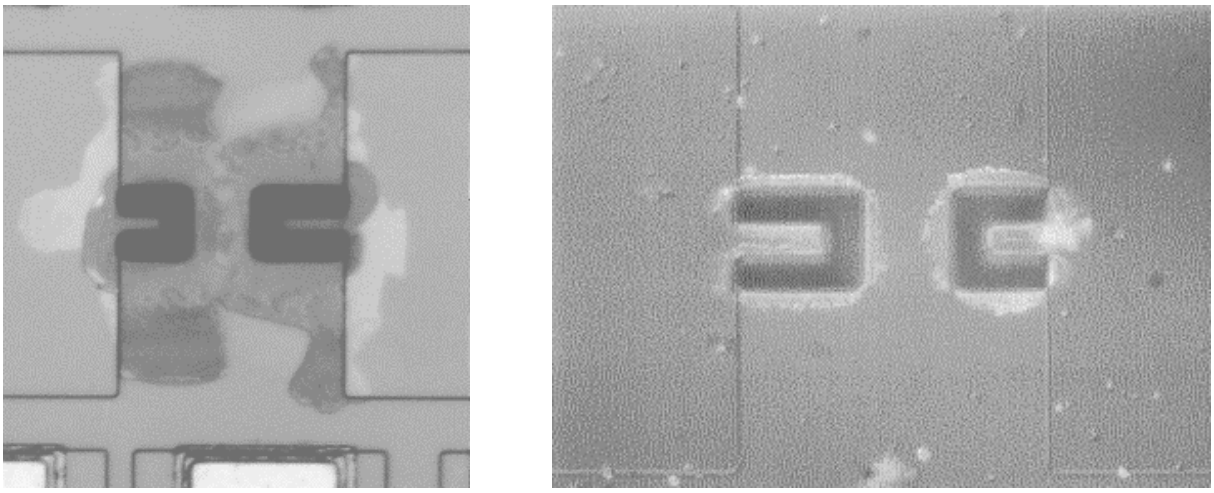
Three selective wet etching systems of GaAs with respect to AlGaAs have been found in the literature and investigated : **$NH_4OH:H_2O_2$**, **$C_6H_8O_7:H_2O_2:H_2O$** (citric acid), and **succinic acid:$NH_4OH:H_2O_2$** [16][17]. Etching solution concentrations were chosen taken into account the highest selectivity presented by the authors. The attention has also been focused on the uniformity and reproducibility of such etching procedure. Note that, the solution selectivity is generally associated with the composition of $Al_xGa_{1-x}As$ (x value), which is equal to 0.25 in the case of PML D02AH process.

$NH_4OH:H_2O_2$ — The NH_4OH-based solution for selective etching of GaAs in the presence of AlGaAs epitaxial layers was firstly proposed by Logan et al. [18], whose technique required a

rotating station holding the crystal and the etching solution. They obtained a low *S* value approximately equal to 10 for the GaAs-AlGaAs system. In addition, the etching of GaAs was very slow, $R_1 \approx 6$ µm/h, for the optimal solution composition. Among other publications about NH_4OH selective solution, J. J. LePore [19] and K. Kenefick [20] obtained selectivities up to 30, while Y. Uenishi et al. [21] presented the highest selectivity about 100 for volume ratios between 1:30 and 1:50. In this work, both concentrations were applied, at room temperature and with stirring, and the undercutting rates measured were 2 and 1 µm/min, respectively, presenting an almost isotropic behavior. However, probably due to the high concentration of H_2O_2 in the solution and a bubbling-accelerated effect of the system, non-uniform etching surface profiles have been noticed after 5 min (see Fig. 3.7a). In fact, it is suspected that one or both dielectric layers (SiO_2 and Si_3N_4) are attacked and an irregular bulk etched shape is formed. Anyway, such an etching system does not seem to be suitable for building reliable microstructures.

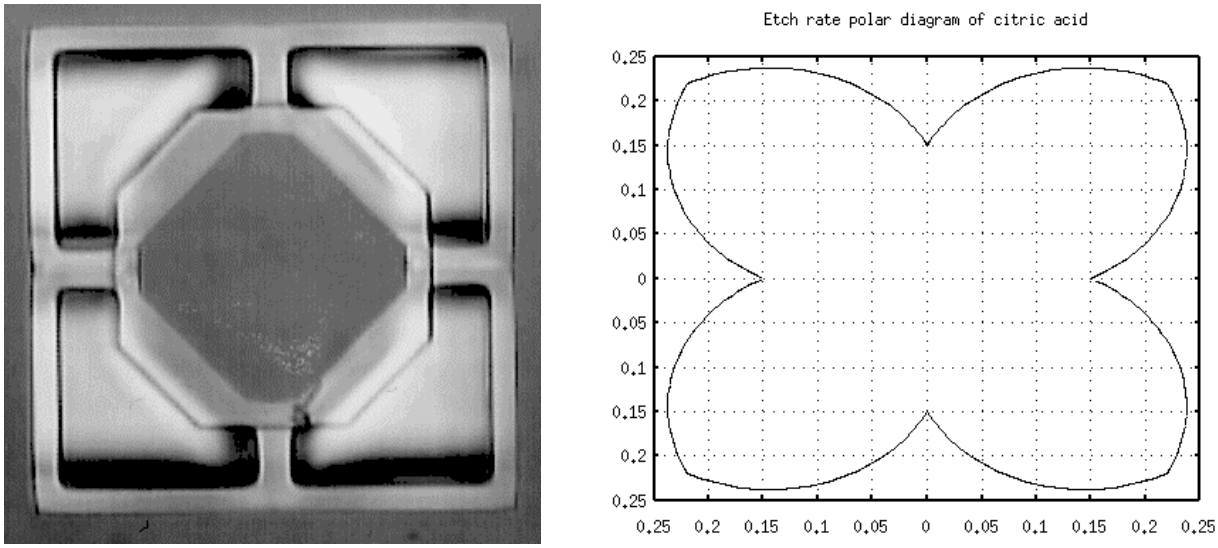
Succinic acid:NH_4OH:H_2O_2 — According to K. Hjort [16], this system should present a complete selectivity of GaAs to AlGaAs, with an etch rate of 0.2 µm/min, based on the results presented by S. Merritt et al. [22], though it is not clear in the original publication. The volume ratio proposed by Merritt and applied herein was 15:1. After 60 min of material exposure to the etching solution, at room temperature and without stirring, an insignificant undercutting of around 0.5 µm was observed. As a consequence, this too slow lateral etching leads to very long etching time for the fabrication of free-standing structure with reasonable dimensions. Stirring or temperature effects should be investigated in order to increase the etch rates, but it may probably affect the selective characteristics of the etchant. Moreover, similar irregularities in the surface etching profile presented by NH_4OH-based solution was observed after two hours (see Fig. 3.7b).

$C_6H_8O_7$:H_2O_2:H_2O — Several publications have shown citric acid as a selective etching solution of GaAs to AlGaAs, with a selectivity of approximately 100 [7][14][23][24]. In general, the 5:1 volume ratio, at room temperature and without stirring, has presented the best results and it was considered in this work. A slower etch rate than the NH_4OH based solution was observed but with an excellent reproducibility and uniformity, as shown in Fig. 3.8a. Undercutting rates around of 0.15 and 0.31 µm/min were measured for the <011> and <001> surface directions. The etch rate polar diagram relative to the die surface plane (100) is depicted in Fig. 3.8b. At the present time, these results suggest to use the citric acid system to fabricate the suspended GaAs/AlGaAs mesa-shaped microstructures.



(a) (b)

Fig. 3.7 - Surface etching profile obtained with (a) NH_4OH and (b) succinic acid based solutions.



(a) (b)

Fig. 3.8 - Citric acid based selective solution: (a) surface etched shape and (b) etch rate polar diagram.

3.3.2 Free-Standing Triangular Prism-Shaped Bridge

3.3.2.1 Structure description

The triangular prism-shaped structure, proposed firstly by Tarui et al. [25] and illustrated in Fig. 3.9, is possible due to the anisotropic etching behavior of certain etchants. It is well known that the III-V semiconductor compounds with zinc blende structure exhibit polarity along the <111> directions. Then, the difference between the etch rates of A{111} planes and other low-index planes results in crystal habits forming the particular V-shaped and the reverse mesa-shaped holes in the

(011) and (01$\bar{1}$) planes, respectively [25]-[27]. To obtain such a structure, particular etching characteristics must be taken into account such as the etch rates of B{111} planes higher than the A{111} planes, in order to reach the desirable profile (negative slope angle), and {100} planes higher than the A{111} ones, to reduce the undercutting distance in respect to the etched depth.

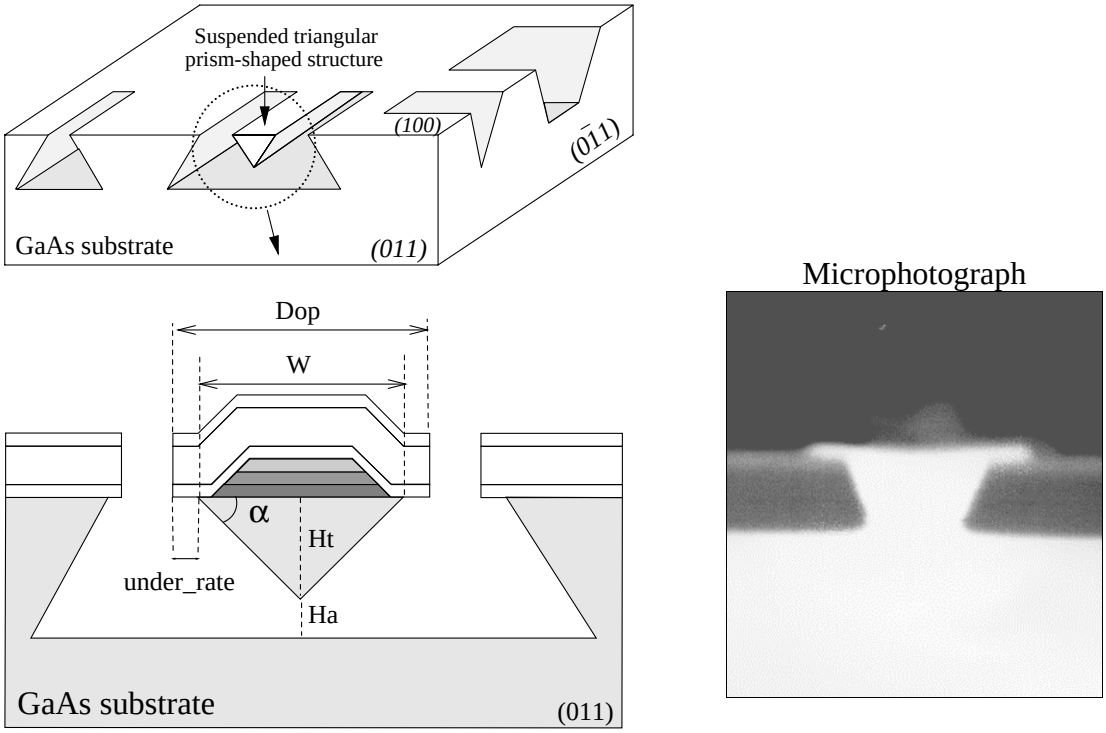


Fig. 3.9 - Free-standing triangular prism-shaped bridge.

According to Fig. 3.9, the base of the inverse triangle (W) and the distance between the bottom of the bridge and the substrate material, that is, the air gap height (H_a) are usually defined by the designer. Moreover, the triangle height (H_t) can be calculated as a function of W :

$$H_t = (W / 2) * \mathrm{tg}(\alpha) \tag{3.2}$$

where α corresponds to the negative slope angle. Therefore, the etching time (*etch_time*) required to obtain such a structure with determined W and H_a can be easily estimated by using :

$$etch\_time = (H_t + H_a) / depth\_rate \tag{3.3a}$$

or

$$etch\_time = (W / 2 * \mathrm{tg}(\alpha) + H_a) / depth\_rate \tag{3.3b}$$

where *depth_rate* represents the etch rate in the [$\bar{1}$ 00] crystallographic direction (depth). As a result, to determine the appropriate open area distance (D_{op}), considering the undercutting or lateral etch rate (*under_rate*), the following equation can be applied :

$$D_{op} = 2 * under\_rate * etch\_time + W \quad (3.4)$$

Note that, unlike the suspended GaAs/AlGaAs mesa-shaped structure, the undercutting rate is desired to be as low as possible in order to reduce the lateral etching and, consequently, the open area distance and the final structure size.

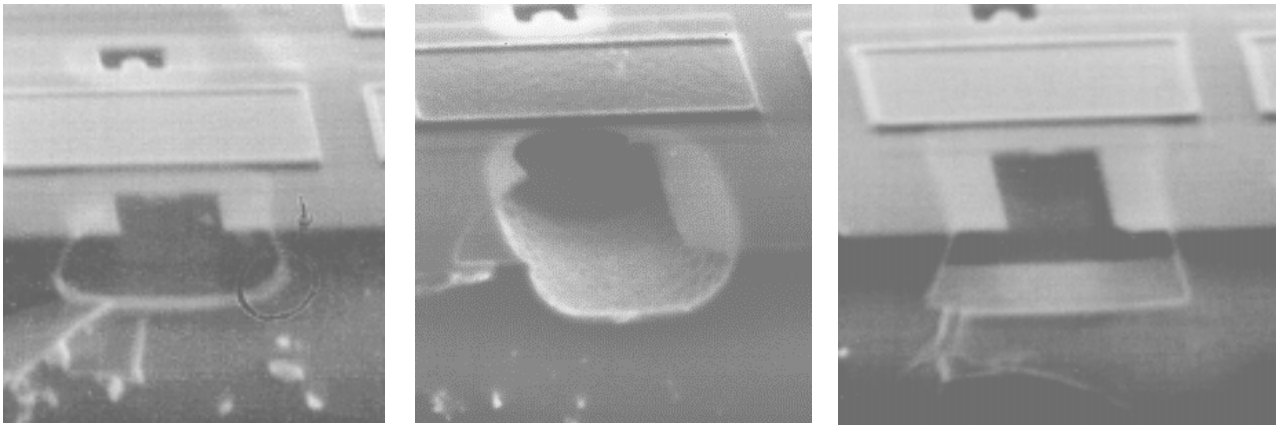
The potential applications targeted with this kind of bridges are the piezoelectric cantilevers, since a significant GaAs mass could be suspended, and free-standing active devices (diodes and transistors) for thermal isolation. Thermocouple-based devices could also be thought, but it is clear that the increased material mass underneath the structure increases the thermal conductivity, reducing the performance of the thermocouples.

3.3.2.2 Anisotropic etchants

In the etchant characterization for this structure, it is very important to verify the vertical profile obtained on the (011) cleavage plane with each etching system. The vertical and lateral etchings have to be well controlled to release the expected shape and are closely related to the open area geometry. Well-established preferential chemical etching systems, proposed in the literature, such as **H_2SO_4:H_2O_2:H_2O**, **H_3PO_4:H_2O_2:H_2O**, **NH_4OH:H_2O_2:H_2O** and **Br_2:CH_3OH**, are evaluated next. All etching procedures were carried out without stirring and at room temperature, with exception of the H_3PO_4 based system also applied at 0°C [28]. Experimental results are summarized bellow :

H_2SO_4:H_2O_2:H_2O — This system has been well characterized in the literature as a preferential etching solution. Iida et al. [26] used a variety of etch solution concentrations to extract the ternary etch rate diagram with respect to the {100} crystallographic planes. The etch rate polar diagram for the {110} planes was proposed by D. Shaw [29] and validated using a 2D anisotropic etching simulator based on a geometrical method. Considering their results, two volume ratios — 1:8:1 and 1:8:0 — were studied in this work. In the case of the 1:8:1 vol., the depth etch rate was measured equal to 7 µm/min, the undercutting rates obtained for the <011> and <001> crystallographic directions were 4 and 6 µm/min, respectively. The 1:8:0 vol. solution, which were expected to etch more rapidly, presented etch rates of 10, 6 and 9 µm/min for the [$\bar{1}$ 00] depth, <011> and <001> surface directions, respectively. However, for both concentrations the aparition of the B{111} planes, already predicted by D. Shaw [29] and D. MacFadyen [8], were observed between the A{111} habit planes and the (100) hole bottom surface (see Fig. 3.10a). This could represent an undesirable effect during the construction of such a kind of bridge.

H_3PO_4:H_2O_2:H_2O — This solution was proposed by Mori et al. [28] as a more stable etching system than the H_2SO_4 based one. Through the equivalent ternary etch rate diagram, it is verified that the preferential etching occurs when the mole ratio of H_2O_2 to H_3PO_4 is higher than 2.3, and the mole fraction of H_2O is lower than 0.9. Experiments were realized for the volume ratio of 1:13.8:13.2 at room temperature and at 0°C. A significant temperature dependence with respect to etch ratio B{111}/A{111} was observed, that is, the process becomes more isotropic when increasing the etching temperature, as shown in Fig. 3.10b [28][30]. At 0°C, the depth etch rate around to 1 μm/min was measured, while the undercutting rates for the <011> and <001> surface directions, respectively, were calculated to be approximately equal to 0.25 and 0.35 μm/min.



(a) (b) (c)

Fig. 3.10 - Vertical etching profiles obtained using (a) H_2SO_4, (b) H_3PO_4 and (c) NH_4OH based solutions, at room temperature and without stirring.

NH_4OH:H_2O_2:H_2O — The characteristics of this solution seem to be as good as the H_3PO_4 based system at 0°C, as show in Fig. 3.10c [31][32]. The two concentrations applied in the experiments, 20:7:973 and 20:7:73 vol., gave depth etch rates of 0.5 and 0.6 μm/min, respectively. The undercutting rates measured for the <011> and <001> directions were, respectively, equal to 0.15 and 0.22 μm/min for the 20:7:973 vol., and 0.6 and 0.9 μm/min for the 20:7:73 vol. Although, for 20:7:973 solution the kinetics of microstructure releasing is weak, this concentration seems suitable due to the higher aspect ratio between the depth and the <011> undercutting distances, which is aproximately 3.3, while for H_3PO_4 the same ratio is equal to 4. It has direct influence on the final structure vertical profile.

Br_2:CH_3OH — This solution with bromide concentrations less than 0.05 by weight was applied in order to increase the etch ratio B{111}/A{111} for the desirable profile, and to avoid the formation of {332}Ga as habit planes discussed in [25][33]. However, non flat-bottomed holes

were always observed, compromising the feasibility of the triangular-shaped microstructure. Moreover, even with low Br_2 concentrations, the pad metallization was hardly attacked, as shown in Fig. 3.11, making it unsuitable for the electronic compatibility using this macromachining technique.

In summary, H_3PO_4:H_2O_2:H_2O and NH_4OH:H_2O_2:H_2O systems seem to be well adapted for fabricating uniform triangular prism-shaped bridges. For both solutions, the angle between the negative slope plane and the surface is approximately equal to 70 degrees, which represents the A{111} crystallographic plane. Moreover, HCl and HF based solutions, also presented as anisotropic etchants in the literature [29][34][35], were rejected due to the well known high reactivity on the pad metallization (alluminum and other metals) and the passivation materials (Si_3N_4 and SiO_2) [36][37].

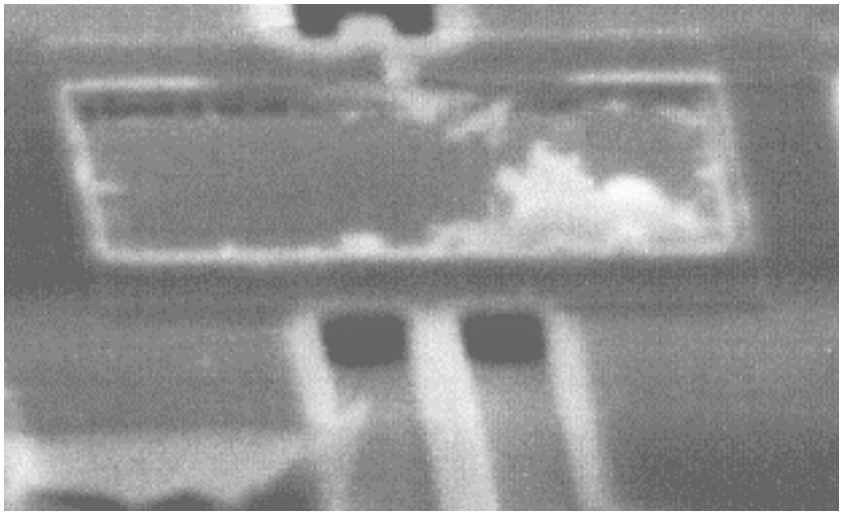


Fig. 3.11 - Pad metallization damage caused by bromide based etchant.

3.3.3 Suspended Metal / Intermetallic Layer Structure

3.3.3.1 Structure description

The third proposed micromachined structure consists of suspending only metal and intermetallic materials by removing completely the GaAs bulk material underneath the structure, as illustrated in Fig. 3.2f. The principal application of this kind of structure is, e.g., to create suspended microwave passive devices with low losses at high-frequency, discussed in detail in Chapter 5.

3.3.3.2 Etching solutions

Since no constraints on selective and preferential etching are to be considered, and the pad metallization and passivation layers are not damaged during the post-process wet etching, which is the basic condition for this front-side bulk micromachinig approach, the analysis and experimental results presented above can be used in this case. That is, the **citric acid** selective solution, as well as **H_3PO_4** and **NH_4OH** anisotropic based etchants are certainly suitable for such kind of structure. Moreover, commonly in this case the undercutting is much more important than the etching depth, when the goal is just to create a tiny air gap layer between the metal wires and the GaAs substrate, and whose height is not so critical.

3.4 GENERAL CONSIDERATIONS

Electronic circuitry compatibility is one of the most attractive features of this maskless front-side bulk micromachining approach, and then it should always be certificated after each chemical etching treatment. Once preliminary experiments have proven the feasibility of suspended microstructures in a particular microelectronics process, and related potential applications are identified and justify additional efforts and investments, a much more careful and detailed characterization work should be done in terms of etching kinetics and material properties.

3.4.1 Electronic Verification

The influence of the post-process wet chemical etching procedure on the electronic circuitry, in particular the active devices (diodes and HEMTs), where carefully verified, considering the validated citric acid (5:1 vol.), H_3PO_4 (1:13.8:13.2 vol.) and NH_4OH (20:7:973 vol.) based solutions. The passivation layer and the pad metallization were visually verified using optical microscope. The pad contacts were also validated by using microprobes to transmit an electrical signal.

3.4.2 Etching Characterization

Usually, in order to obtain detailed data on the crystal orientation dependence of the etch rate, a fan shaped or wagon wheel shaped masking pattern is employed, consisting of radially divergent segments with angular separation of few degrees (between 1 to 3), as shown in Fig. 3.12 [12][38]-[40]. Since the mask is realized using optically transparent layers, such as silicon dioxide or silicon nitride, after etching a blossom-like figure is visually observed on the chip surface. This phenomenon is due to the radial extension of the exposed center area, which depends on the crystal orientation of the individual segments, leading to a different amount of lateral underetching.

Moreover, other test mask shapes, such as circles and rotated rectangles are very helpful to provide complementary etch rate information. However, note that commonly only shape edges in orthogonal orientation or angles multiple of 45° are allowed by microelectronics foundries.

On the other hand, as discussed below, the verification of the vertical profiles of etched regions is very important to certain micromachined structures. However, to cut or cleave dies for this purpose represents a somewhat difficult task, mainly when just small and tiny circuits are available, like in PML HEMT process, for which the maximum chip dimensions of 2 x 3 mm^2 (100 μm-thick substrate) are accepted by CMP for prototyping.

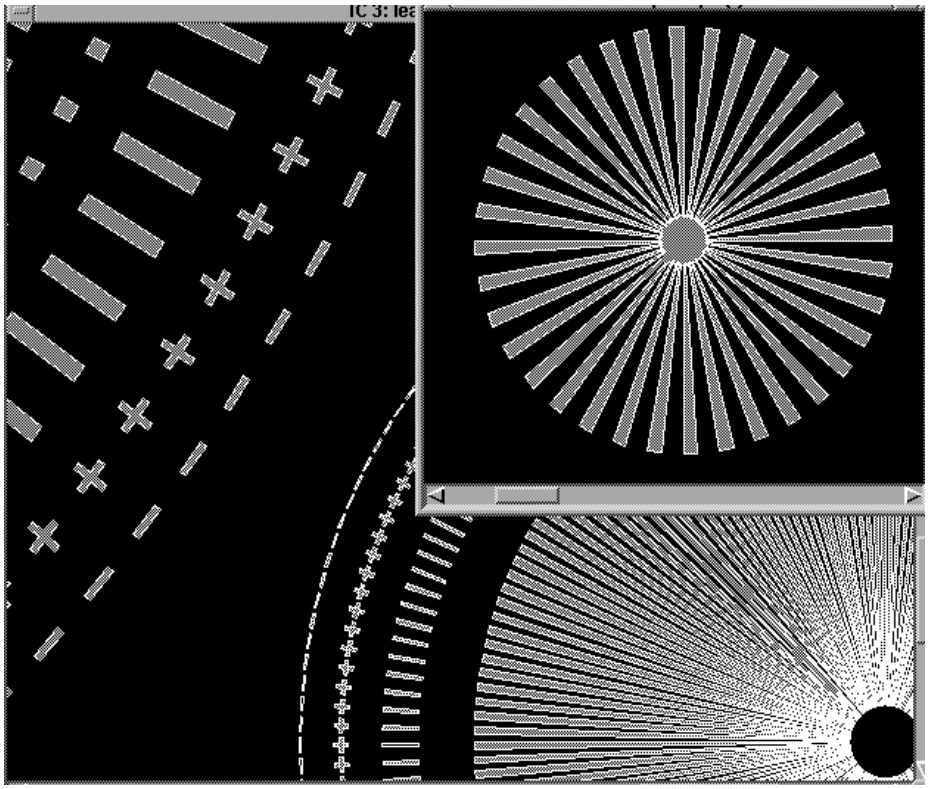


Fig. 3.12 - Wagon wheel shaped masking pattern for etching characterization.

In summary, micromachining prototypes fabricated in standard IC processes are not appropriate to realize a more complete and accurate investigation about the etching behavior. For example, from the etch rate results presented before, it is observed that such rates for depth and <001> surface orientations are slightly different, which can be due to the mask border influence, etchant saturation at particular regions or imprecision of measurements. Thus, it is suggested to use special masking shapes for etching evaluation at wafer level. The cleavage procedure for vertical profile analysis can be replaced by extracting the respective 2D etch rate diagram from the substrate surface plane using wafers with [110] and [$1\bar{1}$ 0] orientations, or equivalent. But, in this case, small

differences in the wafer and IC die properties as well as the influence of mask dimensions and original layers thickness should not be forgotten.

Finally, the selectivity of GaAs to AlGaAs layers provided by some etchants cannot be measured using IC prototypes. Particular epitaxial layers grown in GaAs substrate should be considered for such a kind of evaluation.

3.4.3 Mechanical and Thermal Properties

Released microstructures have been found to be mechanically very robust and no damage was observed when they supported impacts during transportation and eventual packaging or manipulation procedures. Long and straight cantilevers as well as spiral structures formed by dielectric layers were successfully built, as illustrated in Fig. 3.13. It is obvious that a characterization work about the mechanical and thermal properties must be realized in future works for the related layers present in specific targeted processes, in order to obtain the respective fracture toughness, Young' modulus, thermal resistivity, Seebeck coefficients, and so on.

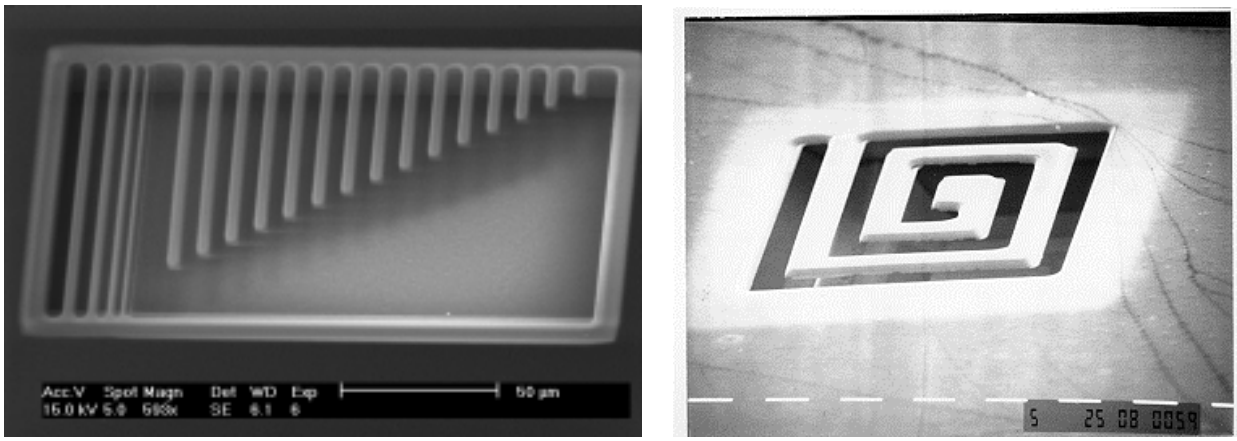


Fig. 3.13 - Suspended metal / intermetallic layer structures : bridges and cantilevers.

3.5 CONCLUSIONS

This micromachining characterization aimed at verifying the feasibility of the maskless post-process wet etching using the GaAs technologies available through the CMP service. The PML HEMT D02AH presented excellent results in terms of dielectric openings (open areas) and etching procedure, while in the Vitesse MESFET H-GaAs III process the problem caused by residual layers has not been solved yet. Therefore, etching solutions for the different structures proposed were characterized according to the selective and preferential properties. Although general conclusions resulted from this work can be extended to other GaAs technologies, it seems

clear that particular effects and phenomena in the etching kinetics are specific to each IC process. Finally, once the use of certain microelectronics processes has been validated, and potential applications justify greater effort in the characterization task, a more complete work should be done towards the generation of the 3D etch rate polar diagram and the extraction of mechanical and thermal properties of IC layers.

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Chapter 4
GaAs THERMAL BASED DEVICES

GaAs based semiconductors are attractive materials for thermal sensors because of the transistor operation at high temperatures (resulting from the large bandgap), low thermal conductivity, high Seebeck coefficient and, of course, electronic compatibility. First, thermally isolated electronic devices placed over triangular prism-shaped bridges are presented as a promising possibility for bolometers, RMS converters and temperature regulated analog circuits. Next, the feasibility and usefulness of GaAs-TiAu thermocouples using the PML D02AH process are extensively evaluated through analytical formulations, electrical circuit models and FEM simulations. Two potential applications were particularly studied. They are the infrared detector and the electro-thermal converter. This converter device can be efficiently used as a microwave power sensor in monolithic microwave integrated circuit design. On the other hand, the absence of a sensitive area (black layer) in the proposed thermopile structures resulted in low performance of infrared sensors. Thermocouple structures have been successfully fabricated and experimental measurements are in progress.

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4.1 INTRODUCTION

Temperature is a fundamental parameter in many processes and it may need to be measured, compensated for, or even controlled in some manner. Not only temperature is often measured in plant, automobiles, household appliances, medicine and environment, but it is also exploited as a secondary sensing variable in non-thermal microsensors, such as gas or mechanical wind flow sensors. Temperature sensors are also used to compensate the errors caused by the temperature variation of components or instruments, or form part of a control circuit. Therefore, such a device represents perhaps the largest and most important class of microsensors today.

In this work, the term *thermal sensor* is used to mean any device that will yield an electrical output signal but has an input or intermediate signal of a thermal type. Thus, basically, three kinds of thermal sensors can be distinguished : the sensors which directly convert a temperature or a temperature difference into an electrical signal; the sensors in which a non-thermal signal is first transduced into a thermal signal and then transduced into an electrical signal by a temperature (difference) sensor; and thermal based devices which are not really sensors at all, but AC-DC or RMS (root mean square) converters which measure electrical voltages and currents by measuring the thermal power developed by these signals [1].

In thermal sensors, in which the thermal signal (temperature or temperature differences) is induced in the device by contact or by a physical effect, such as infrared radiation or cooling by an air flow, the influence of other physical effects has to be as low as possible, like those caused by heat leakage along the connecting and supporting material. Using micromachining techniques, it is possible to fabricate free-standing regions that are thermally isolated from the bulk material, allowing the realization of efficient thermal based micro-devices.

GaAs based semiconductors are attractive materials for thermal sensors because operation at ambient temperatures up to 350°C is possible, as a result of the large bandgap, and integration into electronic circuits can be achieved [2][3]. Moreover, as discussed in previous chapters, GaAs micromachining techniques are simple and interesting because of the preferential etching behavior observed with certain etchants and the selective etching available using III-V materials.

In this chapter, these facilities are considered to present potential GaAs thermal devices through the use of suspended electronic components and micromachined thermopiles. The higher thermal resistivity and higher Seebeck coefficient than silicon make it a very promising material for such a kind of applications, for example, the microwave power sensor that is very useful for the

PML HEMT MMIC technology [4].

4.2 SUSPENDED ELECTRONIC DEVICES

4.2.1 Suspended Resistor

The most straightforward GaAs thermal device allowed with this micromachining approach consists of the creation of a suspended metal or semiconductor resistor. As discussed in Chapter 3, a free-standing GaAs resistor can be released either through selective etching using AlGaAs as stop layer or over the triangular prism-shaped bridge, respecting all parameters such as selectivity and undercutting associated with them (see Fig. 3.6b). On the other hand, the metal resistor (TiAu in PML), which is more easily suspended due to the absence of constraints related to the selective and preferential etching, is not really useful because of its low resistance value. Standard (non-etched) and suspended GaAs resistors were measured and compared to verify the differences in the rise temperature, which is observed by an increasing resistance value, resulting from Joule heating as seen in Fig. 4.1.

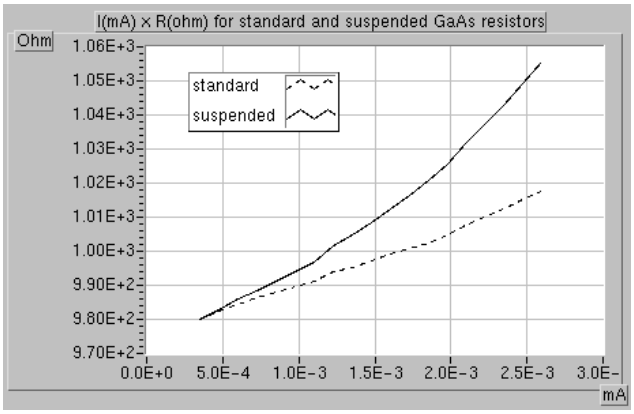


Fig. 4.1 - Graph IxR for standard and suspended GaAs resistors (R ≅ 1KΩ).

In terms of target applications based on suspended resistors, a great number of interesting sensing devices can be listed, such as bolometers, Pirani vacuum sensors, pressure sensors, anemometers and gas-sensing elements [5]-[7]. In these applications, because of the required biasing to measure the resistance value, often two identical resistors are used in a Wheatstone-bridge configuration, one acting as the sensor element and the other as the reference. However, although they can be advantageously used outside the temperature range accepted by other thermal devices, commonly the stress dependence, voltage dependence and their wide tolerances make resistors less attractive.

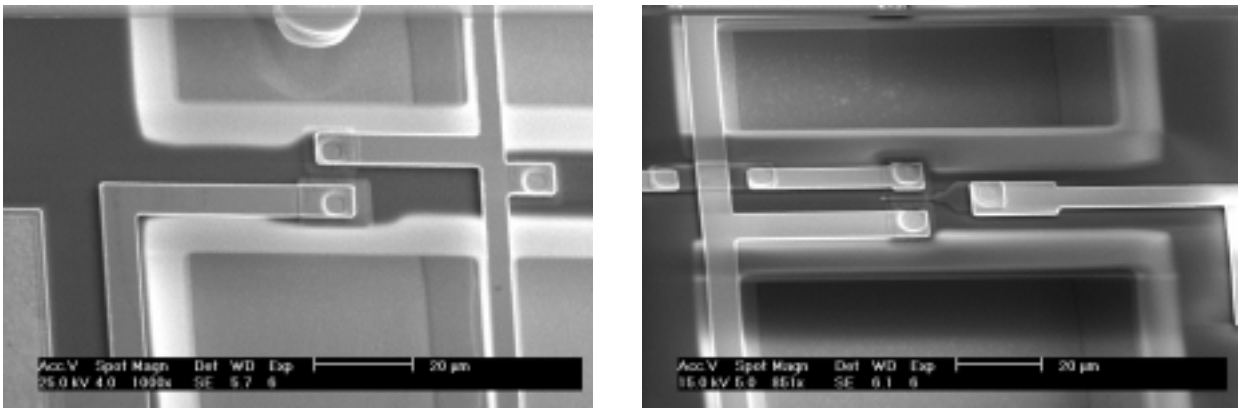
Furthermore, suspended metal resistor is very useful to act as a heater unit in thermopile based applications, while a GaAs resistor represents a part of the proposed GaAs-TiAu

thermocouple structure, discussed later.

4.2.2 Suspended Active Devices

Much more interesting than to create free-standing resistors is the possibility of suspending electronic active devices (diodes and transistors) by using the triangular prism-shaped bridge. Since the active areas of such components are kept intact inside the inverse triangular GaAs mass, they can be efficiently thermally isolated, allowing a wide range of applications. The use of suspended active devices as thermal sensors has been proposed by Klaassen et al. [8] in standard silicon based IC technology by using a new and unconventional post-process etching. Two applications were targeted and discussed in [8] : an RMS converter, where a suspended resistor is used as the heater and a diode is used under forward bias as a temperature sensor, and a temperature regulated analog circuit, where the suspended active device is used to mitigate the effects of ambient temperature changes on precision circuitry such as a bandgap voltage reference. Suspended MESFETs and Schottky diodes have also been proposed by Pogany et al. [9] to study the temperature distribution and thermal time response in GaAs micromachined power sensors.

Fig. 4.2 shows active devices placed over triangular-shaped bridges, fabricated in the PML HEMT D02AH process. Both Schottky diode and HEMT were characterized before and after micromachining, and proven to be fully functional.



(a) (b)

Fig. 4.2 - Active devices over triangular prism-shaped bridges: (a) Schottky diode and (b) HEMT.

4.3 GaAs THERMOCOUPLES

Thermocouples have various attractive properties compared to other sensors which are frequently used for temperature difference measurements, such as the transistor pair and the resistance bridge. First, the thermocouple is based on the self-generating Seebeck effect, in which

the input signal supplies the power for the output signal. This ensures that :

- the thermocouple has an output signal without offset and offset drift, because there cannot be any output signal without input power;
- the thermocouple does not suffer from interference from any physical or chemical signals except light, which can easily be shielded, because the Seebeck effect and the photoelectric effect are the only two self-generating effects in semiconductors;
- the thermocouple does not need any biasing;
- the read-out is very simple, only a voltmeter is required;
- there is no interference caused by power supplies.

In addition, the sensitivity of the thermocouples is almost not influenced by variations in the electrical parameters across the wafer or by the temperature, while in transistor and resistor based sensors, both the sensitivity and the offset usually depend on the position on the wafer and on the temperature.

4.3.1 Thermoelectric Effects

Initially, the thermoelectric effects in metal and semiconductors related to such a kind of structure are briefly reviewed. The Joule effect is not treated herein.

a) Seebeck Effect

When two different materials are joined together at one point and a temperature difference is maintained between the joined and non-joined parts of the materials, an open-circuit voltage develops between the non-joined parts of this thermocouple (see Fig. 4.3a). The resulting voltage ΔV is proportional to the temperature difference (ΔT) between hot and cold junctions, and to the Seebeck coefficient of the thermocouple materials a and b ($\alpha_{ab} = \alpha_a - \alpha_b$) :

$$\Delta V = \alpha_{ab} \, . \, \Delta T \tag{4.1}$$

The Seebeck coefficient (α) of a material can be expressed in terms of the Fermi level (E_F) and the charge carriers (q), which are dependent of temperature variations :

$$\alpha \, . \, q \, . \, \nabla T = \nabla E_F \tag{4.2}$$

In practice, it may be approximated for the range of interest used in sensors and at room temperature as a function of electrical resistivity (ρ) :

$$\alpha = m \, . \, k \, . \, \ln(\rho/\rho_o) \, / \, q \tag{4.3}$$

where $\rho_o = 5x10^{-6}\ \Omega m$, $m \approx 2.5$, and k is the Boltzman constant [1].

b) Peltier Effect

Apart from the Seebeck effect, the Peltier effect represents another important thermoelectric offset. It corresponds to heat absorption from or release to the ambient, when an electrical current flows through the junction of two different materials [1][10] :

$$Q_{ab} = - \Pi_{ab} . I_{ab} \qquad (4.4)$$

with Q_{ab} as the heat absorbed from the ambient, I_{ab} as the current flowing through the junction from material a to material b, and Π_{ab} as the Peltier coefficient for a junction of these materials.

Such effect is reversible, since heat is absorbed or released depending on the direction of the current, and it must be taken into account in thermal device design using a heating resistor because it may give rise to considerable asymmetries. The Peltier coefficient (Π_{ab}), in Volts, quantifies the ratio of heat absorption to electrical current and is equal to the Seebeck coefficient multiplied by the absolute temperature (T), called the first Kelvin relation :

$$\Pi_{ab} = \alpha_{ab} . T \qquad (4.5)$$

c) Thomson Effect

An electric current (I) flowing in a temperature gradient (∇T) absorbs heat from or releases heat to the ambient [1][10] :

$$Q_{th} = \gamma_{th} . I . \nabla T \qquad (4.6)$$

where γ_{th} is the Thomson coefficient, that is closely related to the Seebeck coefficient according to the second Kelvin relation :

$$\gamma_{th} = T . (\partial\alpha / \partial T) \qquad (4.7)$$

The Thomson effect is useful for determining the absolute Seebeck coefficient of lead (Pb), which serves as a reference for all materials at temperatures up to room temperature, because it has a low Seebeck coefficient and can be measured accurately as a function of temperature.

4.3.2 Micromachined Structures

In order to increase the self-generated Seebeck voltage, thermocouples are usually

connected in series configuration, given a total thermopile voltage equal to the unitary thermocouple voltage multiplied by the number of series thermocouples. Moreover, in micro-thermopiles implemented over semiconductor substrates, the sensitivity of such devices is significantly improved by removing the bulk material underneath the hot junctions, in order to increase the thermal resistance associated (see Fig. 4.3b) [11].

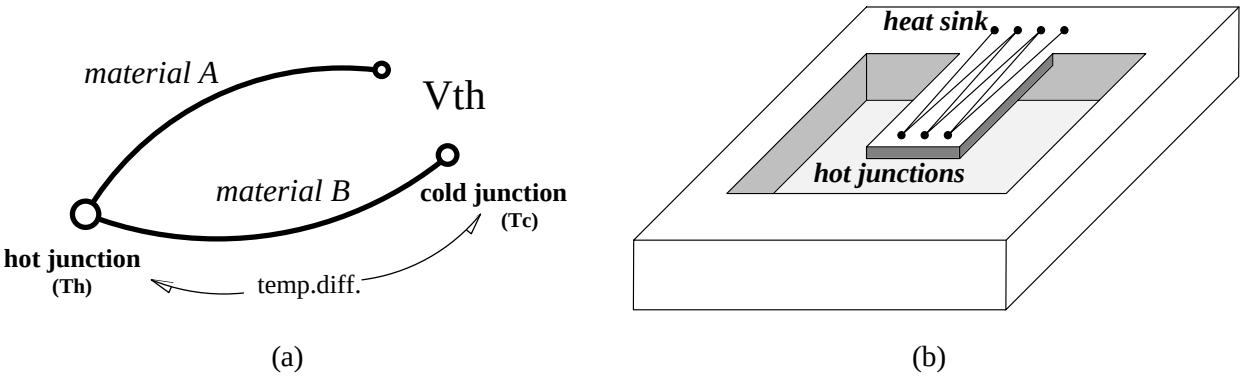


Fig. 4.3 - Seebeck based devices: (a) thermocouple structure and (b) micromachined thermopile.

Since semiconductors exhibit a large Seebeck coefficient, a great effort has been done to realize on-chip thermopile based sensors using micromachined structures, where the hot junctions are placed at the most isolated portions of free-standing structures, and the cold junctions over the non-etched substrate region, which acts as heat sink. Several examples have been presented in silicon technologies, by using membranes, cantilevers and bridges [12]-[16]. Investigations have also been developed considering GaAs processes in order to take the advantage of high thermal resistance and high Seebeck coefficient from GaAs material [17]-[21].

In comparison to silicon, GaAs presents approximately twice the thermal resistivity value. Such parameter is possible to be increased even more, up to 10 times that of silicon, if III-V ternary alloys are available. Therefore, the hot regions and eventual heater devices, as used in flow sensors and AC-DC converters, can be efficiently isolated, resulting in a lower power consumption and higher sensitivity. Furthermore, the Seebeck coefficient of $Al_xGa_{1-x}As$ can vary from 300 to 700 µV/K by changing the p- or n-type carrier density and the aluminum mole fraction $\underline{x}$ [19][22]. On the other hand, the electrical resistivity which contributes to the noise parameter in the device performance is slightly higher than that of silicon.

a) Figure of Merit

In order to compare different thermoelectric materials, figure of merit for each material (Z) is commonly considered [10][14][23] :

$$Z = \alpha^2 / (\rho.\kappa) \quad (4.8)$$

where α is the Seebeck coefficient, ρ the electrical resistivity and κ the thermal conductivity of the respective material. For optimal signal-to-noise ratio, the figure of merit of a thermocouple (Z_{ab}), composed by the materials a and b, has to be maximized. This is defined as :

$$Z_{ab} = (\alpha_a - \alpha_b)^2 / ((\rho_a.\kappa_a)^{1/2} + (\rho_b.\kappa_b)^{1/2})^2 \quad (4.9)$$

A comparison between some thin-films and microelectronics compatible materials, summarized in Table 4.1, shows that, although GaAs presents a high Seebeck coefficient and relatively low thermal conductivity, the elevate electrical resistivity value reduces significantly its figure of merit. On the other hand, AlGaAs layer could be significantly improved for thermocouple structure during the fabrication. Nevertheless, note that the Seebeck coefficient and electrical resistivity parameters used to estimate such comparative value can vary strongly with dopand type and carrier density. Moreover, the layer thickness which contributes significantly to the thermal conductivity is not taken into account in the estimation of this figure of merit.

TABLE 4.1 - Seebeck coefficient, electrical resistivity, thermal conductivity and figure of merit of some thin-films and microelectronics compatible materials.

Material	Seebeck coefficient α (μV/K)	Electrical resistivity ρ ($\mu\Omega$.m)	Thermal conductivity κ (W/(K.m))	Figure of merit Z (10^{-6}/K)
GaAs (n=10^{17}cm^{-3})	-300	150	44.1	13.6
$Al_{0.15}Ga_{0.85}As$ (n=10^{17}cm^{-3})	-350	180	16.9	40.3
$Al_{0.45}Ga_{0.55}As$ (n=10^{17}cm^{-3})	-670	130	10.9	317
Si	± 100-1000	35	144	40
PolySi (n=3.10^{19}cm^{-3})	-121	8.9	29.4	56
n-Poly AMS	-65	8	≈ 29	17.9
p-Poly AMS	135	55	≈ 29	12.1
Au	0.1	0.023	314	0.0014
Al	-3.2	0.028	238	1.53
Sb	48.9	0.42	24.0	237
Sb_2Te_3	130	5	2.8	1200
$Bi_{0.87}Sb_{0.13}$ (n)	-100	7.1	3.1	454
$Bi_{0.5}Sb_{1.5}Te_3$ (p=3.10^{19}cm^{-3})	230	17	1.05	2963
CuNi	-35.1	0.52	19.5	121

Obs.: Values obtained from [10][14][16][19][23].

b) PML GaAs-TiAu Thermocouples

In the case of PML HEMT process, the thermocouple structure can be created with the GaAs doped layer (used for resistor) and the interconnection metal TiAu. In fact, the titanium is

used with gold for layer adherence, but it represents less than 10% of the TiAu composition, allowing the use of Au characteristics as a good approximation for this study. The GaAs doped layer presents a very small thickness equal to 0.05 µm and an electrical resistivity around to 19.5 µΩ.m. With the α and κ values given in Table 4.1, the figure of merit of a GaAs layer is estimated to be equal to 104.6×10^{-6}/K. However, Z of gold is very low due to its almost zero Seebeck coefficient. As a consequence, Z_{ab} for the GaAs-TiAu thermocouple is approximately 87.8×10^{-6}/K.

To build the GaAs-TiAu thermocouple over a free-standing structure, both selective and preferential etching approaches are suitable:

- In the first case, the suspended GaAs/AlGaAs mesa structure is limited by the selectivity of the etchant. As discussed before, cantilevers with the maximum width of approximately 10 µm can be created using a selectivity of 100. Therefore, respecting the minimum dimensions given in the electronic design rules from PML, and illustrated in Fig. 4.4, only one thermocouple can be placed over the structure.

- In the second case, the GaAs doped layer can be kept over a triangular prism-shaped bridge, as presented for the suspended resistor. However, the bulk material included in the structure contributes to the heat dissipation, reducing the temperature in the hot junctions and, consequently, the efficiency of the structure. On the other hand, like in the first approach, only one thermocouple with minimum width dimensions is placed over the cantilever (or two in symmetrical configuration on a bridge). Note that, an undercutting rate of about four times lower than the etching depth rate results in larger dielectric borders.

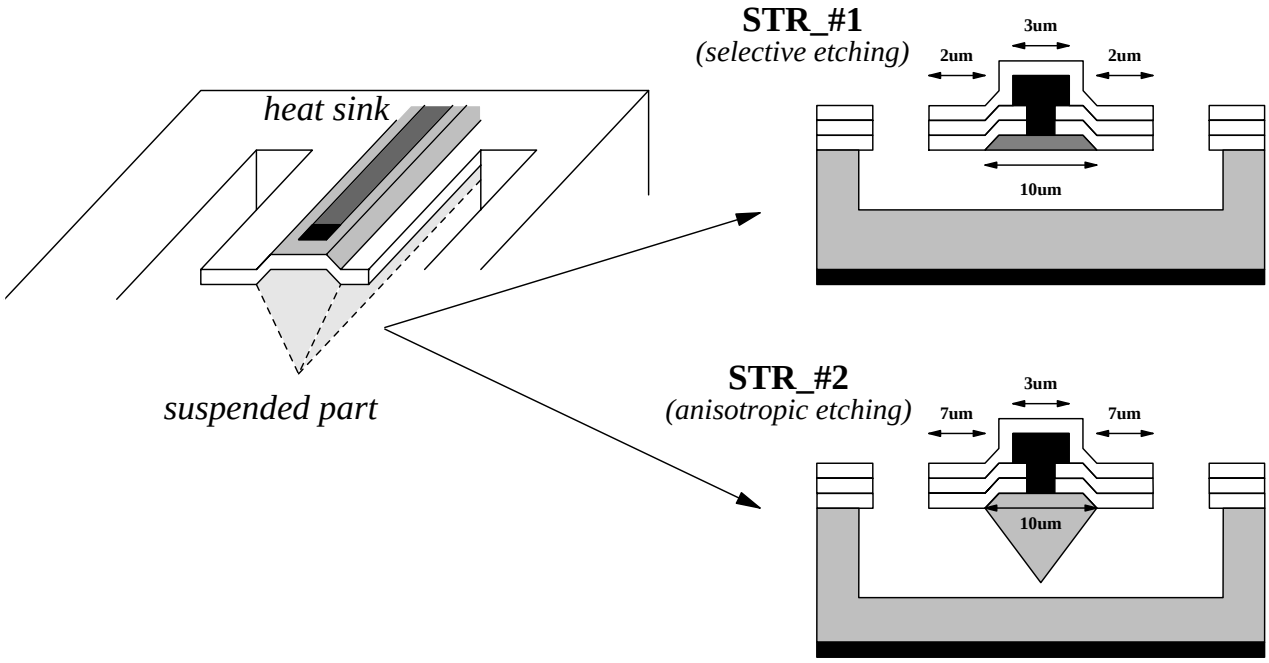


Fig. 4.4 - Micromachined GaAs-TiAu thermocouple in PML HEMT process.

4.3.3 Analytical Modeling

Although the optimization of the design of thermocouples can be carried out, in principle, by three-dimensional modeling of the temperature distribution on the structure, in many cases it is sufficient (and less costly) to analyze such devices in terms of one-dimensional model, ignoring consequently temperature distributions in the thickness dimension.

Initially, two different incoming powers can be considered : a heat load applied at the boundary opposite the heat sink (**N_B**) and a power homogeneously applied at the surface of the structure (**N_S**). Both can be generated directly ($N^{(d)}$), e.g., by internal electrical heating, or as a consequence of irradiation ($N^{(r)}$) of the structure with an irradiance Φ :

$$N = N^{(d)} + N^{(r)} \tag{4.10}$$

and

$$N^{(r)} = A_{\Phi}.\varepsilon.\Phi \tag{4.11}$$

where A_{Φ} is the irradiated area, and ε is the emissivity of this surface.

Since, in practice, a sensitive area (A_B) is placed at the end of the structure, the power N_B is reduced by the surface conductance of that area (G_A), discussed below. In this case, the **heat flow (Q_B)** transferred to the structure at the boundary is :

$$Q_B = N_B - G_A.(\Delta T_B - \Delta T_e) \quad (4.12)$$

with $\bullet T_B = T_B - T_o$, that is, the temperature difference between the boundary of the structure (T_B) and the heat sink (T_o), and $\Delta T_e = T_e - T_o$, where T_e represents the temperature of the environment.

The power N_S, in turn, is evaluated through the parameter *I*, which has the dimension of temperature and is not dependent of $\underline{x}$ (structure position in longitudinal direction). It is defined as :

$$I = \Delta T_e + T_N \quad (4.13)$$

with

$$T_N = N_S / G_S \quad (4.14)$$

where G_S represents the surface conductance of the structure.

The **temperature distribution** $\Delta T(x)$ on a bridge can be obtained from the stationary one-dimensional heat-transport equation (Fourier's equation), with the appropriate boundary conditions, i.e., the temperature in the heat sink (at x=0) is equal to T_o, and at the end of the structure (at x=l) is T_B [24]-[26] :

$$\partial^2\Delta T(x)/\partial x^2 - \beta^2[\Delta T(x) - I] = 0 \quad (4.15)$$

where

$$\Delta T(x) = T(x) - T_o \quad (4.16)$$

and

$$\beta = (G_S/G_L)^{1/2} / l \quad (4.17a)$$

or better

$$\beta.l = (G_S/G_L)^{1/2} \quad (4.17b)$$

As mentioned, G_S corresponds to the **surface conductance** resulted from the heat transfer between the top/bottom sides of the suspended structure and the environment, and it is calculated taking into account losses by convection and radiation. Note that, the linearization of radiant heat transfer is applicable only if the temperature difference between the structure and the environment is insignificant when compared to the absolute environment temperature :

$$G_S = G_{SR} + G_{SC} = A.[4\sigma(\varepsilon_1 + \varepsilon_2)T_o^3 + \gamma] \quad (4.18)$$

where σ is the Stefan-Boltzmann constant, ε_1 and ε_2 are the **emissivities** of both sides of the suspended structure with area $\underline{A}$, and γ represents the heat-transfer coefficient for convective dissipation. Such **convection heat-transfer coefficient** (γ) depends on the properties of the surrounding media (gas, fluid, pressure, velocity, and so on) and the free or forced convection conditions. For a quiet gas environment in a small package it could be estimated using [27] :

$$\gamma = \kappa_g \, (d_1^{-1} + d_2^{-1}) \qquad (4.19)$$

where κ_g denotes the thermal conductivity of the gas atmosphere (equal to 0 in vacuum), d_1 is the distance between the back side of the structure and the bottom of the etched hole, and d_2 is the distance between the structure surface and package cap. Such coefficient (γ) usually prevails over the radiation one given by $4\sigma(\varepsilon_1 + \varepsilon_2)T_o^3$. The surface conductance G_A, discussed above, is calculated similarly to G_S, but, in this case, considering the sensitive area A_B.

On the other hand, G_L represents the thermal conductance associated with the **inplane conductivity** of the free-standing structure formed by one or more layers :

$$G_L = (w / l).\kappa.d \qquad (4.20)$$

where w and l are the width and length of the structure, respectively, and the **average thermal conductivity** (κ) is defined by :

$$\kappa.d = \Sigma \, \kappa_i.d_{i\text{-}eff} \qquad (4.21)$$

where κ_i corresponds to the thermal conductivity of individual layers comprising the structure stack (metallization, oxide/nitride support, insulating and passivating layers, suspended bulk material) with respective effective thickness $d_{i\text{-}eff}$. The effective thickness takes into account a factor representing the degree of coverage of the structure by a layer :

$$d_{i\text{-}eff} = n_i.(w_i / w).d_i \qquad (4.22)$$

with w_i and d_i equal to the width and thickness of layer i placed n_i times on the suspended structure. Note that, for a layer that covers uniformly all the structure width, such factor becomes one.

Finally, the solution of the stationary one-dimensional heat-transport equation is given by the following expression [24] :

$$\Delta T_B = \{N_B + G_A T_e + I.[G_L.G_S]^{1/2}[\coth(\beta.l) - \sinh(\beta.l)^{-1}]\} / \{G_A + [G_L G_S]^{1/2}.\coth(\beta.l)\} \qquad (4.23)$$

and the total thermal resistance of the structure is obtained by dividing the temperature difference by the total incoming power N_B and/or N_S :

$$R_T = \Delta T_B / N_{B,S} \qquad (4.24)$$

In order to apply these equations herein, the GaAs structures proposed were numbered, that is, str_#1 corresponds to the suspended GaAs/AlGaAs mesa structure, and str_#2 is the triangular

prism-shaped bridge, as was shown in Fig. 4.4. Moreover, only one thermocouple is considered on a cantilever with the minimum cross section dimensions. Initially, the average thermal conductivity is calculated according to the values presented in Table 4.2.

TABLE 4.2 - GaAs-TiAu thermocouple layers characteristics (PML D02AH process).

Layer	w(μm)	d(μm)	d_{eff}(μm)	κ(W/m.K)
Si_3N_4	w_{cant}*	0.15	0.15	19
TiAu	3	1.25	3.75 / w_{cant}	314
SiO_2	w_{cant}*	0.85	0.85	1.4
GaAs doped	10	0.05	0.5 / w_{cant}	44.1
$Al_{0.25}Ga_{0.75}As$	10	0.05	0.5 / w_{cant}	13.15

*w_{cant} is the cantilever width, i.e., equal to 14μm for str_#1 and 24μm for str_#2.

Note that, the effective thickness of the GaAs bulk material present in the triangular-shaped bridge is equal to 5.65 μm and was obtained converting the triangular shape to a rectangular one with equivalent cross section area and width equal to the total cantilever width. Furthermore, InGaAs was not taken into account because in the str_#1 structure it is removed, while in the str_#2 its thickness can be neglected with respect to the suspended bridge mass. Thus :

- str_#1 $\Rightarrow$ $\kappa.d = 90.2$ μW/K
- str_#2 $\Rightarrow$ $\kappa.d = 299.5$ μW/K

Next, the inplane conductance (G_L) is then given as a function of the cantilever length (l), in microns :

- str_#1 $\Rightarrow$ $G_L(l) = 1262.8 / l$ μW/K
- str_#2 $\Rightarrow$ $G_L(l) = 7188.0 / l$ μW/K

To calculate the surface conductance (G_S), T_o was considered equal to 300K, the average emissivity for both top and bottom sides equals to 0.5, and the convection heat-transfer coefficient (γ) equals to 508.3 W/m^2.K, for $\kappa_g = 25 \times 10^{-3}$ W/m.K, $d_1 = 50$ μm and $d_2 = 3$ mm. The surface area (A) is somewhat different for the two kinds of structures because of the bulk mass underneath the triangular bridge :

- str_#1 $\Rightarrow$ $A(l) \approx 30 \times l$ μm^2 and $G_S(l) = 7.72 \times 10^{-12} \times l$ W/K
- str_#2 $\Rightarrow$ $A(l) \approx 98 \times l$ μm^2 and $G_S(l) = 25.21 \times 10^{-12} \times l$ W/K

As a result, the factor β.l, as a function of the length (μm), for each structure is :

- str_#1 $\Rightarrow$ $\beta.l\,(l) = 78.2 \times 10^{-6} \times l$
- str_#2 $\Rightarrow$ $\beta.l\,(l) = 59.2 \times 10^{-6} \times l$

Finally, assuming that the environment temperature equals the heat sink temperature ($T_e = T_o$), if only a direct incoming power of 1 mW is applied at the end of cantilever (N_B), that is, no homogeneous power is distributed on the surface structure ($N_S = 0$), then the parameter *I* is not used, and because of the absence of sensitive area G_A is zero. Thus, the temperature at the boundary (hot region), as a function of structure length, is calculated using :

$$\Delta T_B(l) = N_B / [G_L(l).G_S(l)]^{1/2}.\coth(\beta.l(l)) \qquad (4.25)$$

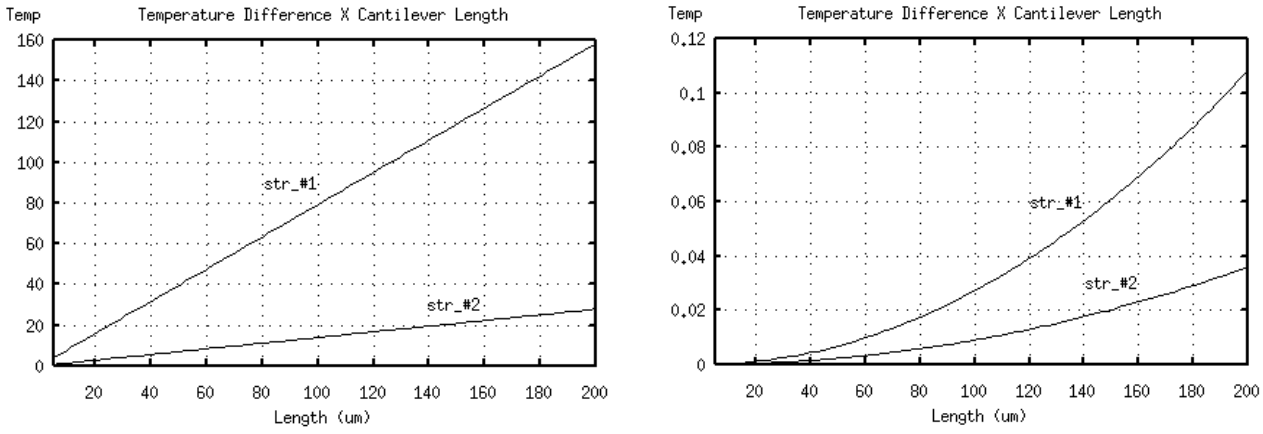
In the second case, if only an homogeneous irradiation with $\Phi = 1000\ W/m^2$ is applied to the whole cantilever top surface, N_S is calculated for the respective irradiated area and surface emissivity, knowing that the gold emissivity is equal to 0.09 and the Si_3N_4/SiO_2 one is approximately 0.6 :

- str_#1 $\Rightarrow$ $N_S(l) = 6.83x10^{-9}\ x\ l$ W
- str_#2 $\Rightarrow$ $N_S(l) = 12.87x10^{-9}\ x\ l$ W

The parameter *I* is also a function of the structure length (μm), that is, $I(l) = N_S(l) / G_S(l)$, and G_A is kept equal to 0 (absence of sensitive area). Now, the temperature equation becomes :

$$\Delta T_B(l) = \{I(l).[G_L(l)G_S(l)]^{1/2}[\coth(\beta.l(l)) - \sinh(\beta.l(l))^{-1}]\} / \{[G_L(l)G_S(l)]^{1/2}.\coth(\beta.l(l))\} \qquad (4.26)$$

Fig. 4.5 shows the behavior of the temperature difference as a function of the structure length for both cases and both kinds of structures. As expected, it was observed that the triangular-shaped bridge is less efficient because of the additional bulk mass that contributes to the heat dissipation. Moreover, in the case of the homogeneous irradiation the absence of a sensitive area results in a very low increase in temperature.



(a) (b)

Fig. 4.5 - Temperature difference as a function of cantilever length: (a) only incoming power at the end of the structure and (b) only irradiated power homogeneously distributed.

4.4 THERMOPILE BASED DEVICES

The performace of thermopile based devices is generally evaluated and optimized through their self-generated Seebeck voltage, sensitivity, detectivity and time constant characteristics, which can be obtained analytically taken into account the formulations presented above. For thermal radiation sensors or AC-DC power sensors, this optimization yields the optimal Volt per Watt or signal-to-noise ratios, while for other sensor principles (e.g., flow or vacuum/pressure sensors) it yields the best ratios of thermoelectric voltage and power supply.

4.4.1 Performance Characteristics

At first, the **thermoelectric voltage** (V_{th}) generated in a device with n thermocouples is given by :

$$V_{th} = n.\alpha_{ab}.\Delta T_B \tag{4.27}$$

with α_{ab} denoting the Seebeck coefficient of the thermoelectric junction, and ΔT_B corresponds to the temperature difference between the hot and cold junctions, as presented before.

On the other hand, the **sensitivity** (S) of the device is given by the ratio of the thermoelectric voltage and the incoming heating power ($N_{B,S}$), and can also be expressed as a function of the thermal resistance :

$$S = V_{th} / N_{B,S} = n.\alpha_{ab}.R_T \tag{4.28}$$

The **detectivity** (D*), in turn, is related to the sensitive area (A_Φ) commonly used in infrared detectors and represents the reciprocal of the NEP (noise equivalent power) per unit frequency (Δf) :

$$D^* = (A_\Phi.\Delta f)^{1/2} / NEP \tag{4.29a}$$

and for Δf = 1 Hz, and assuming that only thermal noise, $(4.k.T.R_{el})^{1/2}$, is present in the thermopile structure, then it can be expressed in terms of the sensitivity characteristic (S) :

$$D^* = S\,[A_\Phi / (4.k.T.R_{el})]^{1/2} \tag{4.29b}$$

where R_{el} corresponds to the electrical resistance of the thermopile, T is the absolute temperature and *k* is the Boltzmann constant. It is given in $Hz^{1/2}$.m/W.

Finally, the thermal **time constant** (τ) is calculated through the thermal resistance (R_T) and capacitance (C_T) of the whole suspended structure :

$$\tau = R_T.C_T \tag{4.30}$$

where C_T, given in J/K, can be estimated as the simple sum of the thermal capacitances of individual layers (i), as following :

$$C_T = \sum_i C_i = \sum_i density_i \cdot volume_i \cdot heat\_capacity_i \tag{4.31}$$

For more precision, it can be weighted by the mean temperature difference to the sink, as presented in [24]. Note that, the minimization of τ implies a reduction of the thermal resistance which will also reduce the sensitivity. This is an important trade-off depending on the application.

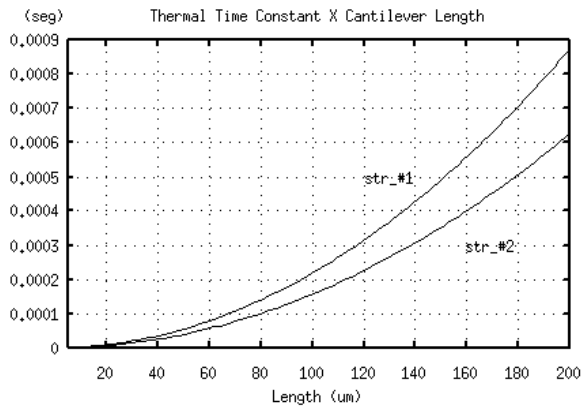
For both GaAs structures proposed, the thermal capacitances were calculated as a function of the structure length (in microns) using the values presented in Table 4.3 :

- str_#1 $\Rightarrow$ $C_T(l) = 39.5 \times 10^{-12} \times l$ J/K
- str_#2 $\Rightarrow$ $C_T(l) = 314.0 \times 10^{-12} \times l$ J/K

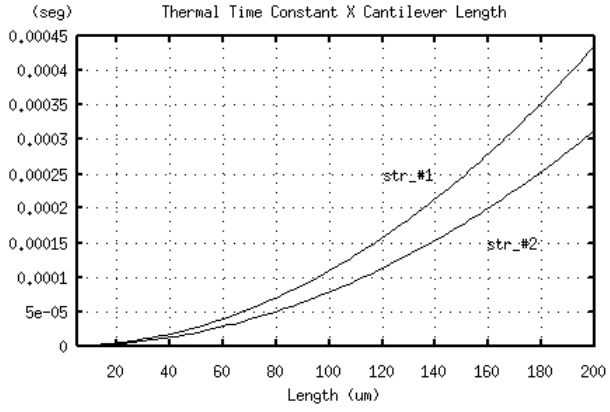
and the thermal time constant for both incoming power cases considered and both GaAs suspended structures proposed, as a function of the cantilever length, is shown in Fig. 4.6.

TABLE 4.3 - Specific heat and density of suspended structure layers.

Material	Specific heat (J/kg.K)	Density (kg/m^3)
GaAs	350	5360
$Al_{0.25}Ga_{0.75}As$	383	4960
TiAu	129	19300
Si_3N_4	700	3100
SiO_2	730	2200



(a)



(b)

Fig. 4.6 - Thermal time constant as a function of cantilever length: (a) only incoming power at the end of the structure and (b) only irradiated power homogeneously distributed.

4.4.2 Electrical Equivalent of Thermal Parameters

For electrical engineers is commonly easier to evaluate systems in terms of electrical parameters. Fortunately, the behavior of thermal and electrical systems are mathematically described by the same equations. Thus, temperature and heat flux are fundamental variables, equivalent to voltage and current in an electrical circuit, while heat capacity and thermal resistance describe the basic properties of a system and correspond, respectively, to capacitance and electrical resistance [28][29].

Therefore, the analogy between thermal and electrical systems, summarized in Table 4.4, enables to describe thermal systems as equivalent electrical circuits, which is convenient because of the many excellent tools available for electrical circuit analysis and the familiarity of solving electrical network problems. Moreover, certain boundary conditions have to be fulfilled at the edges of the structure that can be translated into additional components. The most frequenly encountered boundary conditions are prescribed temperature, heat flow and conductance, which can be represented by a voltage source, a current source and a contact conductance, respectively.

TABLE 4.4 - Analogy between thermal and electrical parameters [1].

Thermal Parameters	Electrical Parameters
Temperature T (K)	Voltage V (V)
Heat flow - Power P (W)	Current I (A)
Heat Q (J=W.s)	Charge Q (C=A.s)
Resistance R (K/W)	Resistance R (Ω=V/A)
Conductance G (W/K)	Conductance G (S=Ω^{-1})
Capacity C (J/K)	Capacitance C (F=A.s/V)
Thermal resistivity ρ_{th} (K.m/W)	Electrical resistivity ρ_{el} (Ω.m)
Thermal conductivity K (W/K.m)	Electrical conductivity σ (S/m)
Specific heat c_p (J/kg.K)	Permittivity ε (F/m)

Note that, even though in the true physical sense thermal power and electrical power are equivalent, thermal power is represented as to an electrical current, and there is no thermal equivalent for electrical power. Moreover, while geometrical dependence are similar for both electrical and thermal resistances and conductances, they differ from capacitances. The thermal capacitance is directly proportional to the volume of the body and thus, for bodies of equal

composition and shape (congruent bodies), to the third power of the linear scaling factor. The electrical capacitance of congruent bodies, however, increases in direct proportion to the linear scaling factor. Finally, there is no known thermal equivalent to an electrical inductor [1].

The real behavior of a thermal system is obviously non-linear because the heat capacity and thermal resistance are generally temperature dependent. However, a linear model of a thermal system or a thermal sensor can often yield a good estimation of its characteristic behavior. For example, a useful estimation of the real thermal time constant can be obtained from a simple model of the temporal response of a body as a first order system, that is, an exponential function.

In many cases a numerical solution of a model is required, since no easy analytical solutions are at hand. In these cases, numerical modeling of the physical situation may be used. By using electrical analogies, electrical circuit simulators, such as SPICE, are very helpful for time dependent analysis. Alternatively, software packages such as ANSYS or other finite element modeling packages can be used, while for simple problems one can do numerical calculations using simple software routines based on elementary models.

a) Electro-Thermal Converter

In the AC-DC converter and microwave power sensor, a direct incoming power is applied at the end of a cantilever or in the middle of bridges and membranes by using a heater (resistor). An alternate electrical current passes across the resistor and the generated heat by Joule effect is transmitted through the structure towards the sink (non-suspended part). Such heat flux generates a temperature rise in the suspended device. Thermal convection, irradiation and conduction represent important parameters.

An equivalent electrical circuit for the AC-DC converter is illustrated in Fig. 4.7 [29]. R_i represents the thermal resistance of the area comprised between the heater and the hot junction of the thermocouple, while R_t is the total thermal resistance of the portion between the hot junction and the sink. These values are obtained using the following equation :

$$\frac{1}{R_{i,t}} = \sum_j \frac{1}{R_j} = \sum_j \frac{\kappa_j \cdot w_j \cdot t_j}{l_j} \qquad (4.32)$$

More precisely, the resistance division of R_i and R_t is done taken into account the actual bridge position where the average temperature is found [11]. R_s corresponds to the inverse of the surface conductance estimated using (4.18), i.e., $R_s = 1 / G_s$. In turn, C_i and C_t correspond to the

thermal capacitance of respective regions, estimated using (4.31).An electrical simulation output is shown in Fig. 4.8, and the results of temperature difference and time constant for both structures are given in Table 4.5.

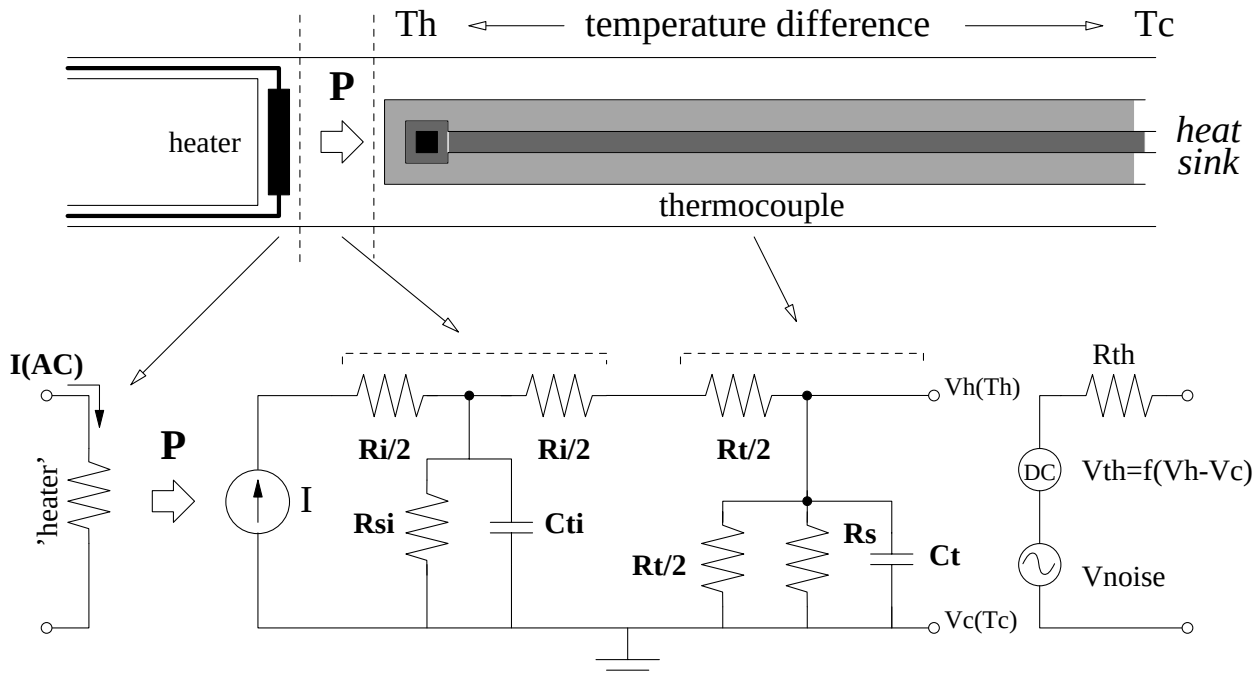


Fig. 4.7 - Equivalent electrical circuit model of electro-thermal converter.

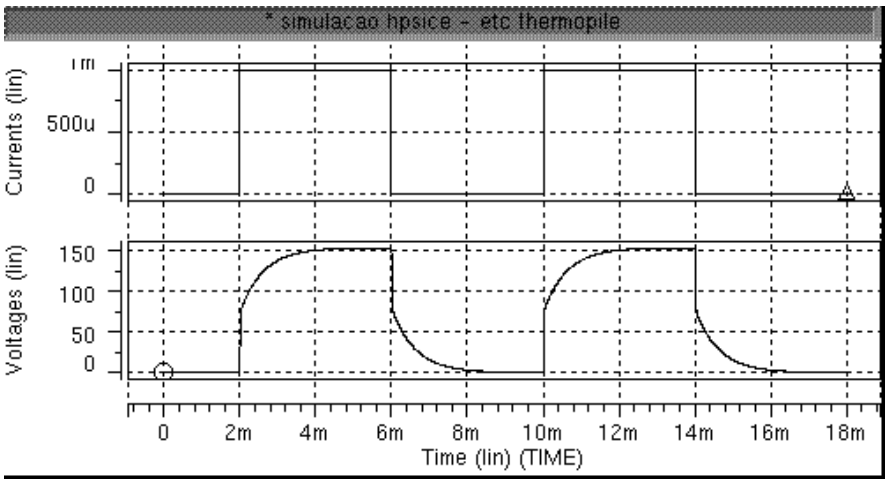


Fig. 4.8 - Electrical simulation of electro-thermal converter.

b) Infrared detector

In the case of the infrared detector, where an irradiation is homogeneously applied to the structure, the method consists in dividing the whole structure in n small portions, i.e.,

dx = length / n, as depicted in Fig. 4.9. Each portion dx is represented by a sub-circuit containing the proportional incoming power ($I = N_S / n$), thermal resistance ($R_{si} \approx R_T / n$), thermal capacitance ($C_{ti} \approx C_T / n$), and surface conductance ($R_{si} \approx 1 / n.G_S$). The values of C_T and R_T are calculated using (4.31) and (4.32), respectively, and G_S through the expression (4.18).

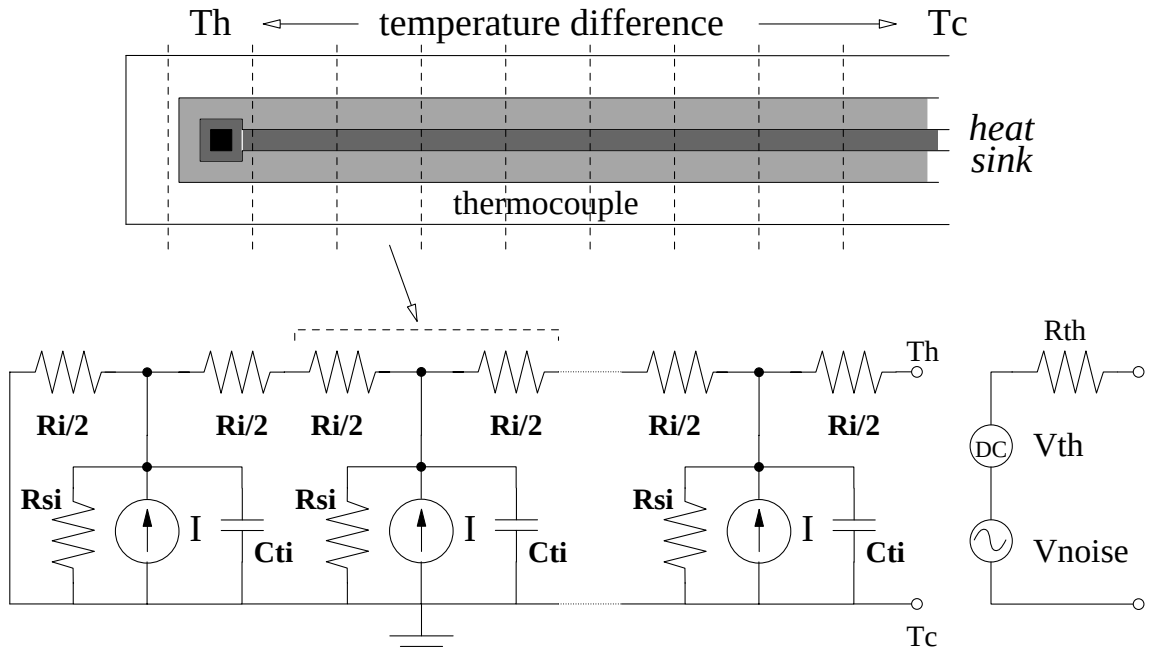


Fig. 4.9 - Equivalent electrical circuit model of infrared detector.

These circuits are placed in series configuration to represent the whole device. The precision of the model is improved by increasing the number of divisions (n), or reducing dx. The output from the electrical simulation is shown in Fig. 4.10, and the results are presented in Table 4.5.

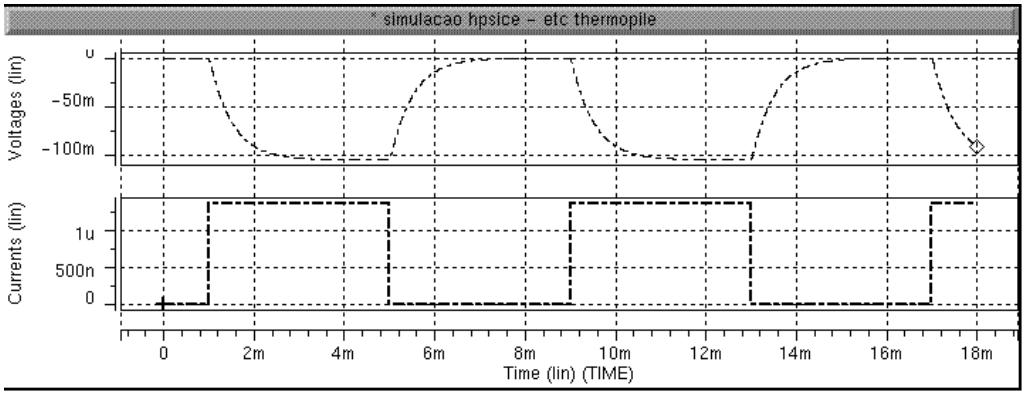


Fig. 4.10 - Electrical simulation of infrared detector obtained using SPICE tool.

4.4.3 Finite Element Method Simulation

Both proposed GaAs-TiAu thermocouples were also evaluated through FEM simulations. The three-dimensional solid model for both cantilevers (str_#1 and str_#2) were created and simulated considering the two kinds of incoming powers, presented in the previously discussed methods of analysis. Static and transient simulations were carried out in order to obtain the temperature differences and the time constant parameter. These results are presented in Table 4.5 and compared to the analytical formulations and electrical circuit models. The illustration of the thermocouple FEM geometry and an output obtained from the transient analysis are shown in Figs. 4.11 and 4.12, respectively.

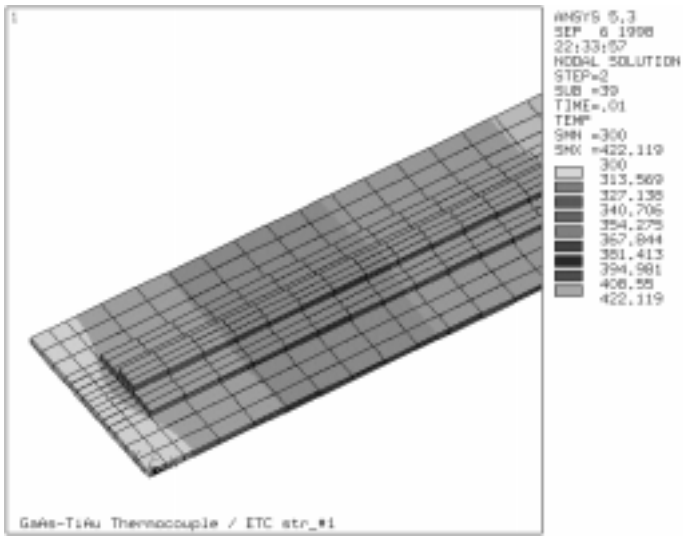


Fig. 4.11 - GaAs-TiAu thermocouple solid model for FEM simulations.

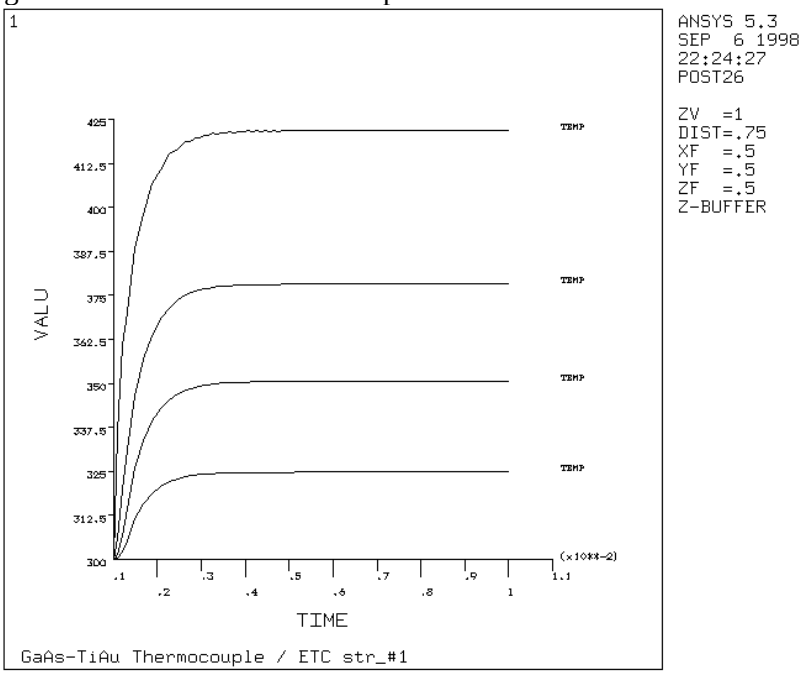


Fig. 4.12 - Results from a FEM transient simulation.

TABLE 4.5 - Temperature difference and time constant of 200 µm-length GaAs-TiAu thermocouples.

	ΔT_B			τ (ms)		
	analytical	electrical	FEM	analytical	electrical	FEM
ETC str_#1	160.0	160.0	121.8	0.6	0.2	0.4
ETC str_#2	28.0	27.8	25.2	0.8	0.3	0.4
IR str_#1	0.11	0.10	0.15	0.3	0.5	0.6
IR str_#2	0.036	0.034	0.031	0.4	0.7	0.6

Obs.: ETC - electro-thermal converter (1mW); IR - infrared detector (1000 W/m^2).

4.4.4 Fabrication and Experimental Results

The fabrication and characterization tests of infrared detectors and microwave power sensors are in progress. Unfortunately, no useful experimental results are available at the present time. In Fig. 4.13 is shown the microwave power sensor, or electrical-thermal converter, while the microphotograph of a thermopile-based infrared detector composed by 20 GaAs-TiAu thermocouples is shown in Fig. 4.14.

4.5 CONCLUSION

The investigation of micromachined thermal-based devices has shown the feasibility of suspended passive and active electronic devices, which can be efficiently exploited in future works for a large number of promising applications. On the other hand, this chapter was dedicated mainly to thermopile-based devices, because of the interesting features presented by the GaAs material, such as high thermal resistivity and significant Seebeck coefficient. Two kinds of GaAs-TiAu thermocouple structures, which take into account the selective and preferential etching behaviors, were proposed to the PML HEMT process. Three different methods of analysis, i.e., the analytical formulation, electrical circuit model and FEM simulation, were carried out, and showed that the microwave power sensor is very useful in MMIC design, while the infrared detector presents a low performance due to the absence of the sensitive area or black layer in the hot region. Fabrication and experimental measurements are on going.

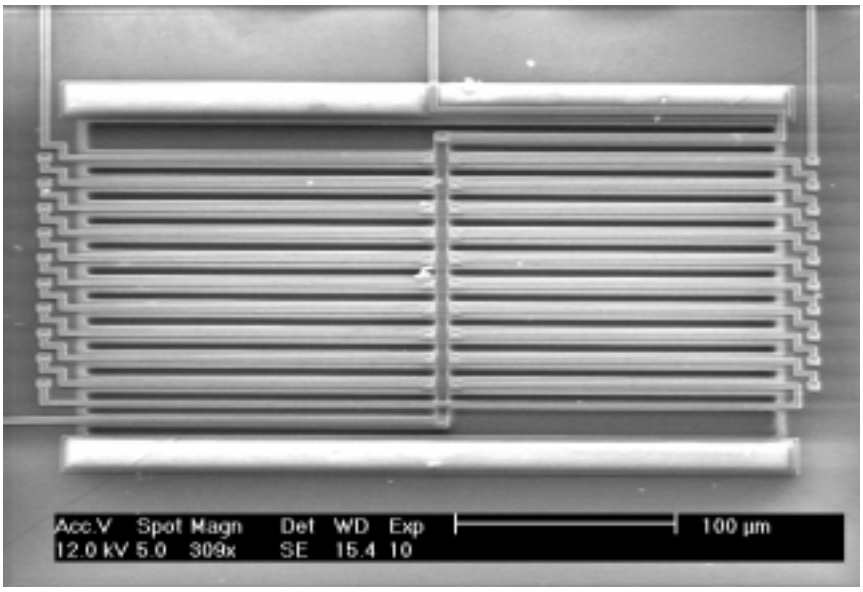


Fig. 4.13 - Microwave power sensor composed by 20 GaAs-TiAu thermocouples.

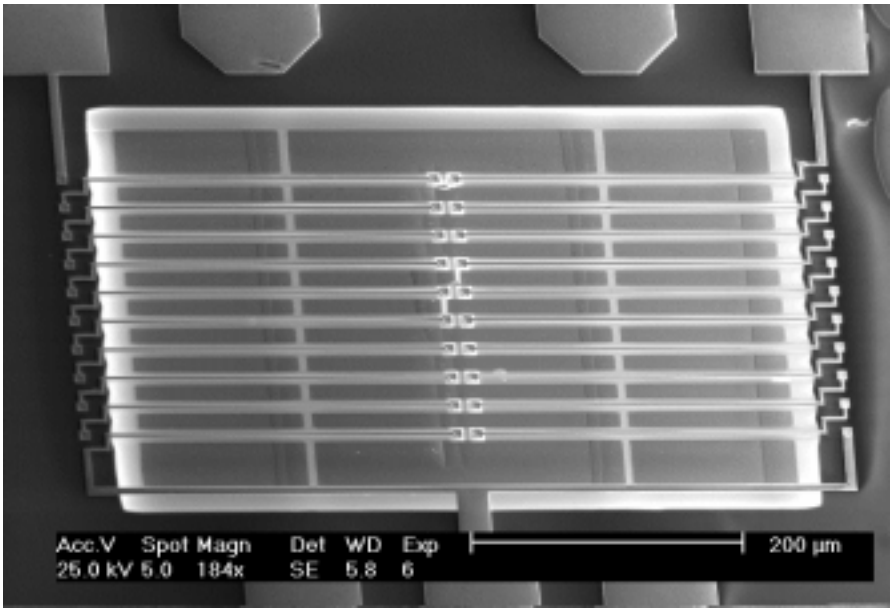


Fig. 4.14 - Infrared detector composed by 20 GaAs-TiAu thermocouples.

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Chapter 5
MICROMACHINED MICROWAVE PASSIVE DEVICES

Besides microsensors and microactuators, micromachining techniques are also very useful to enhance microwave and millimeter wave passive devices and circuits. In general, the etching of bulk material underneath microstrip lines reduces significantly shunt parasitic capacitances and substrate losses, commonly critical in silicon processes. The GaAs front-side bulk micromachining compatible with the PML HEMT D02AH process presents interesting features such as the small open area width, the numerous suitable etchants, and the availability of MMIC design. Initially, the microstrip transmission theory is briefly reviewed, and the shunt capacitance reduction is suspended lines are evaluated through computing simulations and experimental measurements. Next, a novel micromachined planar spiral inductor, with each strip suspended individually, is presented. Significant improvements in Q-factor and resonant frequencies have been predicted by theoretical analysis and verified through measurements carried out up to 15 GHz. A two interleaved spiral inductor structure, in 1:1 transformer-like configuration, has also been fabricated in order to demonstrate the promising capabilities of this new micromachined device. Finally, mechanical and heating characteristics related to suspended microwave passive components are investigated.

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5.1 INTRODUCTION

Monolithic microwave integrated circuits (MMIC) are rapidly outspacing discrete and hybrid components in wireless communication market. Such increasing interest in MMICs is a result of several emergent applications, like mobile products, satellite reception (GPS and DBS), millimeter-wave radiometers and automotive systems. The reasons are embedded in the following promising attributes of the monolithic approach : low cost, volume manufacturability, improved reliability and reproducibility, small size and weight, low power consumption, circuit design flexibility, multi-function performance on the chip, as well as the broadband performance due to the elimination of undesirable parasitic influence caused by wire bonding and embedded active components [1].

With recent advances in microelectronics processes, silicon based bipolar transistors and FET's with GHz cut-off frequencies (f_T) are nowadays available for radio-frequency (RF) applications [2][3]. Nevertheless, GaAs, whose IC processes have shown an important increase in fabrication yield, continues to be the most useful technology at such broadband frequency mainly because of its higher carrier mobility and the semi-insulating substrate characteristics. GaAs based technologies, such as the 0.2 µm HEMT D02AH process from Philips Microwave Limeil (PML), which provides pseudomorphic high-electron mobility transistors (P-HEMT's) with f_T up to around 60 GHz, are commercially available for monolithic microwave and millimeter-wave applications [4].

However, integrated RF passive components, in particular planar inductors, represent one of the key elements for MMIC design, because of the low performance at high frequencies caused by losses and parasitic effects. In silicon, with the advent of SiGe-HBT and submicron technologies which allow transistors with performances comparable to GaAs ones, a great effort has been realized in order to provide silicon-compatible inductors with acceptable quality factors (Q), by considering, e.g., multilevel interconnect processes, high-resistivity substrates, and Cu metallization instead of Al for interconnections [5]-[12].

In GaAs, on the other hand, to minimize the thermal resistance through the substrate, e.g. for FET power amplifier applications, it is desirable to use a wafer as thin as practical. However, a thin wafer increases even more the circuit skin effect losses, and consequently the signal attenuation. Furthermore, since heat-sinking requires bottom-side metallization of the chip, additional shunt capacitance to ground is introduced and corrections must be done for planar inductors to account for 'image' currents due to the ground plane [1].

Micromachining techniques, in turn, have been efficiently applied to reduce high-frequency losses and parasitic capacitances in planar lumped devices, for which the physical length of the line is assumed shorter than one-tenth of the wavelength at the desired frequency of operation, such as microstrip transmission lines, coplanar waveguides, planar spiral inductors and transformers. Membrane-supported and shielded components are easily constructed with IC process compatible micromachining [13]-[20]. Other specific processes, commonly not compatible with electronic circuitry, can provide even more superior performance by creating tall metal transmission lines, vertical inductors and adding magnetic core [21]-[27]. Among all these techniques, the front-side bulk micromachining is certainly the simplest and most efficient approach to micromachined microwave passive devices since a straightforward maskless post-process wet etching is enough to release the structure, with no modifications in the IC fabrication and no influence on the unconcerned electronic blocks [13]-[15].

In this chapter, free-standing microwave passive devices are presented taking into account the PML GaAs HEMT D02AH process. A minimum open area width value of 4 μm, accepted in this technology for micromachining purposes, allows the realization of planar spiral inductor structures with the strips suspended individually. This novel structure is easier to fabricate than the well-known membrane version because the etching time depends only on the line width and not the number of spiral turns, reducing, consequently, the possibility of damage in the pad metallization and passivation layers caused by certain etchants. Moreover, besides shunt capacitances, fringing parasitic effects, very critical in planar spiral transformers, are also significantly reduced. Another important feature is the fact that such PML process is available to MMIC design, allowing the direct use of these suspended devices in microwave and millimeter-wave circuits.

Initially, the microstrip transmission line theory is briefly reviewed, and the behaviour of the free-standing line as a function of the etching depth is evaluated through computer simulations and experimental measurements. Next, the lumped equivalent circuit model, theoretical analysis, fabrication and test of suspended planar spiral inductors are presented. A two interleaved spiral inductor device, in 1:1 transformer-like configuration, has also been modeled and fabricated, and its performance is as well evaluated in order to demonstrate the promising features of the proposed structure. Finally, to complete this study, heating and mechanical characteristics of such micromachined devices are briefly discussed.

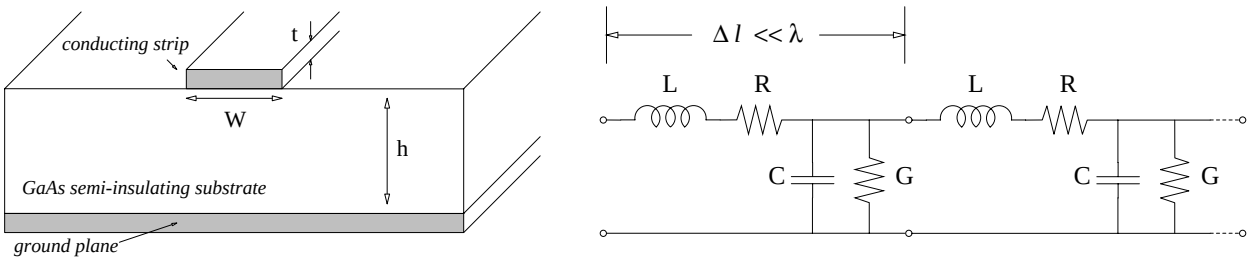
5.2 MICROSTRIP TRANSMISSION LINE

Basically, four types of transmission lines are available on planar substrates : microstrip,

slot line, coplanar waveguide and coplanar stripline [28]. The microstrip line structure, as provided by the PML D02AH process on a 100 μm-thick GaAs substrate, consists of placing a metal strip above a conducting (or ground) plane, with the substrate and intermetallic dielectric layers sandwiched between the two conductors, as illustrated in Fig. 5.1a.

5.2.1 Theory review

The equivalent lumped model which represents a small subsection per unit length of a lossy microstrip transmission line is shown in Fig. 5.1b, where R is the series resistance of the line, L is the associated inductance, C represents the shunt capacitance to the ground plane and G corresponds to the dielectric and bulk conductances, which is usually negligible in semi-insulating GaAs substrate. Note that, all elements are defined per unit of length.



(a) (b)

Fig. 5.1 - Microstrip transmission line: (a) structure and (b) equivalent lumped model.

Therefore, the input impedance of the microstrip depends on the values of R, L, C, and G, the line length, and the termination at the far end. Thus, in order to simplify the description of such a circuit, a reference impedance, called *characteristic impedance* (Zo), is commonly used. The characteristic impedance of a transmission line corresponds to the impedance measured at the input considering infinite the line length. Under these conditions the type of termination at the far end has no effect on the characteristics of the transmission line.

Moreover, electromagnetic waves travel at the speed of light ($c = 3.10^8$ m/s) in free space. In a transmission line, on the other hand, the voltage and current propagations are delayed due to their interaction with the line material. The inductance and capacitance along the line reduce the effective propagation velocity, also known as *phase velocity* (υ). In quasi-static analysis, the mode of wave propagation in lossless microstrip is assumed to be pure TEM.

As a result, both characteristic impedance and phase velocity dependent only on the permeability (μ_r) and the permittivity (ε_r) of the insulating medium, and can be estimated by using

the following equations [28] :

$$Zo(\Omega) = \sqrt{\frac{L}{C}} = 60\sqrt{\frac{\mu_r}{\varepsilon_r}} = \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{W_e} + 0.25\frac{W_e}{h}\right) \qquad \text{for } W/h \le 1 \tag{5.1}$$

and

$$\upsilon(m/s) = \frac{1}{\sqrt{\mu_r \varepsilon_r}} = \frac{c}{\sqrt{\varepsilon_e}} \tag{5.2}$$

where

$$W_e = W + \frac{1.25t}{\pi}\left(1 + \ln\frac{4\pi W}{t}\right) \qquad \text{for } W/h \le 1/2\pi \tag{5.3}$$

and

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(\frac{1}{\sqrt{1 + 12h/W}} + 0.04\left(1 - \frac{W}{h}\right)^2\right) - \frac{\varepsilon_r - 1}{4.6} \cdot \frac{t/h}{\sqrt{W/h}} \tag{5.4}$$

The capacitance C and inductance L, where L represents the self inductance of the signal line minus the mutual inductance of the return current in the back-side ground plane, can be estimated as a function of the characteristic impedance and the substrate permittivity by using :

$$C\ (pF/\mu m) = 3.35x10^{-3}.(\varepsilon_r)^{1/2} / Zo \tag{5.5}$$

$$L\ (nH/\mu m) = 3.35x10^{-6}.Zo.(\varepsilon_r)^{1/2} \tag{5.6}$$

In terms of losses, there are numerous reasons for the attenuation of a signal traveling through a transmission line. Radiation losses occur because the signal energy radiates away from the transmission line, and can be minimized with careful shielding of the lines. Mismatch losses are caused by part of the signal reflecting towards the source, e.g., this could happen because of a mismatch between the load impedance and the characteristic impedance of the microstrip. Conductor or resistor losses are caused by the resistive nature of the conducting medium, knowing that at microwave frequencies the signal flow is concentrated in the surface layer of the conductor, where the current density is maximum, and decreases exponentially with the depth into the conductor. The penetration of the current flow is defined by the *skin depth* (δ), which, for sine wave signals, depends on the conductor resistivity (ρ), the sine wave frequency (∂), and the magnetic permeability of free space (μ_o) :

$$\delta = [\rho / (\pi.\mu_o.\partial)]^{1/2} \tag{5.7}$$

The exact calculation of the frequency-dependent resistance of a metallic conductor with rectangular cross section is a very difficult task and can be done only using sophisticated numerical methods. An empirical expression of the resistance value per unit length is [29][30] :

$$R = R_o\left(1 + K_1 x_w^{2\left(K_2 + K_3 x_w^2\right)}\right) \tag{5.8}$$

where

$x_w = (2.\partial.\sigma.\mu.w.t)^{1/2}$ represents the normalized frequency (5.9)

and

$R_o = (\sigma.w.t)^{-1}$ is the DC resistance of the conductor (5.10)

with

∂ - frequency in Hz;
σ - conductor conductivity;
μ - conductor permittivity;
w - conductor width (μm);
t - conductor thickness (μm);
K_1, K_2 and K_3 - fitting parameters.

Dielectric losses, in turn, are introduced if the dielectric medium is not a vacuum. This is because the medium will absorb part of the energy from the signal passing through it. For most practical applications, the dielectric losses from DC conductivity and the high frequency dissipation factor can be ignored. Anyway, the shunt conductance per unit length (G) depends on the geometrical features of the conductors in the same way as the shunt capacitance (C), and it is given by :

$$G = \omega.C.\tan(\delta) \tag{5.11}$$

where ω is the angular frequency, and $\tan(\delta)$ is the dissipation factor of the substrate which represents the ratio of the imaginary part to the real part of the dielectric permittivity. Finally, hysteresis losses occur when ferrite materials are used as a medium for microwave signals to propagate, and they can be minimized by plating the ferrite material with a conducting metal.

Conductor and dielectric attenuation constants (α_c and α_d, respectively), in dB per unit length, can be estimated using the following equations [28] :

$$\alpha_c = 1.38\Lambda\frac{R_s}{hZ_o}\cdot\frac{32 - (W_e/h)}{32 + (W_e/h)} \qquad \text{for } W/h \le 1 \tag{5.12}$$

and

$$\alpha_d = 520.8\pi\sigma\frac{\varepsilon_e - 1}{\sqrt{\varepsilon_e}(\varepsilon_r - 1)} \tag{5.13}$$

with

$$\Lambda = 1 + \frac{h}{W_e}\left(1 + \frac{1.25t}{\pi W} + \frac{1.25}{\pi}\ln\frac{4\pi W}{t}\right) \qquad \text{for } W/h \le 1/2\pi \tag{5.14}$$

$$R_S = (\pi . f . \mu_0 . \rho_c)^{1/2} \quad \text{where } \rho_c \text{ is the strip conductor resistivity} \tag{5.15}$$

$$\sigma = \omega . \varepsilon_o . \varepsilon_r . \tan(\delta) \quad \text{which represents the dielectric substrate conductivity} \tag{5.16}$$

To model the frequency behavior of the spiral inductors and transformers, the fringing capacitance between the strips and the shunt capacitance between these segments and the back-side ground plane must be taken into account. A 'coupled line' configuration consists of two transmission lines placed parallel to each other in close proximity. In such a case, there is a continuous coupling between the electromagnetic fields of the lines. The capacitances depicted in Fig. 5.2 can be approximated by simple formulas as presented in [31]. Considering these capacitances distribution, the total even- and odd-mode capacitances (C_e and C_o, respectively) are written as :

$$C_e = C_p + C_f + C_f' \tag{5.17}$$

$$C_o = C_p + C_f + C_{ga} + C_{gd} \tag{5.18}$$

where C_p is the parallel plate capacitance, and C_f, C_f', C_{ga}, and C_{gd} represent the various fringing capacitance effects. They can be estimated using :

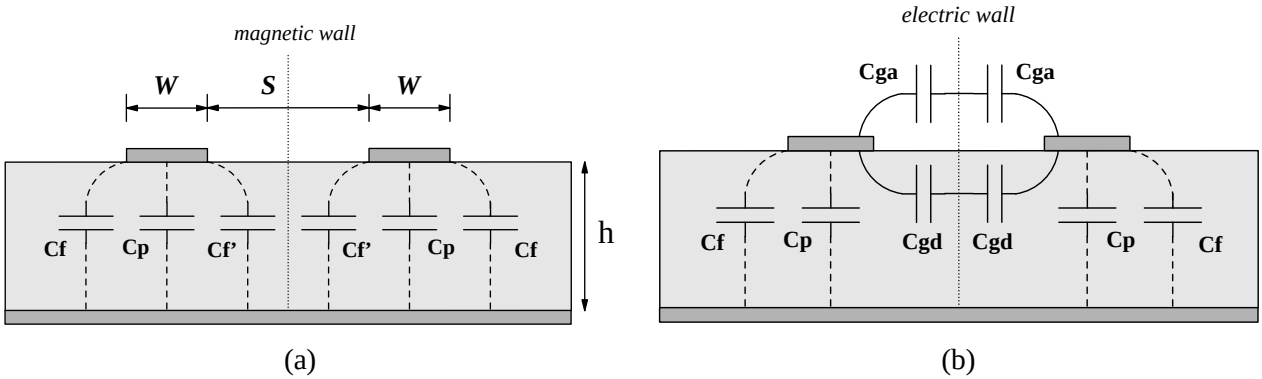
$$C_p = \varepsilon_o . \varepsilon_r . W . h^{-1} \tag{5.19}$$

$$C_f = (\varepsilon_e)^{1/2} / (2.c.Zo) - C_p / 2 \tag{5.20}$$

$$C_f' = C_f / [1 + A.(h / s).\tanh(8.S / h)] \tag{5.21}$$

with

$$A = \exp[-0.1 \exp(2.33 - 2.53\, W.h^{-1})] \tag{5.22}$$



(a) (b)

Fig. 5.2 - Coupled microstrip lines : (a) even- and (b) odd-mode capacitances.

C_{ga} is the capacitance term in odd-mode for fringing field across the gap, in air region, and it is obtained from an equivalent geometry of coplanar strips, given by :

$$C_{ga} = \frac{\varepsilon_o}{\pi} \ln\left(2\,\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right) \qquad \text{for} \quad 0 \le k^2 \le 0.5 \tag{5.23}$$

$$C_{ga} = \pi\varepsilon_o \Big/ \ln\left(2\,\frac{1+\sqrt{k}}{1-\sqrt{k}}\right) \qquad \text{for} \quad 0.5 \le k^2 \le 1 \tag{5.24}$$

where

$$k' = (1 - k^2) \tag{5.25}$$

and

$$k = S / (S + 2.W) \tag{5.26}$$

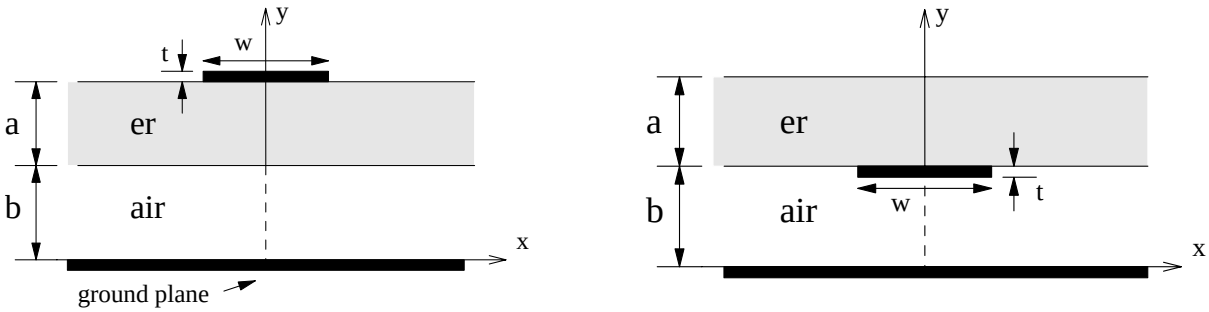
C_{gd}, in turn, represents the capacitance in odd-mode for fringing field across the gap, in dielectric region. It is evaluated by modifying the corresponding capacitance for coupled striplines as following :

$$C_{gd} = \frac{\varepsilon_o \varepsilon_r}{\pi} \ln\left\{\coth\left(\pi S / 4h\right)\right\} + 0.65 C_f \left(\frac{0.02}{S/h}\sqrt{\varepsilon_r} + 1 - \varepsilon^{-2}\right) \tag{5.27}$$

5.2.2 Micromachined microstrip

As presented in Chapter 3, front-side bulk micromachining can be efficiently used to build free-standing microstrips, with no constraints in selective and preferential etching, since no GaAs material is kept underneath the conductor. The main interest in such a kind of transmission line is the significant reduction of losses and parasitic capacitances which appear during GHz frequency operation.

The use of an air gap layer between the metal line and the ground plane is not really a new strategy to improve the performance of microstrips. Suspended and inverted microstrip lines, as shown in Fig. 5.3, are known since the end of the 60s. They present a higher quality factor and wider range of impedance values than conventional microstrips, and an analytical formulation for these lines has been proposed by Pramanick and Bhartia [32]. However, such kind of lines are not fully compatible with microelectronics technology, and the closed-form expressions described in [32] can be used for micromachined lines only in the case that the maximum etching depth is reached, that is, all bulk material beneath the line has been removed. In this case, the height a in Fig. 5.3 is made as small as possible, while height b corresponds to the substrate thickness.



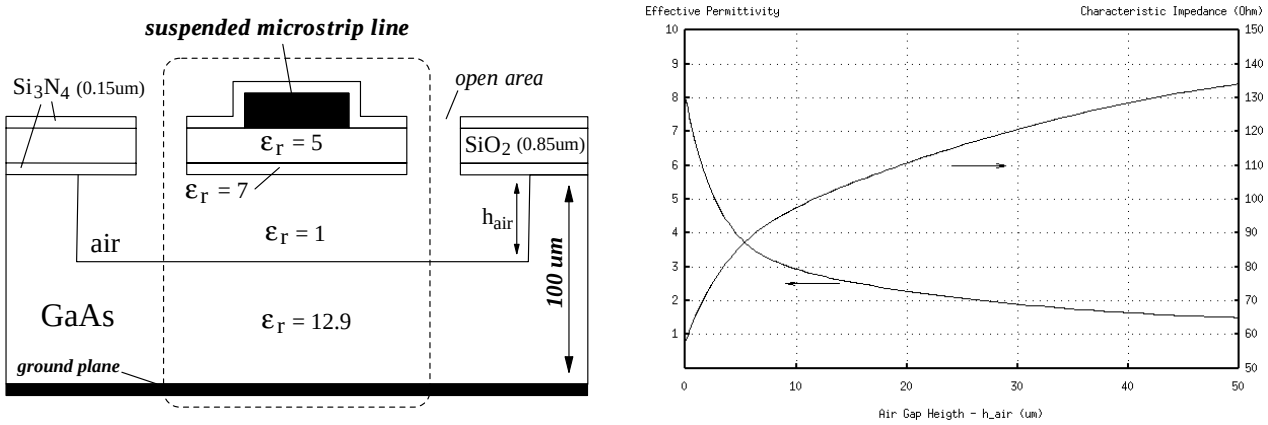
(a) (b)

Fig. 5.3 - Suspended (a) and inverted (b) microstrip lines.

On the other hand, in order to obtain similar improvements, transmission lines built using an air bridge technique are also presented in the literature by Golfard and Tripathi [33]. The microstrip properties as a function of air bridge height were investigated and showed that Zo and ε_e change too rapidly to be physically possible, resulting in a decrease of capacitance value of 35% for a 3 μm high air bridge, while the shift in the inductance per unit length is very small (< 5%) for air bridges up to 10 μm of height. However, such technique is limited to some structure dimensions and geometries.

Micromachined lines, in turn, present several advantages such as the use of standard IC processes, flexibility in the structure geometry, good mechanical properties, electronic compatibility and straightforward manufacturing procedure. Moreover, it is well known that one of the reasons for the high-frequency distortion in planar transmission lines is the mismatch in permittivity between the substrate and air, which causes energy to radiate into the substrate as a shock wave. When the bulk material is etched away, the inhomogeneous dielectric medium encountered by the electric field is eliminated, avoiding consequently radiation losses [16]. On the other hand, although the electrical and magnetic field distributions are slightly modified by micromachining, they could be accurately considered identical for evaluation of their influence on the near circuitry.

The effective permittivity has been computed using a 2D electromagnetic method working in spectral domain [34]. Such analysis has shown that it is not necessary to obtain high air gap, since the ε_e decreases exponentially with the etching depth, as illustrated in Fig. 5.4. As a result, the capacitance between the wires and the back-side ground plane is expected to reduce, e.g., twice by removing only 5% of the substrate material underneath the line. Consequently, the characteristic impedance as well as the phase velocity should increase, according to the equations (5.1) and (5.2).



(a) (b)

Fig. 5.4 - Micromachined microstrip: (a) cross section view and (b) effective permittivity and characteristic impedance as a function of air gap height.

5.2.3 Experimental Results

Suspended microstrip lines were fabricated with different etching depths in order to evaluate the influence of micromachining. Dielectric arms of 5 μm width were placed at intervals of 100 μm along the long lines to avoid mechanical problems, as shown in Fig. 5.5 for a 0.5 mm-length line.

Two-port S-parameter measurements were performed at frequencies in the 0.5 to 15 GHz range, using the HP8510B network analyzer and Cascade Microtech probe station. Open-, short-, thru- and 50 Ω structures were available on a standard substrate for SOLT calibration. Moreover, open and short circuit test patterns were probed to measure pad parasitics for de-embedding. The measured data were transmitted to a computer for automatic parameter extraction. Prior to each acquisition, an additional procedure based on the Y-parameter subtraction method was used to remove the parasitic effects from the probe pads. Such test environment and procedure were also applied for the other microwave passive devices discussed later in this chapter.

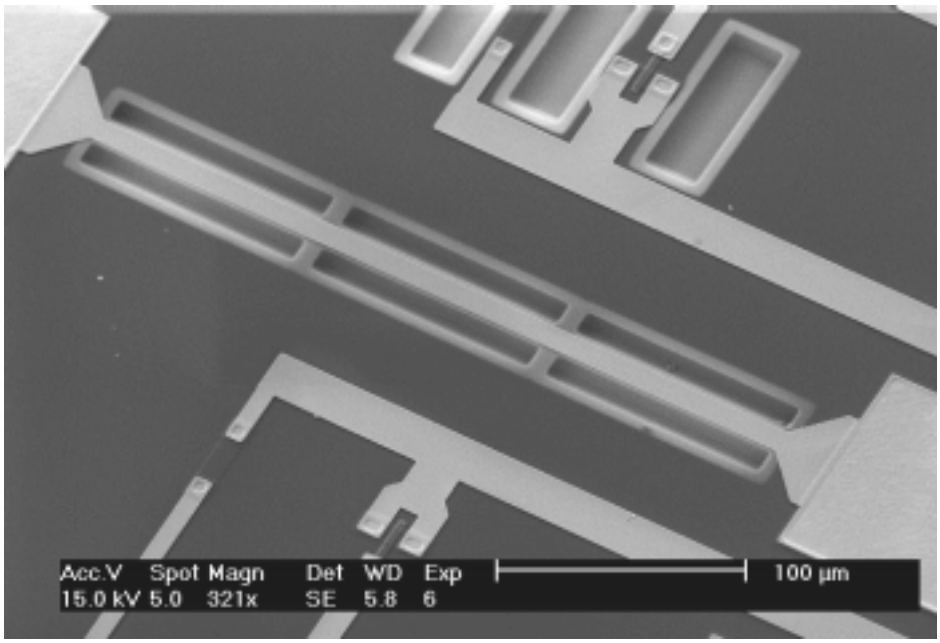
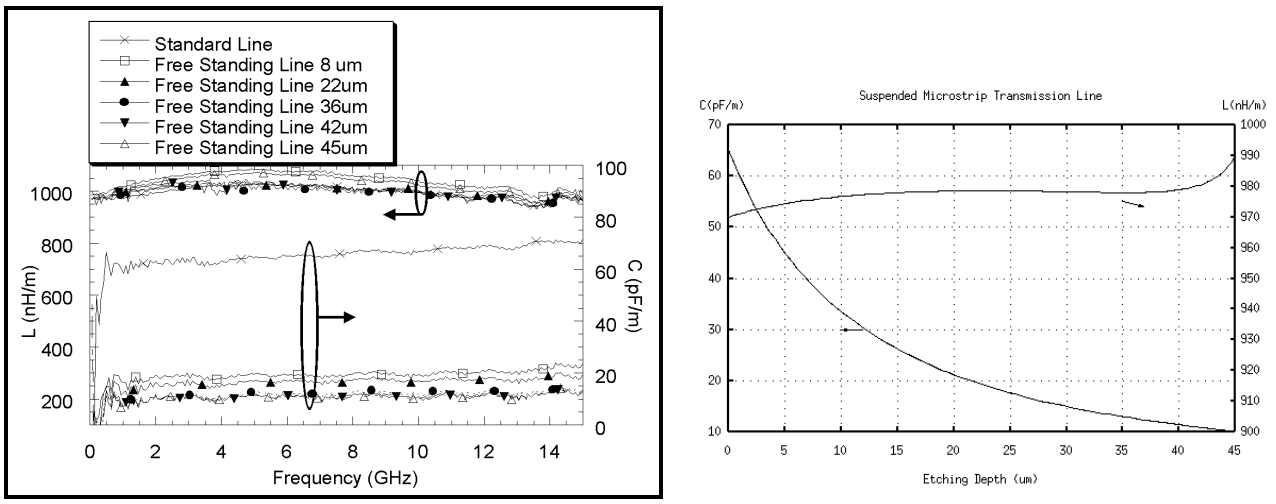


Fig. 5.5 - Microphotograph of 0.3 mm-length suspended microstrip.

The distributed circuit parameters R, L and C were deduced at each frequency point from the propagation constant and characteristic impedance of the microstrip by using the classical Telegrapher's transmission line equation [35]. The measured data showed that both L and C are relatively invariant as a function of the frequency of operation, as shown in Fig. 5.6a for a 5 µm-width and 2 mm-length microstrip. Moreover, in respect to the etching depth, C exhibits an exponential decreasing with the air layer thickness, and agrees well with the computed effective permittivity shown in Fig. 5.4b. On the other hand, L is not really affected by micromachining because it is predominantly determined by the magnetic flux external to the conductor and GaAs substrate, and dielectrics (SiO_2 and Si_3N_4) are not considered as magnetic materials.

5.3 RECTANGULAR PLANAR SPIRAL INDUCTOR

In MMIC design, planar spiral inductors allow strong coupling among individual turns and thus provide high values of inductance on a small area. However, it is a critical component to be integrated because of the undesirable parasitics present in this lumped element, which cause, among others effects, a significant reduction in the self-resonant frequency and the broadband operation. Due to these reasons, planar rectangular spiral inductor devices, like the one provided by PML, have been widely studied and modeled in the literature [36]-[42].

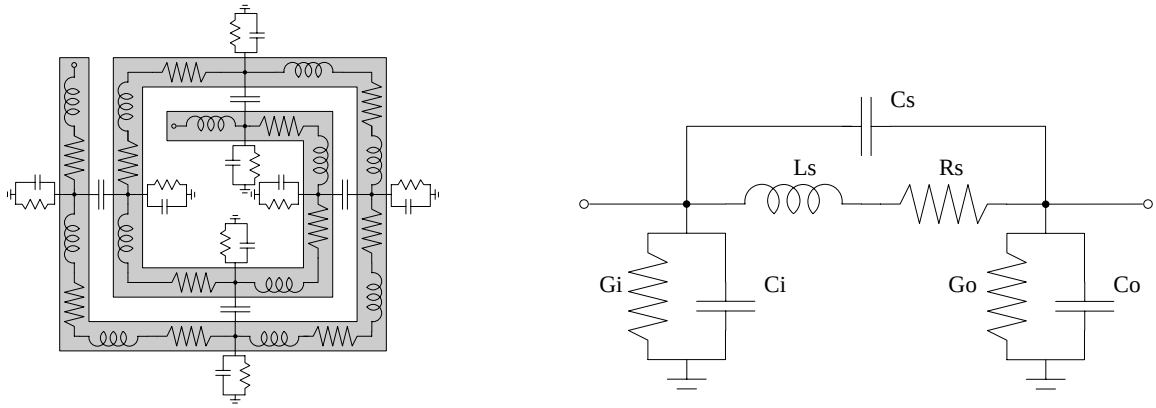


(a) (b)

Fig. 5.6 - Inductance and capacitance, per unit length, of a 5 µm-width and 2 mm-length microstrip *versus* (a) frequency and (b) air gap height.

5.3.1 Design Considerations

As can be seen in Fig. 5.7a, besides the intrinsic inductance and resistance behaviors associated with the metal line, coupling capacitances between spiral segments, as well as shunt capacitances and conductances between the strips and back-side ground plane are present [43]. The classical lumped element equivalent model is depicted in Fig. 5.7b. In this circuit, L_S represents the self and mutual series inductance of the structure and should be estimated taken into account the mirror coil under the ground plane [29][37]. Moreover, R_S represents the series resistance of the metallization and includes a frequency dependent term related to the skin effect and other high frequency parasitics, discussed before for microstrip lines.



(a) (b)

Fig. 5.7 - Planar spiral inductor: (a) intrinsic elements and (b) lumped element equivalent model.

Furthermore, C_s is the coupling capacitance between the metal segments in both dielectric and air regions, while C_i and C_o are the shunt capacitances between the strips and the ground plane. G_i and G_o correspond to the conductivity of the bulk material, frequently neglected in semi-insulating GaAs substrate. Notice that, such substrate conductance represents one of the principal drawbacks of planar inductors on silicon.

To calculate the total inductance L_s of a spiral structure a somewhat complex method must be used. First, the coil is divided up into discrete straight segments, that correspond to each side of the rectangular spiral. Then, L_s is estimated by the sum of the self-inductances of all the segments (L_i) and the mutual inductances between parallel strips, for both positive and negative influence, knowing that the positive mutual inductance (M_+) occurs when current flow in two conductors is in the same direction, and the negative one (M_-) in the opposite sense. Thus :

$$L_s = L_i + M_+ + M_- \tag{5.28}$$

and to calculate L_i, M_+ and M_- the following function I(l,GMD) is useful [36][37] :

$$I(l,\mathrm{GND}) = 2.10^{-4} l \left[\ln\left(\frac{l}{\mathrm{GMD}} + \sqrt{1+\frac{l^2}{\mathrm{GMD}^2}} \right) - \sqrt{1+\frac{\mathrm{GMD}^2}{l^2}} + \frac{\mathrm{GMD}}{l} \right] \tag{5.29}$$

where l is the strip length, in microns. The GMD (geometric mean distance) of a conductor cross section is the distance between two imaginary filaments normal to the cross section, whose mutual inductance is equal to the self-inductance of the conductor. For a rectangular cross section wire, a good approximation of GMD is obtained with :

$$\mathrm{GMD} = 2235.2\ (w + t) \tag{5.30}$$

where w is the width and t is the thickness of the strip, in microns. Making so, the self-inductance for each segment L_i (nH) is equal to I(l,GMD), using the respective l and GMD values.

The GMD between two conductors is the distance between two infinitely thin imaginary filaments, whose mutual inductance is equal to the mutual inductance between the two original conductors. It is calculated using :

$$\ln(\mathrm{GMD}) = \ln(d.10^{-4}) - \{[1/12(d/w)^2] + [1/60(d/w)^4] + [1/168(d/w)^6] + [1/360(d/w)^8] + \ldots\} \tag{5.31}$$

where d is the distance between the track centers, in microns. Thus, taking into account this last expression of GMD and considering that frequently such segments are of different lenghts, to calculate the mutual inductance M between two parallel top-side segments the function I(l,GMD) must be applied twice, that is :

$$M = I(l,\mathrm{GMD}) = I(l_a,\mathrm{GMD}) - I(l_b,\mathrm{GMD}) \tag{5.32}$$

where

$$l_a = (l' + l'') / 2 \tag{5.33a}$$

$$l_b = (l' - l'') / 2 \tag{5.33b}$$

and *l'* and *l"* correspond to the strip lengths, considering *l'* the longest one.

The mirror coil under the ground plane is treated as if it was another physical spiral, on the same exact dimensions as the actual spiral, but located at twice the substrate thickness distance, and with currents flowing in opposite directions. Therefore, the mutual inductance from the top-side coil and its ground plane reflection is estimated using the procedure described above, with the exception that the GMD does not need to be computed, since the segments are so widely separated.

Moreover, note that each mutual inductance between top-side strips is added twice in the total inductance value, since this inductance must be added to both line segments, while the mutual inductance to the mirror coil is only counted one, because the reflected spiral is not in series with the top-side one. Finally, the effects of phase shifting on inductance and capacitance values, discussed by Krafcsik and Dawson [37], were not considered in this work.

The most important characteristics of the inductor are the input impedance (Z_{in}), the self-resonant frequency (f_{res}) and the quality (Q-) factor. The resonant frequency decreases when the number of turns and, consequently, the line capacitance increases. Since the inductors are applicable only for frequencies bellow f_{res}, it is highly desirable to make the ratio of such frequency to the inductance value as high as possible.

The Q-factor of the inductor is defined as the ratio of the imaginary part to the real part of the input impedance value, being so dependent of the operation band. That is, Q-factor increases with the frequency up to the peak value and drops at higher frequencies. This is easily understood by the fact that the reactance of Z_{in}, dominated by the inductance at lower frequencies, rolls off at higher frequencies due to the fringing and shunt capacitances. Therefore, the maximum Q-factor and the frequency at this point are important to guarantee the inductive behavior of the structure.

These characteristics can be calculated taken into account the Z_{in} function, obtained from one side port of the device with the other one grounded. Thus, considering :

$$Z_{in}(\omega) = \alpha(\omega) + j\,\beta(\omega) \tag{5.34}$$

they are :

- Impedance module ($|Z_{in}|$): $$|Z_{in}(\omega)| = \sqrt{\alpha(\omega)^2 + \beta(\omega)^2} \tag{5.35}$$

- Impedance phase (Zin_θ): $Zin_\theta(\omega) = tg^{-1}(\beta(\omega)/\alpha(\omega))$ (5.36)
- Reactance (X) $X(\omega) = \beta(\omega)$ (5.37)
- Self-resonant frequency (ω_{res}): $\omega_{res} \Rightarrow \beta(\omega) = 0$ (5.38)
- Quality factor (Q): $Q(\omega) = \beta(\omega)/\alpha(\omega)$ (5.39)
- Maximum quality factor (Q_{max}): $Q_{max} = Q(\omega_Q)$ (5.40)
- Frequency of Q_{max} (ω_Q): $\omega_Q \Rightarrow \partial Q/\partial\omega = 0$ (5.41)

The GaAs HEMT D02AH process allows to build rectangular planar spiral inductors up to 15 nH, using width and spacing line values ranging from 5 µm to 15 µm. Moreover, the lumped equivalent circuit model proposed by PML presents additionally series inductance elements (L_p) at each side port, as depicted in Fig. 5.8. To calculate the electrical inductor characteristics, described before, the resultant equations from the PML model to obtain the variables $\alpha(\omega)$ and $\beta(\omega)$ are :

$$\alpha(\omega) = \alpha_1(\omega) / \Delta(\omega) \quad (5.42a)$$

$$\beta(\omega) = \beta_1(\omega) / \Delta(\omega) \quad (5.42b)$$

where

$$\alpha_1(\omega) = A(\omega) \,.\, C(\omega) + B(\omega) \,.\, D(\omega) \quad (5.43a)$$

$$\beta_1(\omega) = B(\omega) \,.\, C(\omega) - A(\omega) \,.\, D(\omega) \quad (5.43b)$$

$$\Delta(\omega) = C(\omega)^2 + D(\omega)^2 \quad (5.43c)$$

and

$$A(\omega) = R - \omega^2.L_p.R.(C_i + C_o + 2.C_s) + \omega^4.R.L_p^2.(C_i.C_o + C_i.C_s + C_o.C_s) \quad (5.44a)$$

$$B(\omega) = \omega^5.L_s.L_p^2.(C_i.C_o + C_i.C_s + C_o.C_s) - \omega^3.L_p.(L_s.C_i + L_s.C_o + 2.L_s.C_s + L_p.C_i + L_p.C_o) + \omega(L_s + 2.L_p) \quad (5.44b)$$

$$C(\omega) = \omega^4.L_s.L_p.(C_i.C_o + C_i.C_s + C_o.C_s) - \omega^2.(L_s.C_i + L_s.C_s + L_p.C_i + L_p.C_o) + 1 \quad (5.44c)$$

$$D(\omega) = \omega R.(C_i + C_s) - \omega^3.R.L_p.(C_i.C_o + C_i.C_s + C_o.C_s) \quad (5.44d)$$

The model element values are provided in the foundry design manual [4]. Taking into account such values, for instance, the maximum Q-factor and self-resonant frequency of 1.5 nH inductors from PML are approximately 15 (at 18 GHz) and 30 GHz, respectively, while a 15.0 nH inductor presents the Q_{max} of approximately 4.5 (at 1.7 GHz) and f_{res} equal to 3 GHz.

As presented for microstrip lines, the performance of planar inductors can also be significantly improved by creating an air gap layer underneath the structure, in order to reduce the

shunt capacitance effects. Although partially suspended GaAs inductors have been successfully realized using air bridged lines, showing approximately a 27% decrease in the effective capacitance of the spiral, this technique is somewhat problematic to construct completely free-standing devices, easily obtained using micromachining approaches [33].

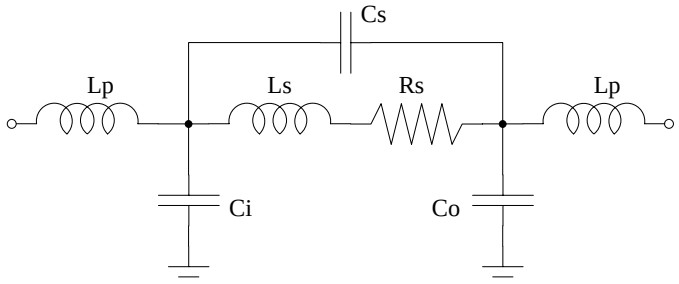
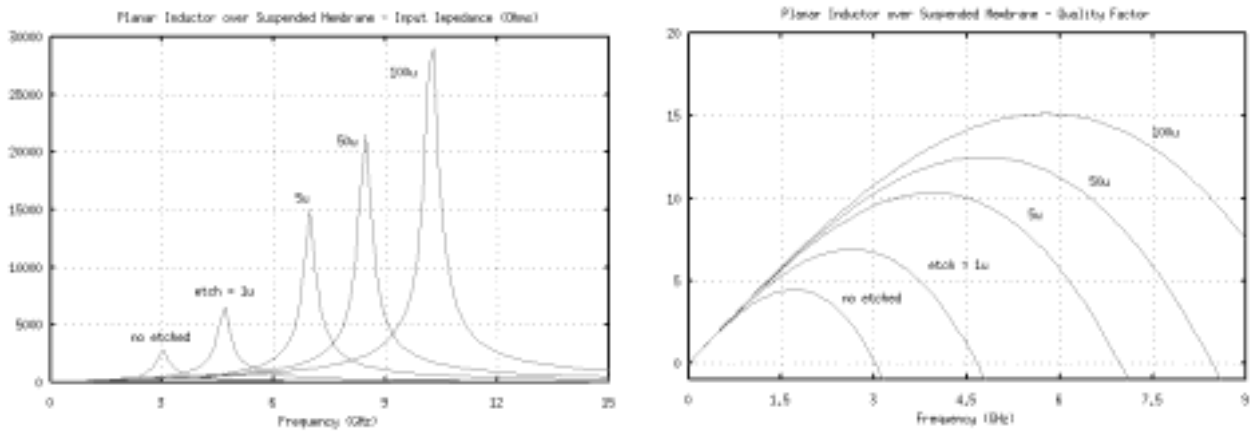


Fig. 5.8 - PML lumped equivalent model for planar inductor.

According to the formulations given above, and considering the model element values provided by PML and the shunt capacitance reduction predicted for a single micromachined microstrip line, a brief theoretical analysis shows that, for an etched depth of around 5 μm, improvements of 80% in the maximum Q-factor and 77% in resonant frequency are expected for a 1.5 nH inductor (R_s=7.2Ω; L_s=1.5nH; L_p=0.0nH; C_i=15.5fF; C_o=8.8fF and C_s=3.0fF), while for larger structures it could be even more significant, attaining 133% and 118%, respectively, for a 15 nH inductor (R_s=23.7Ω; L_s=12.2nH; L_p=1.4nH; C_i=200.0fF; C_o=144.4fF and C_s=2.2fF), as illustrated in Fig. 5.9. Note that, the frequency of the Q_{max} also increases, suggesting the applicability of such micromachined planar inductors at higher broadband operation.

5.3.2 Experimental Results

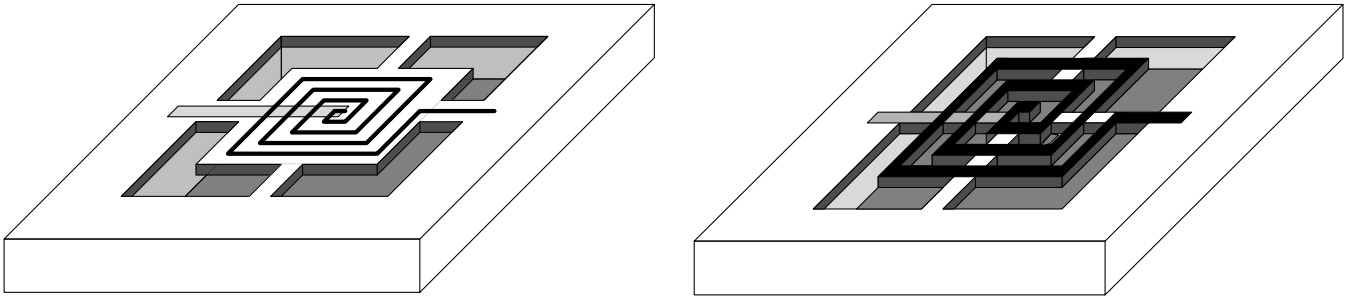
Like presented by Chang et al. [13] in silicon technology, the construction of a membrane-supported planar spiral inductor is also easily realized by using this approach (see Fig. 5.10a). Moreover, a novel planar inductor with the strips suspended individually is possible, taking the advantage of small open area dimensions used herein for micromachining purpose, as illustrated in Fig. 5.10b.



(a) (b)

Fig. 5.9 – Estimated input impedance (a) and Q-factor (b) of 15 nH inductor with suspended segments.

Both versions present very distinct characteristics. In terms of the post-process etching procedure, the membrane requires longer etching time for complete suspension, which corresponds approximately to the underetching rate multiplied by the half membrane width. In the second structure, such etching time is equivalent to that one required to suspend a single line, that is, the underetch rate multiplied by the half segment width. Note that, as a result, it is independent of the total spiral dimensions or turns number. In terms of the electrical behavior, since the lines are completely isolated by air, an even more significant reduction in the fringing parasitic capacitances is obtained. Mechanical properties and heating dissipation are also dissimilar, and they are discussed in details bellow.



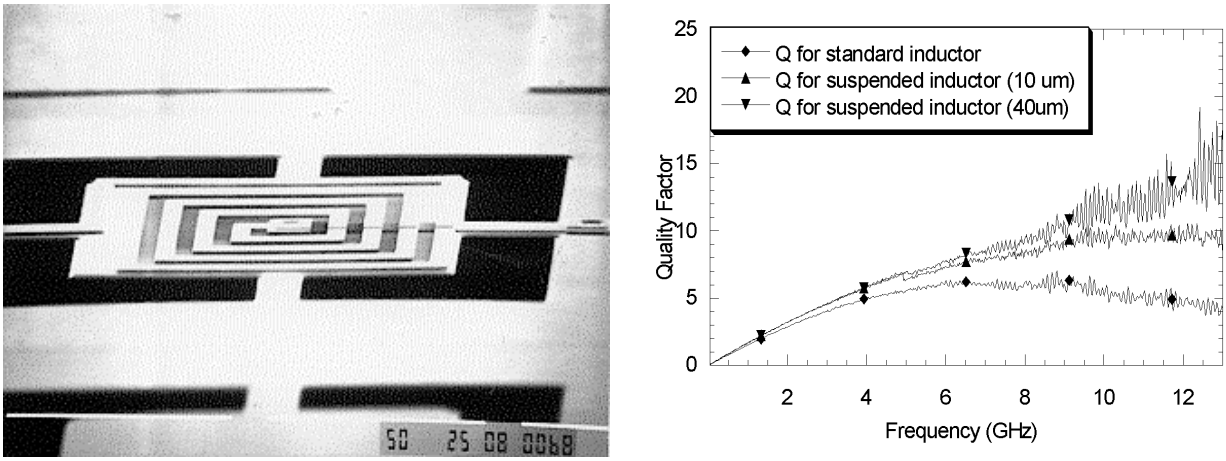
(a) (b)

Fig. 5.10 - Suspended planar spiral inductor: (a) over membrane and (b) with isolated strips.

An 1.1 nH inductor, formed by 4 spiral turns and 5 μm-width and 5 μm-space segments, was fabricated on a dielectric membrane, as shown in Fig. 5.11a. However, because of the small inductance value the resonant frequency occurs far from the limit of the operation frequency of 15 GHz imposed by the test environment (see Fig. 5.11b), and no useful information could be extracted from the measurements.

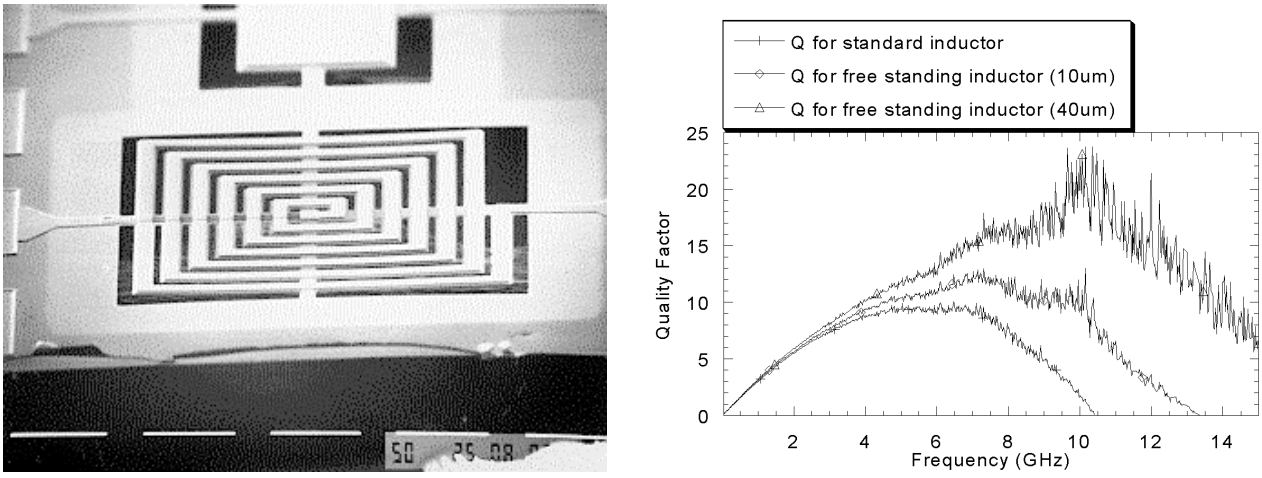
In the case of the structure presenting suspended isolated wires, two planar spiral inductors were fabricated and etched: a 4.9 nH inductor formed by 6 spiral turns and 9 µm-width and 9 µm-space segments (see Fig. 5.12), and a 12 nH inductor with 10 turns, and 5 µm-width and 6 µm-space segments. In the 12 nH inductor structure, thin dielectric arms are placed at four corners of the 5 most external spiral turns to prevent eventual mechanical fracture, as shown in Fig. 5.13.

At low frequencies, measured inductance, which can be easily obtained in terms of Y-parameters as $L_s=Im(1/Y_{12})/\omega$, agrees well with the predicted theoretical values. Notice that, the negative mutual inductances due to image spiral are equal to 0.3 nH and 1.1 nH for the 4.9 nH and 12 nH inductors, respectively, representing more than 5% of the total L value. The measured resistive component, $R_s= Real(1/Y_{12})$, is close to the DC resistance of the metal line.



(a) (b)

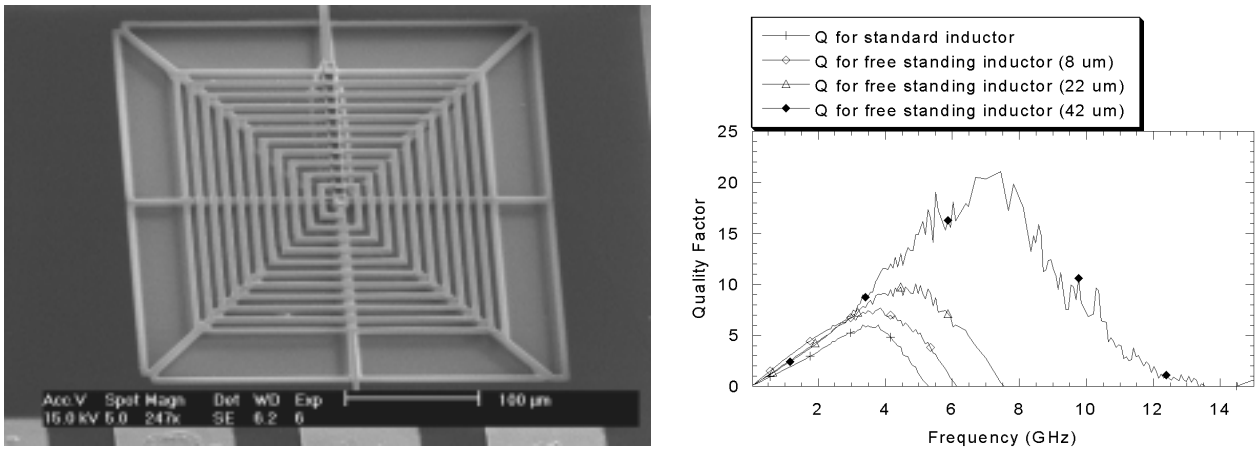
Fig. 5.11 - Planar inductor of 1.1 nH over membrane: (a) microphotograph and (b) measured Q-factor.



(a) (b)

Fig. 5.12 - Inductor of 4.9 nH with isolated strips: (a) microphotograph and (b) measured Q-factor.

The extracted capacitances, on the other hand, which are directly given by $C_i=Im(Y_{11}+Y_{12})$ and $C_o=Im(Y_{22}+Y_{21})/\omega$, are 50 fF and 65 fF for the 12 nH standard or non-suspended inductor, while a much lower value down to 3 fF was obtained with the micromachined structure. However, the C_s value was found to be predominantly determined by the spiral and center-tap underpass capacitance, not influenced by micromachining. The extracted values are summarized in Table 5.1 and illustrated in Fig. 5.15. Furthermore, the equivalent element model behavior agrees well with the measured S-parameters, as illustrated in Fig. 5.14.



(a) (b)

Fig. 5.13 - Inductor of 12 nH with isolated strips: (a) microphotograph and (b) measured Q-factor.

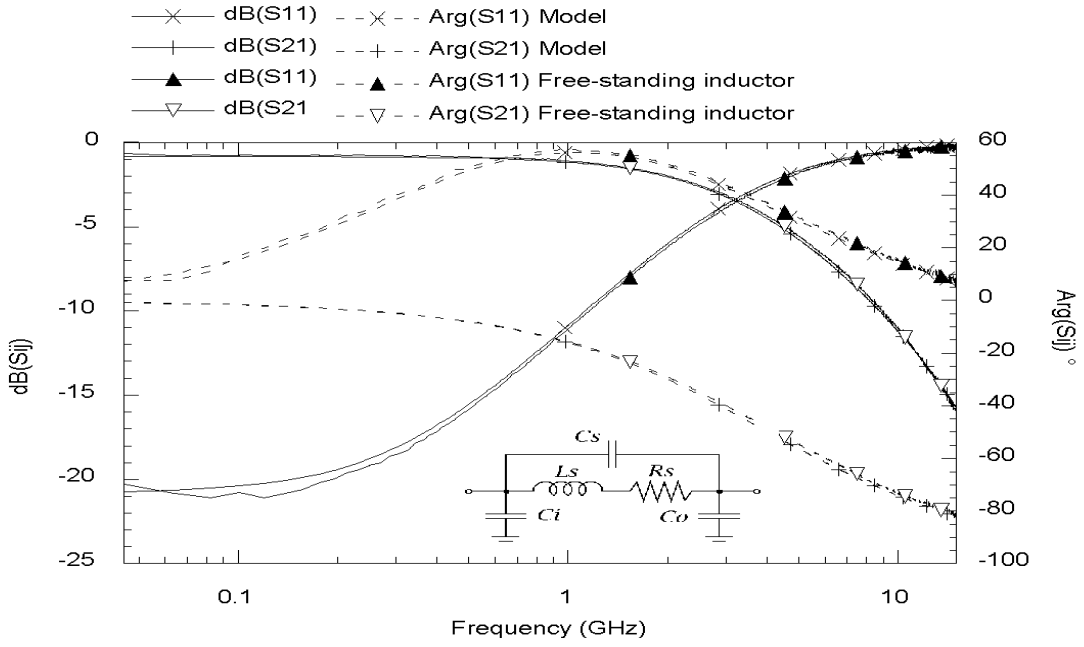
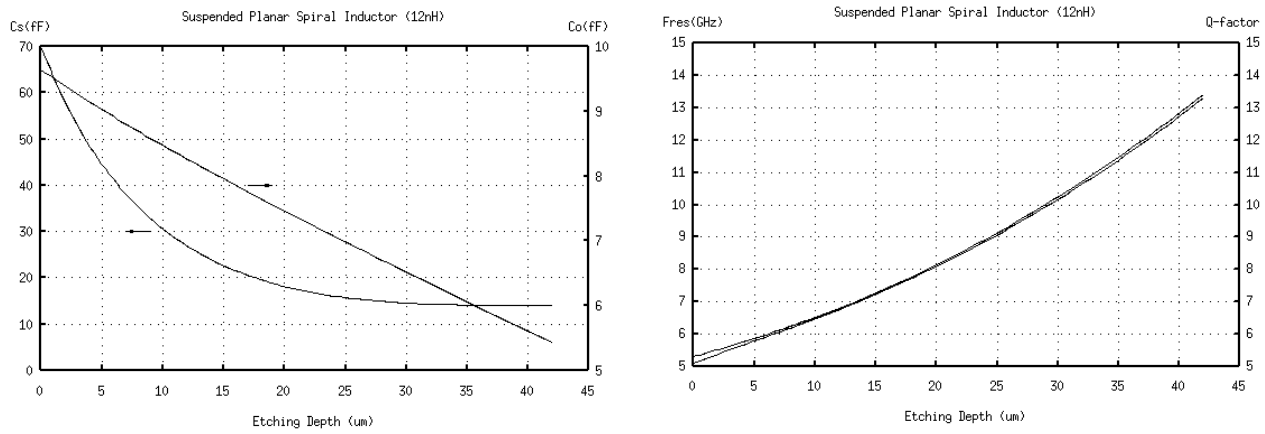


Fig. 5.14 - S-parameters measurements versus inductor lumped model.

5.4 PLANAR SPIRAL TRANSFORMER

A planar transformer structure is formed by two interleaved spiral inductors, as shown in Fig. 5.16a, and its potential applications are centered around two characteristics : the ability to transform impedance level, changing the ratio of current to voltage without losing a significant amount of power, and the ability to transfer energy between two electrical meshes, without having these meshes at the same potential. For instance, transformers can be used to generate high AC voltages when only low voltages are available, match low impedance load to high impedance source, isolate loads from ground, provide 180 degree phase shift, shape pulses and, by tuning, provide bandpass filter characteristics [30]. In the literature, several works show the construction of monolithic lumped parameter four-port quadrature hybrid and phase shifter based on coupled spiral inductors [44]-[46], but the use of a planar transformer can also be extended to microsensors, e.g., the Eddy-current proximity sensors, as proposed by Gupta and Neikirk [47].



(a) (b)

Fig. 5.15 - Parameters of 12 nH inductor as a function of etching depth: (a) C_o / C_s, and (b) F_{res} / Q_{max}.

TABLE 5.1 - Characteristics of standard and micromachined planar inductor with isolated strips.

12 nH Inductor (etching depth)	R_S (Ω)	L_S (nH)	C_o (fF)	C_i (fF)	C_S (fF)	F_{res} (GHz)	F_{Qmax} (GHz)	Q_{max}
Standard	30	12	65	50	10	5.3	3.1	5.1
8 µm	28	11.9	50	45	6	6.2	3.6	6.3
22 µm	29	12	31	29	6	7.6	4.4	7.5
42 µm	29	12	6	3	6	13.4	7.7	13.3

5.4.1 Design Considerations

Ideally, perfect magnetic flux linkage is assumed in the transformer structure. In other words, all the flux from the primary inductor links the secondary one as well. If the inductance of both windings approaches to infinity, the frequency response does not have low frequency limits. On the other hand, if the stray capacitance is assumed to be negligible, then the same response does not present upper limits either. With these assumptions, the transformer can be modeled as a simple voltage or current transformation, with the voltage and current ratios given by :

$$N = \text{turns ratio} = \frac{\text{secondary winding}}{\text{primary winding}} = \frac{I_{prim}}{I_{sec}} = \frac{V_{sec}}{V_{prim}} = \sqrt{\frac{Z_{out}}{Z_{in}}} \qquad (5.45)$$

where Z_{in} is the impedance seen into the primary when an impedance Z_{out} is imposed on the secondary. The coefficient of coupling (K) of two-winding coupled inductors is commonly used to describe how closely a transformer comes to being ideal, and represents the fraction of flux linkage from the primary coil that links the secondary one, or *vice-versa*. It is defined as :

$$K = M \,.\, (L_{prim}.L_{sec})^{-1/2} \qquad (5.46)$$

where L_{prim} and L_{sec} represents the self-inductances and M is the mutual inductance of the coupled inductors.

In fact, any non-ideal transformer has a limited bandwidth, even if parasitic capacitances are neglected. The usefulness of a transformer drops off at low frequencies because the inductive reactance of the windings becomes too low. At high frequencies, the reactance of the series inductors limits energy transfer. The value of K determines the size of these inductors and, with the self-inductance, the upper frequency of operation. Therefore, it is important to maintain the value of K as high as possible for a large bandwidth. However, in transformers where K is significantly less than 1 the turns ratio becomes meaningless, and rather the self and mutual inductances must be specified.

A simple, but yet accurate, lumped element model, proposed by Frlan et al. [48] and illustrated in Fig. 5.16b, has been adopted. In this equivalent circuit, R_p and R_s are the series resistance, while L_p and L_s are the total inductance of the primary and secondary, respectively. Since the structure is formed by identical spiral inductors, theses values are assumed to be equal for both coils. In turn, M represents the mutual inductance between the coils. Static self and mutual inductances between parallel segments are calculated according to the Greenhouse formulation [36], described above, assuming that perpendicular segments have negligible mutual inductances. The direction of current through the transformer dictates the sign of the mutual inductance between segments. Furthermore, the mutual inductance related to the fictional mirror image inductor from

the back-side ground plane must be taken into account for increased accuracy. The significant reduction in the net inductance is accounted for by the reverse current flow in the image.

Calculation of the segment-to-ground capacitance and the mutual interline capacitance can be realized using the method presented for planar inductors. The capacitance between non-adjacent lines are usually negleted with little effect in the final accuracy of the model, unlike the total inductance in which all the individual self-inductances must be considered. The variation in phase shift with frequency also produces a change in the effective mutual capacitance C_m, between the primary and secondary. The value of C_m at DC is effectively zero, but its influence on the device performance becomes significant with the increasing frequency of operation.

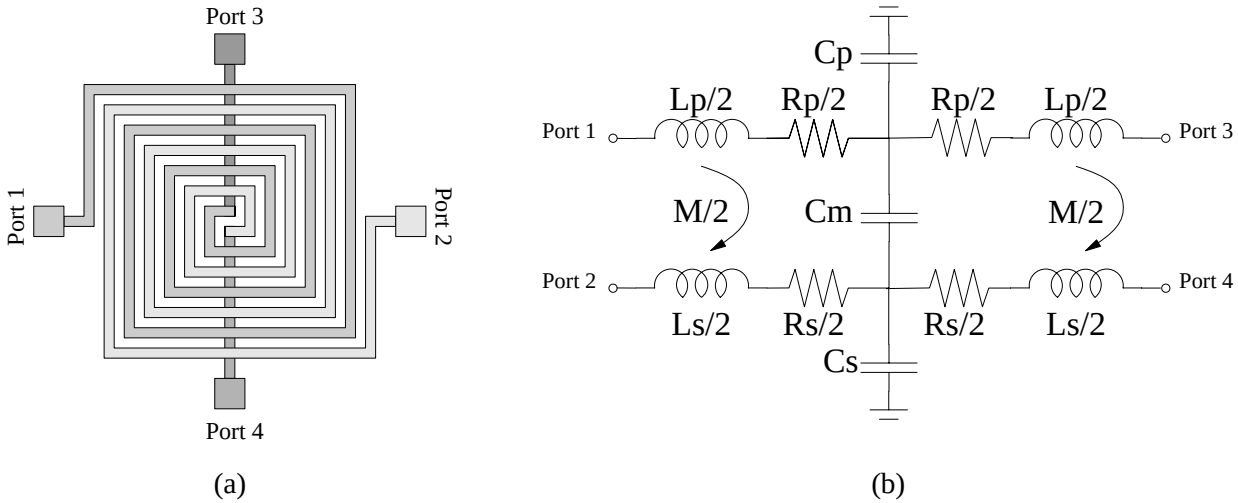


Fig. 5.16 - Planar spiral transformer: (a) structure and (b) lumped element equivalent model.

Overall, the most sensitive components in the lumped transformer model are M and C_m. If these equivalent circuit components are not carefully calculated, the resonant frequency response of the model is severely affected. The model is fairly insensitive to small variations of the self-inductances L_p and shunt capacitances C_p.

The free-standing transformer device proposed is composed by two coupled inductors with the strips suspended individually, as presented in previous section. Therefore, both shunt and fringing capacitances are expected to be drastically reduced, increasing the broadband operation. Notice that, the coefficient of coupling should not be influenced by micromachining since the GaAs substrate and dielectric layers (SiO_2 and Si_3N_4) are not considered as magnetic materials.

5.4.2 Experimental Results

A planar spiral transformer formed by two 7-turns coupled inductors, with 5 µm-width and 6 µm-spacing strips (i.e., open area width of 5 µm and margin distance of 0.5 µm between the metal line and the border of the bridge), was fabricated and etched, as shown in Fig. 5.17. Thin dielectric arms were place at the four corners of the three most external strips for mechanical support. The ports 3 and 4, according to Fig. 5.16, were conected to ground through via holes in order to simplify the characterization procedure, reducing the device to a two-port element.

The extracted element values obtained for an etching depth of 42 µm were $L_p=L_s=8.6$nH, M=6.8nH and $R_p=R_s=30\Omega$. Since the lowering in self inductance due to its own image spiral is 0.85 nH and the mutual inductance between one actual spiral and the image of the other is 0.8 nH, the ground plane effects on self and mutual inductances have to be taken into account for improved accuracy. Capacitances are strongly reduced with micromachining since $C_p=C_s=15$fF and $C_m=80$fF are obtained with the micromachined structure, whereas $C_p=C_s=40$fF and $C_m=200$fF were obtained with the standard transformer.

Measured data for a standard transformer and the micromachined structure are shown in Fig. 5.18. The lumped-element modeling approach using computed values agrees well with measurements, for both S-parameter magnitude and phase.

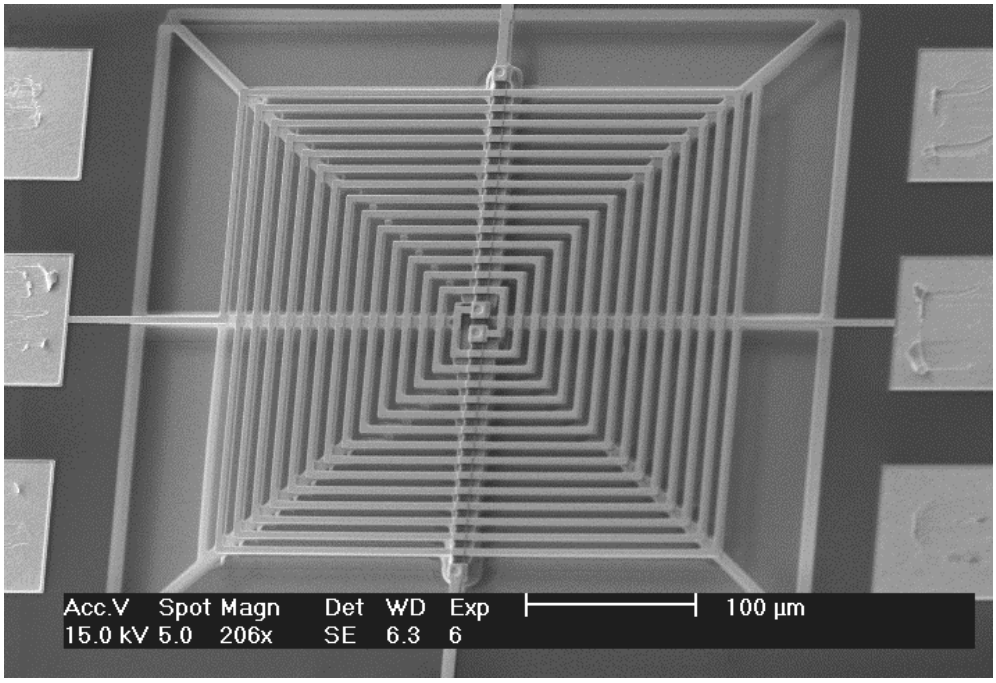
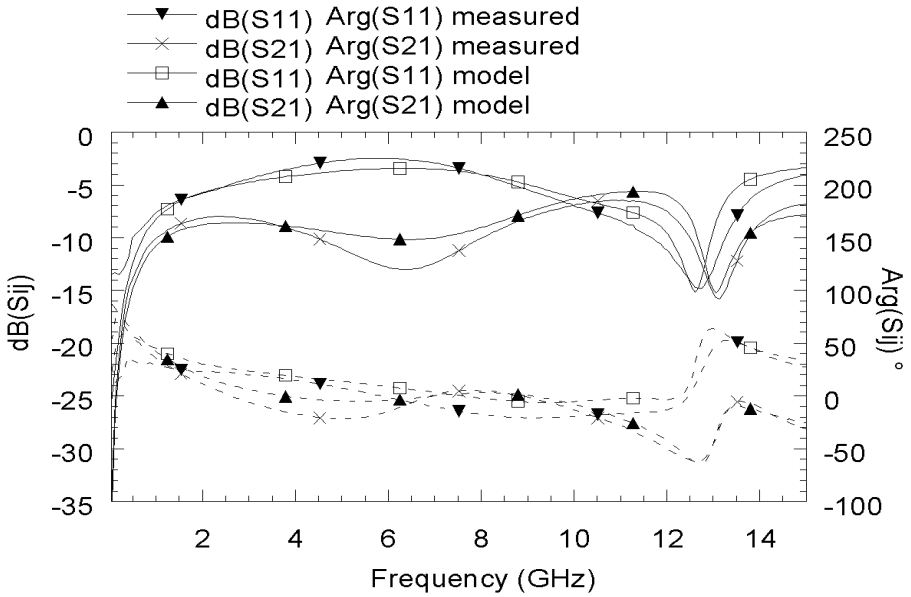


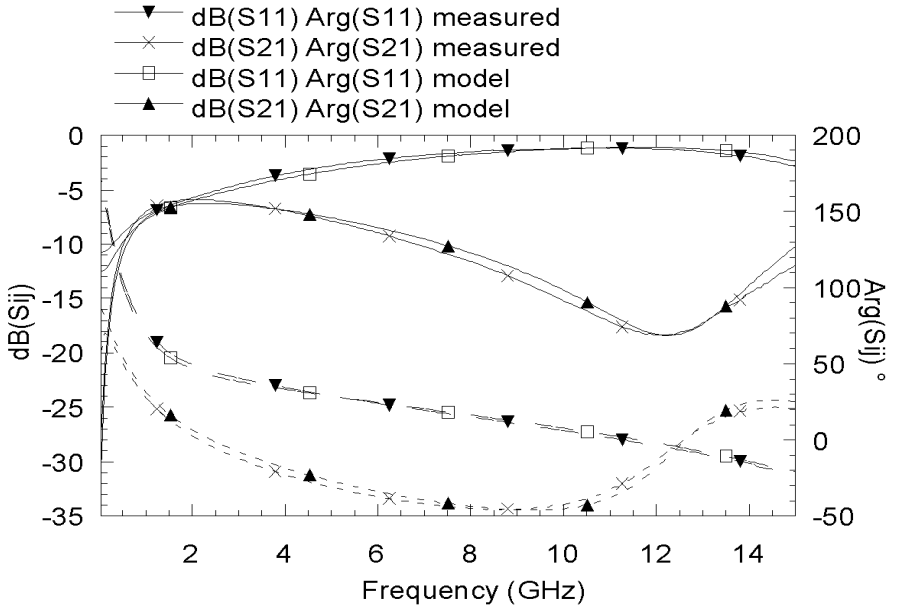
Fig. 5.17 - Microphotograph of micromachined planar spiral transformer.

Moreover, even if the transformer geometry was not optimized for a specific frequency band, a higher range of frequency operation has been demonstrated. For exemple, note that the

resonant frequency of the standard device is approximately 12 GHz (S11 parameter in Fig. 5.18a), while such frequency parameter has been shifted after 15 GHz in the micromachined transformer, as verified in Fig. 5.18b.



(a)



(b)

Fig. 5.18 - S-parameters from measures and lumped model : (a) standard and (b) 42 µm-depth suspended planar spiral transformer.

5.5 THERMAL AND MECHANICAL CHARACTERISTICS

Besides electrical performance, thermal and mechanical characteristics are also very important to verify the usefulness of these micromachined devices. A complete analysis of such parameters was carried out through extensive finit element method (FEM) simulations, using the ANSYS tool.

5.5.1 Heat Distribution

It is well known that free-standing structures have been widely used in thermo-electric based micromachined devices, such as bolometers and thermopiles, since suspended parts present a reduced heat dissipation, giving rise to as hot regions for temperature sensing or for Seebeck voltage generation, considering the substrate as a heat sink (cold region). However, in the case of suspended microwave passive devices it could represent an important constraint due to the increasing series resistance of the wires, which influence significantly the Q-factor of the device.

Although the electrical resistivity of both metals and semiconductors varies with temperature, the nature of their behavior is different. The temperature coefficient of resistivity (TCR) is given by :

$$TCR = (1/\rho_o)(\partial\rho/\partial t) \tag{5.47}$$

and for metals, in the approximately linear region, the resistivity ρ can well be described by a second order polynomial expression :

$$\rho = \rho_o (1 + a.T + b.T^2) \tag{5.48}$$

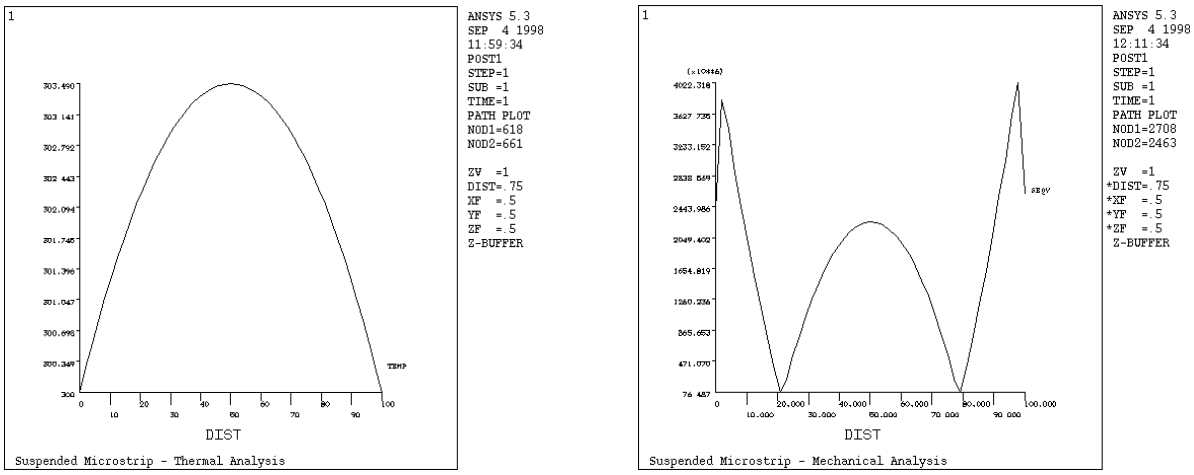
with T in degrees, and ρ_o the resistivity at a standard temperature of 0°C, while a and b are material constants. Therefore, the TCR value becomes :

$$TCR = a + 2.b.T \tag{5.49}$$

It must be observed that the material constant a represents the linear temperature coefficient of resistivity, and for metals it is positive and takes a typical value of approximately $5x10^{-3}$/K [49]. In other words, a temperature difference of 100 degree results in an increasing of about 50% in the resistance value.

At first, a single and straight suspended microstrip line with width equal to 5 µm was simulated considering the maximum current of 6 mA/µm given by PML for the interconnection metal (i.e., the worst case), which represents in this case a total current equal to 30 mA. The temperature distribution on a free-standing microstrip is shown in Fig. 5.19a, and the maximum temperature as a function of the bridge length is observed in Fig. 5.20a. Moreover, such behavior is almost independent of the line width, as presented in Table 5.2 for a 100 µm-length microstrip.

Moreover, both versions of planar spiral inductors, over a membrane and with isolated strips, were also investigated, but in this case considering the maximum sheet current of 3 mA/µm given for the center tap metal. The segment spacings and widths were equal to 9 µm. The maximum increasing temperature as a function of the number of spiral turns is shown in Fig. 5.20b. Note that, the heat dissipation is higher in the membrane structure. The temperature distribution for both cases is illustrated in Fig. 5.21.



(a) (b)

Fig. 5.19 - Temperature (a) and mechanical stress (b) distribution on a suspended microstrip line.

Furthermore, in small structures and normal environment conditions, convention and radiation dissipations are commonly negligible in respect to the thermal conduction and were not taken into account in this investigation.

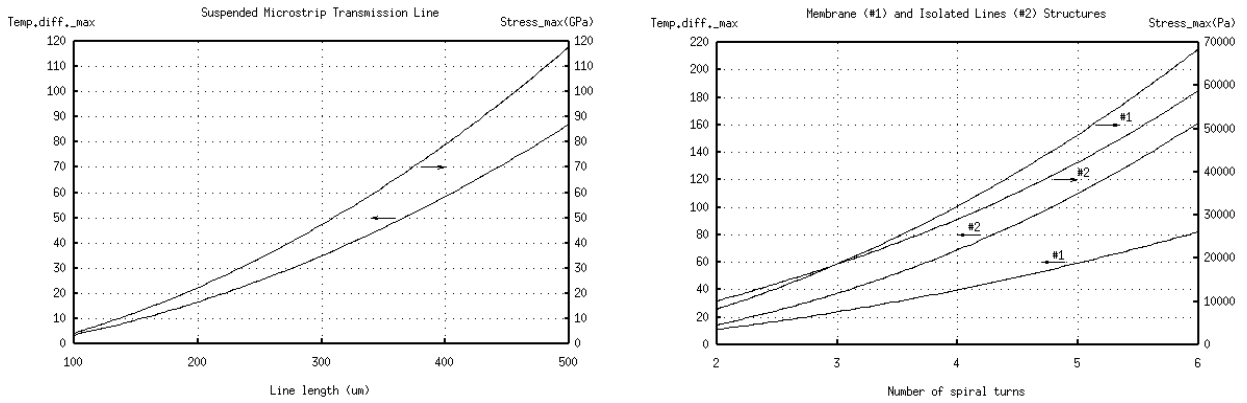
TABLE 5.2 - Thermal and mechanical characteristics for a 100 µm-length suspended microstrip as a function of the width.

Line width (µm)	ΔT_{max}* (°C)	Max. stress** (GPa)	Max. displacement** (µm)
5	3.49	4.28	3.72
10	3.51	4.61	3.88
15	3.51	4.65	3.91
20	3.51	4.65	3.92
25	3.52	4.60	3.93
30	3.52	4.57	3.94

* Using the maximum current of 6 mA/µm.
** Using an acceleration of 100g.

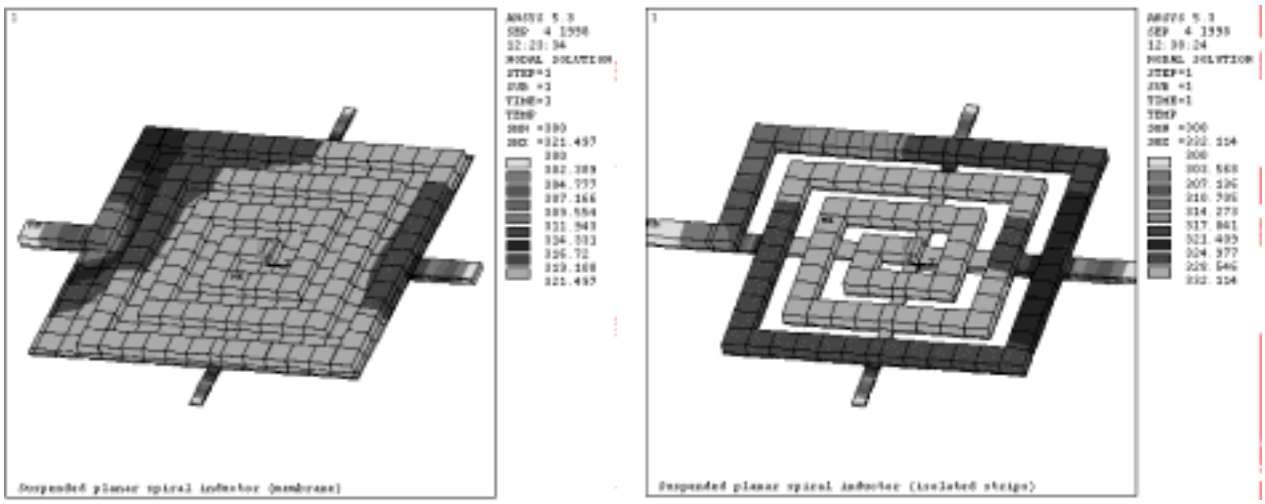
5.5.2 Mechanical Stress

For mechanical evaluation, an acceleration of 100g (i.e., 980 m/s^2) was considered in the FEM simulations. To have an idea of such acceleration value, airbag accelerometers for automotive systems work at a range of ±50g [50]. In Fig. 5.20b is illustrated the mechanical stress distribution on a straight suspended microstrip, while in Fig. 5.20a the maximum stress is shown as a function of bridge length. Similarly to the temperature behavior, the maximum stress as well as the maximum displacement were also observed approximately invariant in respect to the structure width, as presented in Table 5.2.



(a) (b)

Fig. 5.20 - Maximum temperature and mechanical stress on: (a) microstrip and (b) planar inductor.



(a) (b)

Fig. 5.21 - Temperature distribution on planar inductors: (a) over membrane and (b) with isolated strips.

In the case of planar inductors, considering the same dimension used in the thermal analysis and always an acceleration of 100g, the maximum mechanical stress is observed in the dielectric arms of the structure, and it is represented in Fig. 5.20b, as a function of the number of spiral turns, for both membrane and isolated strips approaches. It is interesting to note that SiO_2 presents the

lowest fracture strength (50-55 MPa) among the structure layers. That is, according to the values obtained, the inductor structures seems to be mechanically very robust, while the use of suspended microstrip lines may need to be carefully verified for certain applications. In any case, it is suggested to use dielectric arms at four corners for larger spiral structures. Finally, note that the internal stress between the layers in the IC process are very critical in some structures and they have not be taken into account in this simulation.

5.6 CONCLUSIONS AND SUMMARY

The front-side bulk micromachining compatible to a standard GaAs HEMT technology, investigated in this work, has been demonstrated to be very useful for performance improvement of micromachined microwave passive devices, in particular planar spiral inductors and transformers. The promising results presented, associated with the fact that the D02AH process from PML is already available to MMIC design, represent a significant advance in RF circuits, such as filters, matching networks and low-noise amplifiers.

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Chapter 6
CAD TOOLS FOR MEMS

Computer-aided-design (CAD) tools must bridge the gap between microsystem designers and foundry facilities. Since existing microelectronics CAD tools include a number of features useful for MEMS design, especially when IC-compatible microsystems are addressed, then it is mandatory that such tools are extended to microsystems rather than developing completely new and specific CAD environments. In this chapter, the use of a fictitious layer, named 'open area', is proposed to efficiently check the dielectric opening design rules for both micromachining and electronic circuits. A computing program which is used to convert such open areas to 'real' layers (contacts, vias and passivation openings) has been developed. Moreover, a set of tools related to the back-end design flow (layout and post-layout level) is presented, including layout generators for micromachined and electronic devices, cross section and 3D layout viewers, and bulk etching simulators for surface and vertical profiles. These tools are independent of the technology and have been developed specifically for the Mentor Graphics environment, using the AMPLE language. Such facilities are described herein taken into account the PML GaAs HEMT ED02AH process.

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6.1 INTRODUCTION

In order to boost microelectronics development, multi-project wafer services have provided access to IC foundries for chip prototyping and small volume production. The basic idea of a multi-project chip or wafer (MPC - MPW) is to collectively process circuits that are different and dissimilar, sharing the high fabrication costs. MOSIS in USA, CMC in Canada, CMP in France and PMU in Brazil are examples of MPC services for ICs available at a national level [1]-[3]. Similarly, to serve their customers for prototyping, manufacturers, such as AMS and TRW, often organize an internal prototyping service.

Nowadays, the same strategy of collective fabrication starts to be applied to microsystems, for both specific manufacturing processes and microelectronics-compatible micromachining approaches. The Multi-User MEMS Processes (MUMPs) is an example of a program that provides the industry, government and academic communities with a specific, cost-effective and proof-of-conception surface micromachining fabrication [4]. In the case of microsystems manufacturing on existing microelectronics production lines, ICs containing micromachined and electronic devices are possible because the suspended structures are commonly released by using a maskless post-process wet etching at die level, without modifying the standard IC fabrication, as illustrated in Fig. 6.1 [5][6].

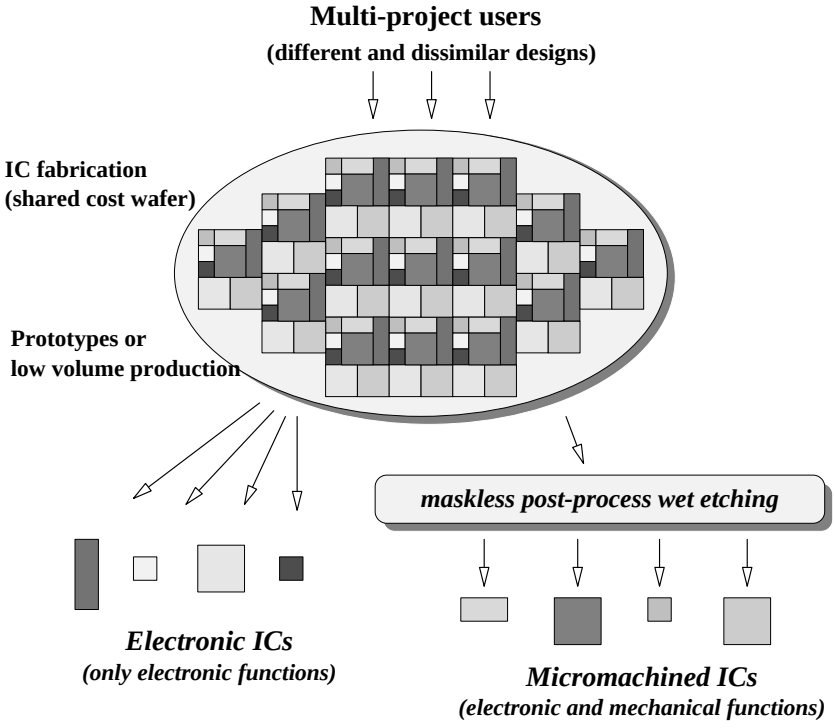


Fig. 6.1 - Multi-user project service for electronic and microsystem circuits.

On the other hand, high-level computer-aided-design (CAD) tools must bridge the gap between microsystem designers and foundry facilities, in order to support a non-specialized system-level designer who wants to combine micromechanical and electronic parts in a new microsystem. Since, MPC services are provided to microsystems design using standard IC technologies, a single CAD environment and design-flow for the whole layout construction is highly desirable, such as proposed in Fig. 6.2. Ideally, CAD tools for MEMS should include schematic capture, multi-level modelization and simulation (etching mechanisms, finite element method - FEM, analog hardware description language - HDL-A, etc.), automatic layout generation and extraction, back-annotation, and so on [7]-[9]. Certainly, there is still much to do. Fortunately, available modules can be reused, extending existing commercial microelectronics CAD tools. Currently, IC design environments, such as Cadence DF2 and Mentor Falcon Framework, need modifications before they can be used for the automated design of microsystems.

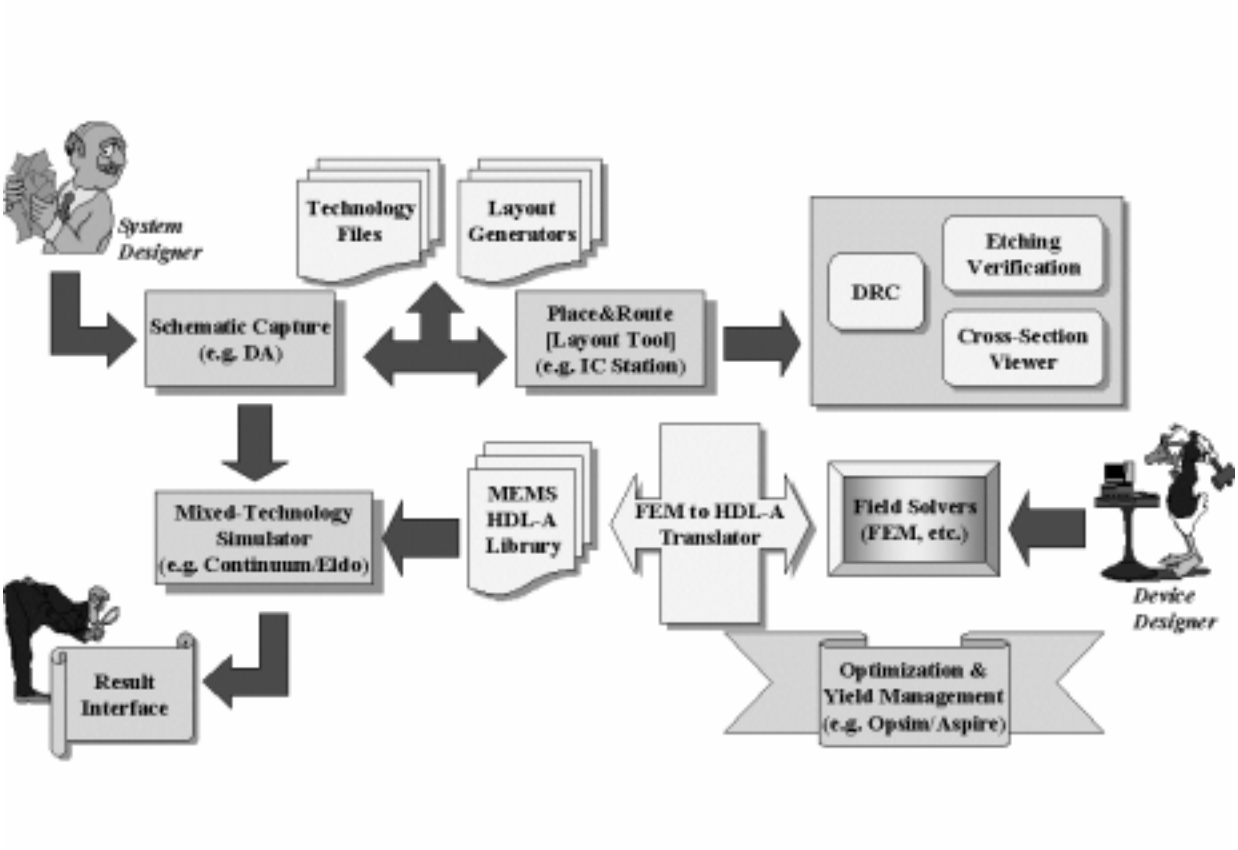


Fig. 6.2 - CAD environment for MEMS design.

In the context of this work, a set of tools, related to the layout and post-layout levels (back-end design flow), have been developed on the Mentor Graphics environment. In 1997, the TIMA laboratory spinned-off a commercial company, MEMSCAP, a partner of Mentor Graphics Corp. for CAD of MEMS. These tools are independent of the technology, and they have been configured and validated considering the PML ED02AH process [10]. Such facilities as well as the

micromachining design rules are included in the GaAs MEMS engineering kit available through the first MPC service for GaAs microsystems in the world, provided by CMP.

This chapter initially presents the strategy adopted to check, at the same time, electronic and micromachining layout design rules using the fictitious 'open area' layer. Moreover, layout generators for generic structures and specific applications have been developed to optimize the time spent in the layout construction and to help non-specialized designers. Next, the cross section viewer and the layout three-dimensional solid model generation are presented. In terms of etching verification two tools related to the bulk etching are described, i.e., an isotropic etching preview for surface profile and a two-dimensional etching simulator for vertical profile. All these tools have been developed using exclusively the AMPLE language of Mentor Graphics. Finally, the conclusions and future perspectives are briefly discussed.

6.2 DESIGN RULES CHECK (DRC)

The purpose of the design rules is to ensure the greatest possibility of successful fabrication with acceptable reliability. The design rules are a set of requirements and advicements that are defined by the limits of the process and characteristics of the etchants. Mandatory rules are given to ensure that the layout remains compatible with lithographic process tolerances. Violation of minimum spacing rules, for instance, can result in missing, undersized, oversized or fused defects. Notice that the minimum geometries allowed should not be confused with the optimal geometries recommended. Furthermore, advisory rules are associated with the correct construction and performance efficiency of the structures, e.g., the layout orientation is a crucial factor in the design of GaAs free-standing triangular prism-shaped bridges.

As mentioned, it is very useful to follow a single and complete microsystem design flow without considering separately mechanical and electronic parts. Therefore, the first and elementary task is to provide the layout construction and correspondent design rules check (DRC) for MEMS design using the same CAD environment. However, the superposition of contacts, vias and passivation openings required to create the open regions is commonly prohibited by IC foundries, resulting consequently in design rules violation. Moreover, the widths and spacings of dielectric openings for micromachining purposes are somewhat different from that used in the electronic circuitry. In order to avoid such drawback, a fictitious layer, named 'open area', has been used to define the uncovered substrate surface regions rather than superpose dielectric opening layers [6].

Thus, by definition, the open area layer represents the stack of all dielectric openings created during the IC fabrication and that are necessary to expose the substrate surface areas for the

post-process etch attack, as shown in Fig. 6.3. It can correspond to only two layers, as in the case of the PML (E)D02AH processes (open area = *CO* + *CB*), or more, as occur in the Vitesse H-GaAs III process where it is equivalent to six layers (open area = *active_area + via_1 + via_2 + via_3 + via_4 + passivation opening*) [10][11]. As a result, unlike presented in the CMOS approach by J. M. Paret [12], the micromachining rules are reduce to a few ones, illustrated in Fig. 6.4, and they are not mixed with the microelectronics design rules.

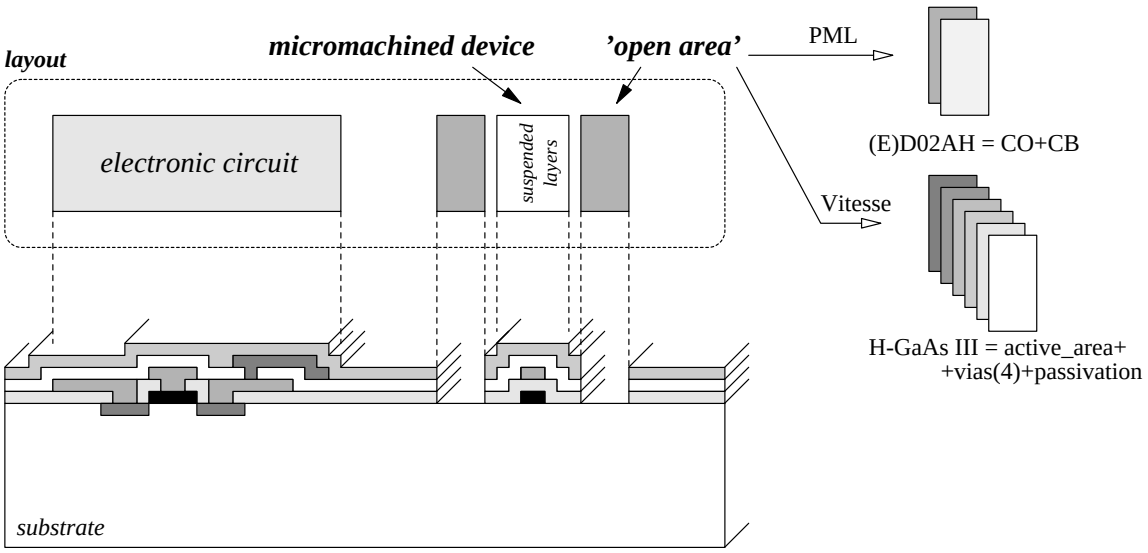


Fig. 6.3 - Representation of the fictitious open area layer.

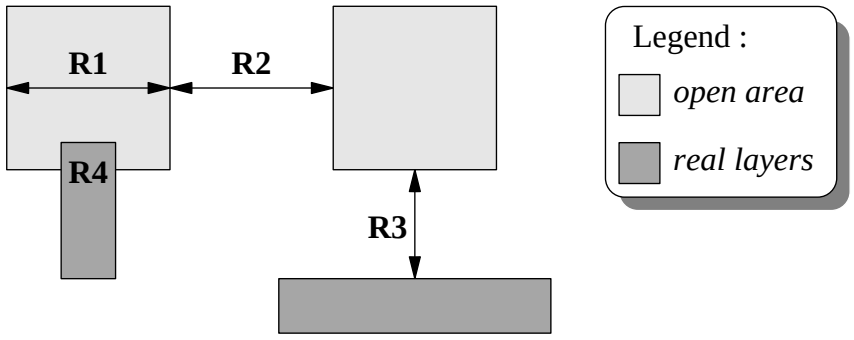
Furthermore, even if the stacking procedure is realized by considering distances of enclosure between the layers, as proposed by J. M. Paret [12] for CMOS micromachining using the ATMEL-ES2 ECPD10 process, these overlaps can be easily taken into account during the open area conversion to electronic ('real') layers. In this case, the open area usually corresponds to the most internal layer and a minimum spacing between the open area and the real layers must be respected to avoid eventual superposition errors caused by overlapping of the most external dielectric opening and the electronic layout. A converter tool to generate the set of real layers (dielectric openings), with appropriate enclosure, from open areas and vice-versa was developed. It seems obvious that the task of the designer and the time spent in the layout construction to design the open regions are significantly improved, as well as the layout presentation becomes much clearer. The open area layer is also very useful for layout generators and other MEMS tools, as presented later.

Differently from purely electronic ICs, where usually only process restrictions determine the respective design rules, such a set of layout rules for microelectromechanical circuits can be divided in three types of rules :

General rules — These rules are associated with the IC process step limitations (lithography), such as the minimum open area width required to avoid residual layers, as discussed in Chapter 3, and the minimum open area spacing to prevent possible fusions. Moreover, the distances between the open area edges and other layers are also included, observing that, by definition, superposition of the fictitious open area and real layers are not allowed. A representation of these general rules is shown in Fig. 6.4, where the values are only illustrative. The correct rules vary according to the target process and they are restricted to CMP users.

Number	Description of the design rules	Value
R1	minimum open area width	8.0 µm
R2	minimum spacing between open areas	6.0 µm
R3	minimum spacing between open area and real layers	2.0 µm
R4	no real layer must overlap the open area	-
R5	all open area edges must be 45° angles or multiples	-
R6	layout grid for the open area	0.5 µm

(a)



(b)

Fig. 6.4 - General micromachining design rules: (a) description and (b) illustration.

Specific rules — They refer to particular structures and the respective etching solution applied. For instance, the maximum etching time for a specific etchant must be respected to avoid possible damage in the unconcerned surface layers. As a result, the maximum distance allowed between open areas to create bridges, membranes or other geometries (structure width) is determined by the multiplication of such maximum etching time and the underetching rates. In this group can also be included the crystallographic directions of the structures for anisotropic etching, the selectivity of the etchants, and the depth etch rates of each solution. Such a kind of rules is commonly verified using etching simulators.

Mechanical rules — These are associated with mechanical characteristics of the suspended structures, e.g., the maximum length of bridges and cantilevers, the arm dimensions in membranes, and so on. They are the most difficult ones to be determined due to the variety of structures, shapes and materials considered. For this, a large set of test structures, as well as extensive mechanical characterization and the designer experience are important. Nevertheless, FEM simulations could

give a good idea of such limits, even if heterostructures fabrication mismatches and intrinsic surface stresses are not taken into account.

6.3 LAYOUT GENERATORS

In order to optimize the design time and provide the correct-by-construction layout generation, i.e. the design rules are respected during this task, three kind of pre-designed layout cells are commonly used : pre-characterized full custom cell libraries, generic parametrized functional blocks, and/or layout generators. In the first case, pre-designed and pre-characterized cells, representing specific devices and circuits with well known functionality and performance, are available in libraries to be re-used when ever necessary. The library of parametrized cells, on the other hand, corresponds to generic structures whose particular layout geometry dimensions can be easily modified, such as widths and lengths, as proposed for micromachined structures by J. M. Karam [13]. This approach is more flexible than pre-characterized cell libraries in terms of the layout construction, but less information is available about the performance.

Layout generators, in turn, were firstly thought for particular digital circuits that present regularity and symmetry in the layout representation, such as memories (RAM and ROM), programmable logic arrays (PLA) and arithmetic function blocks (adders and multipliers). In the last years, IC CAD tools for layout edition have been improved in order to provide such a kind of generators, but also specific in-house computing languages have been made available to create personalized functions and layout generators. Ample and Skill languages from Mentor Graphic and Cadence environments, respectively, are examples of these facilities, which allow the designer to use layout edition commands, such as *move*, *copy*, *delete* and other ones, for automatic layout construction. In this approach, other parameters than the geometry dimensions associated with the layout can also be determined interactively by the user, e.g., the number of gate fingers of HEMT transistors, the passive component values, etc.

Keeping this in mind, layout generators for generic micromachined devices (bridges, cantilevers and membranes) and particular MEMS applications (bolometers, thermopiles and AC-DC converters) have been developed within the Mentor Graphics environment, using exclusively the Ample language, as illustrated in Fig. 6.5. One of the main advantage of these tools is that non-specialized designers are able to create fast and efficiently new microsystems. Although the PML GaAs HEMT ED02AH process has been targeted, both principle and technique presented herein are easily extended to other technologies. Besides micromachined devices, generators have also been created for the electronic compounds provided by PML, such as HEMTs, inductors and so on.

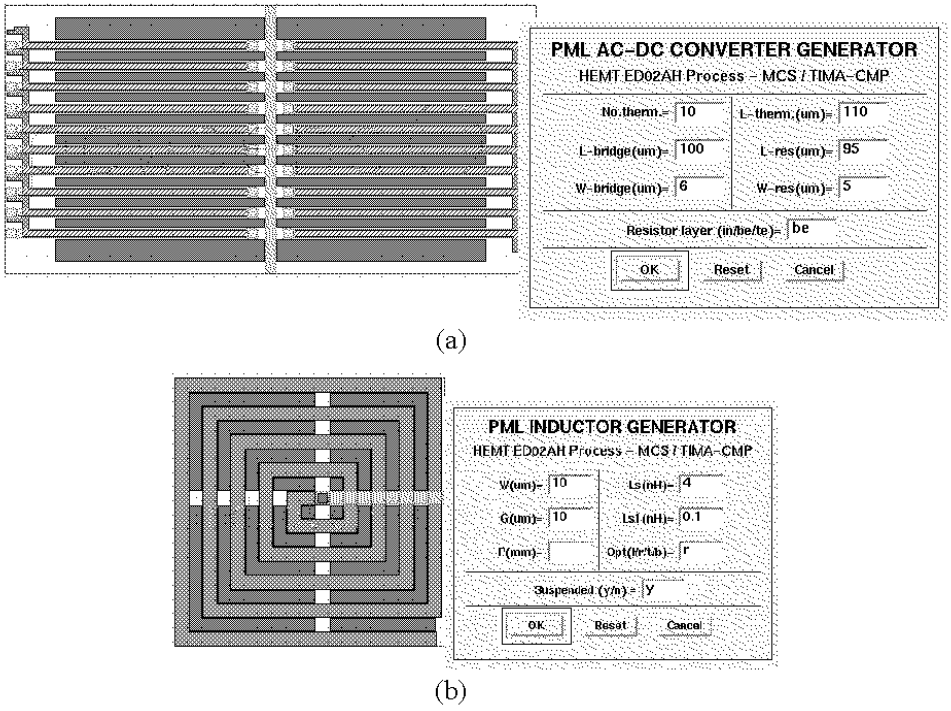


Fig. 6.5 - PML HEMT layout generators : (a) AC-DC converter and (b) planar spiral inductor.

The variables used in the layout generators are divided in two groups: *layout arguments* and *technology variables*. The layout arguments are entered in the dialog box (see Fig. 6.5) and correspond to geometry parameters defined by the designer, such as the number of elements and their dimensions. Technology variables, on the other hand, are associated with the minimum and maximum values from the process design rules, as well as the default values considered when the layout arguments are not given. The technology variables are described through a text file (ASCII format) and are responsible for the correct-by-construction layout, since they are taken into account always when out of range values are entered in the dialog box (see Fig. 6.6). If a certain layout dimension is not defined as a layout argument or as a technology variable, it means that it is determined in the source of the program and cannot be changed by the designer.

Note that, the layout generators are also very useful for the automatic layout synthesis using SDL (Schematic Driven Layout). In this case, they are associated with device symbols in the schematic description entry and/or with hardware description language (HDL-A) packages [14]. Moreover, since new devices and applications are constantly being fabricated and characterized, the development of layout generators becomes a continuous task similarly as new layouts are included in pre-designed cell libraries. The MEMS library proposed by TIMA intends to include a symbol for schematic description, HDL-A model, layout generator and experimental data for each device and circuit available.

```
////////////////////////////////////////////////////
//////
// MCS Group - TIMA/CMP ;  Variables for Layout
Generators //
//               PML MMIC HEMT 0.2um (ED02AH)
//
////////////////////////////////////////////////////
//////

/// AC-DC Converter
extern user_ic_session@@nt_default = 5;
extern user_ic_session@@wb_default = 10;
extern user_ic_session@@lb_default = 50;
extern user_ic_session@@lt_default = 60;
extern user_ic_session@@lr_default = 10;
extern user_ic_session@@wr_default = 5;
extern user_ic_session@@th_co = 2;
extern user_ic_session@@th_mg = 0.5;
extern user_ic_session@@th_sp = 3;

/// Microstructures
extern user_ic_session@@wop_default = 20;
extern user_ic_session@@wbr_default = 20;
extern user_ic_session@@lbr_default = 50;
...
```

Fig. 6.6 – Definition of technology variables for layout generators.

6.4 LAYOUT VIEWER TOOLS

Although each layer shape in the layout corresponds to a particular step in the IC fabrication, it is frequently not obvious for the designer to understand the influence of such layers in the process. For this, cross section views realized on the layout and the representation such the layout in a three-dimensional form appear to be very helpful. Such a kind of viewing tools can also be used for purposes other than just visualizing the layers arrangement in the vertical direction. For example, the cut view can be efficiently used as the graphical interface to show physical simulation results, such as layer etching, current distribution and heating dissipation, while a 3D layout representation could be used for solid model FEM simulation.

6.4.1 Cross Section View Generation

In the literature, a cross section illustration of the wafer or circuit is normally used to describe IC processes, as well as the operation principle of semiconductor compounds and their related physical phenomena. Therefore, it seems very interesting to have a tool that shows a cross section view from a cut line defined on the layout. In the case of micromachined devices, it is even more useful because the suspended substrate portions or layers could be observed, as discussed later in section 6.5.2. Furthermore, it could also be used as the output graphical interface of physical and electrical simulators, such as the electro-thermal behavior giving by the SISSI tool [15] and the current density distribution resulting from magnetic fields [16].

The cross section viewer tool, developed on the Mentor Graphics environment, allows cutting a layout representation in any direction and visualizing in scale the correspondent layers of the process, since the real thickness ratios are respected in the tool configuration file, considering a micron equal to an unit distance in the layout editor. This tool is easily configured for different IC technologies, and it has been validated in the context of this work for the PML ED02AH process, which presents some particularities such as the mesa structure, back-side metal plane and via holes (see Fig. 6.7).

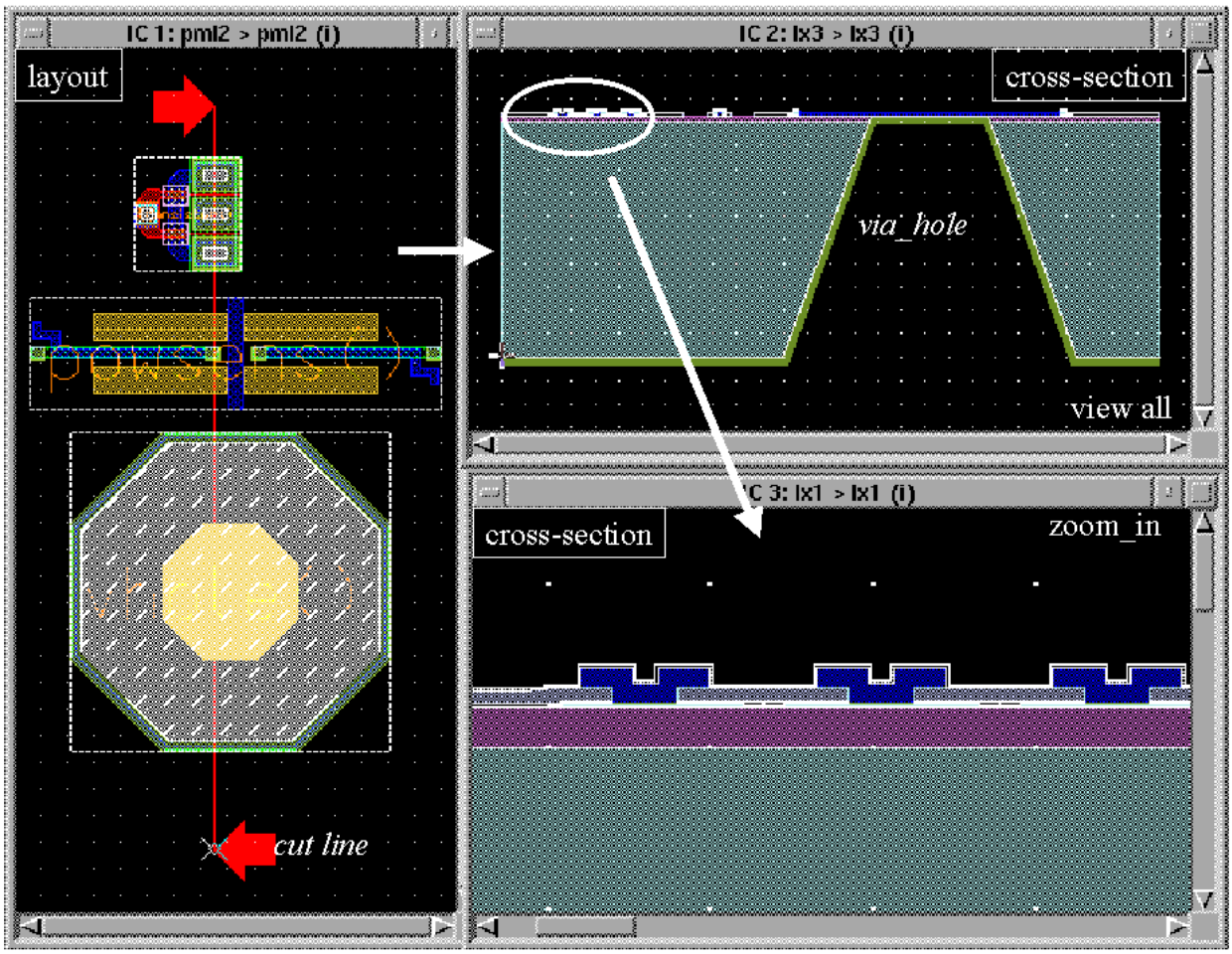


Fig. 6.7 - Cross-section viewer tool.

It was entirely developed using the AMPLE language. After the definition of the cut line in the layout window, all intersected layers with this line are extracted, that is, their distance to the cut line origin and their widths, using the AMPLE command *$get_compose_layer_selection()*. Such information is then transferred to a new IC Station window, where the layers are designed over a substrate, respecting the width, position and thickness distance of each intersected layer from the layout. The width of the substrate shape corresponds to the cut line distance.

Note that each layout layer or a particular set of layers are involved in cross section layer construction. Layout layers must be identified if they are positive or negative masks in the IC fabrication to determinate the presence of the respective cross section layer in or out of the intersected area. For eventual back-side steps, the same principle is used. Note that, since the cross section view is shown using a layout window of an IC Station, all editor commands, such as *zoom_in*, *zoom_out* and *view_area*, are available for detailed visualization. Finally, a special procedure was created for surface relief construction.

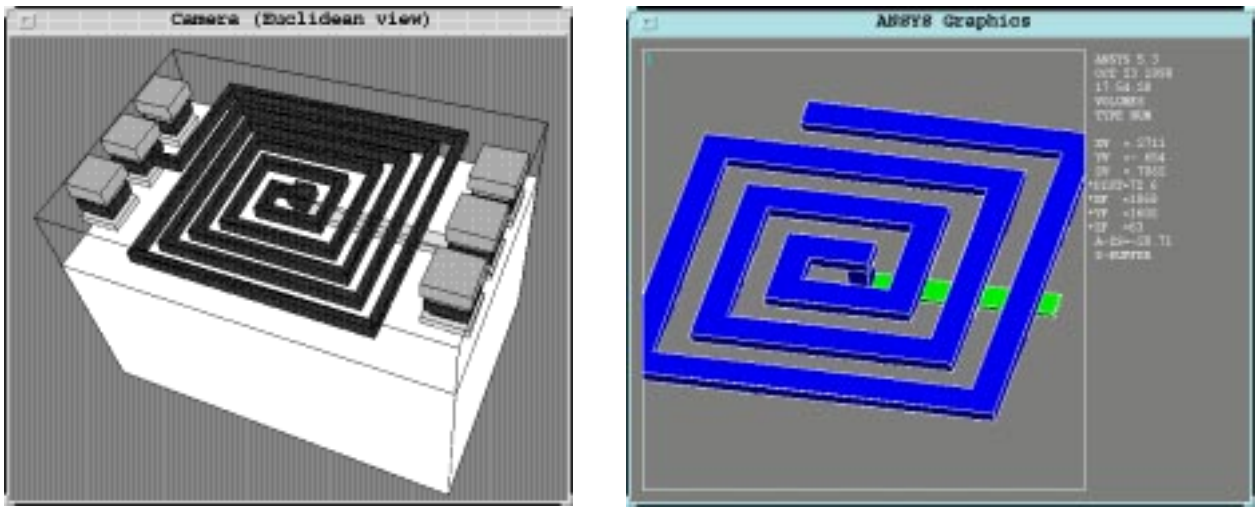
6.4.2 Layout 3D Solid Model Generation

The three-dimensional representation of a circuit layout, with the addition of the thickness value for each layer shape, helps designers, researchers and students to understand the IC fabrication procedure with the respective arrangement of layers and to investigate physical phenomena associated with the structure. In particular for MEMS design, such 3D illustration can also be used for solid model generation required in FEM simulation. In addition, it should be considered to provide an automatic mesh generation for the structure, which is a very time consuming task for FEM simulation, but this is not yet available in the first version of this tool.

The technique applied herein consists of extracting the layout coordinates from the IC Station window and creating volumes (prism shapes) with appropriate thickness and bottom side height. In this method, all layers are flat, that is, the relief observed in fabricated circuits is not observed here, as illustrated in Fig. 6.8. Although this characteristic of the 3D layout representation seems to be far from the real device construction, it is usually the strategy adopted in FEM analysis. Moreover, as the thickness values are commonly much smaller than the 2D layout circuit dimensions, sometimes the 3D visualization is somewhat compromised. To solve this, multiplication factors can be applied to all three structural dimensions by the user in a tool dialog box. Furthermore, only certain layers can be selected for extraction and visualization if the other ones are not desired.

Since the Mentor Graphics environment does not provide graphical windows for 3D visualization, other appropriate tools are required. At the moment, three type of output description file formats are available : ANSYS, X3d and Geomview. ANSYS is a FEM simulator which utilizes a specific description language, while X3d and Geomview are freewares 3D viewers that accept ‘obj’ and ‘coff’ description formats, respectively. Particularities have been found in these 3D tools, for example, shapes with internal holes or closed paths are not accepted by ANSYS, and are not correctly showed by Geomview. But such kind of troubles can be avoided by using the volume subtraction feature in ANSYS, while a special computing program that converts the volume

to a set of triangular prisms must be run before a 3D layout visualization with Geomview.



(a) (b)

Fig. 6.8 - Layout 3D solid model extracted from IC Station window : (a) Geomview and (b) ANSYS.

6.5 ETCHING VERIFICATION

As discussed in Chapter 3, the wet etching removes bulk material and creates a depression in the surface which grows both in normal direction to the surface of the die (etching depth) and laterally (underetching). In fact, the underetching is the principal responsible for the suspension of microstructures by using front-side bulk micromachining. Hence, since a maximum etching time must be respected during the post-process step in order to avoid undesirable damage on the surface layers of the circuit (passivation and pad metallization layers), the maximum structure widths are determined by the respective underetching rates.

Because usually the etchants of interest are anisotropic, the rates of the material etching are different for the various directions, that is, some crystallographic planes are etched very fast while others actually act as etching stop planes. Anisotropic etching relies on the fact that in all crystalline structures the atomic bonds in some planes are more exposed than in others. Assuming the presence of a homogeneous crystalline material with a constant orientation of its lattice, during the etching procedure a planar face is etched away parallelly to itself at a rate that depends only on the face orientation. Such etch rates, measured normally to the actual crystal surface, are described conveniently in a polar plot, where the distance of the diagram values from the origin of the coordinate system indicates the etch rate for particular normal directions.

The behavior of anisotropically etched crystalline materials is commonly modeled using

well-known geometrical methods, which do not require deep knowledge about the etching mechanisms [17]-[20]. Such methods assume that the etch rates are time independent, only depend on the crystal orientation. An etch rate polar diagram is then available. At the moment, it represents the most efficient technique to predict the releasing of micromachined structures. Another very promising line of investigation to predict the anisotropic etched shapes is based on the atomic scale model, which takes into account the dependency of etching speeds in terms of crystalline orientation, concentration of etching solution, temperature and doping concentration of etched substrates [21][22]. This approach is much more accurate but also more complex to be implemented.

6.5.1 Surface Isotropic Etching Preview

The surface etched shape, resulting from an original polygonal (mask) shape, corresponds to the underetching, i.e., the intersection of the crystallographic planes with the surface plane. Such etched shape is easily observed using an optical microscope, as shown in Fig. 6.11c. Even if etching prediction by means of geometrical methods are more easily implemented than atomic models, it is not really a straightforward technique because certain faces may appear while others disappear crystallographic planes are advancing [19][20].

A two-dimensional anisotropic surface etching simulator, named ACESIM, has been developed at TIMA laboratory [14]. It has proven to be very useful for CMOS micromachining using EDP (a watery solution of ethylenediamine and pyrocatechol) and KOH (potassium hydroxide in water) etchants. As illustrated in Fig. 6.9a, the surface etch rate polar diagrams present a wide range of values [12]. However, when isotropic etching is performed or the anisotropic behavior is only slightly observed, the etch rate diagram tends to a circular shape, as in the case of GaAs micromachining using citric acid based etchant (see Fig. 6.9b). Then, the simulation computing time increases significantly due to the large number of faces that appear and disappear during the process. It becomes even more critical for circular etching masks. In fact, in this case, since the dislocation of planes is similar in all directions, the final surface etched shape could be easily predicted by just ‘resizing’ the mask shape according to the etching time and underetching rate.

Therefore, a surface etching preview tool for fast evaluation has been implemented based on a simple method of scaling the open areas. The user defines the start time, step time, number of previews (pseudo-simulations), and the region containing the open areas to be evaluated, as shown in Fig. 6.10. An option parameter is used to take into account the highest and the lowest rates, i.e., the fast and the slow etching cases, respectively. Fig. 6.11 shows a comparison between the etched

shape resulting from the surface preview, the anisotropic etching simulator ACESIM, and the actual etching result. Such tool is also very useful for fast simulation of the etching impact on the unconcerned electronic blocks.

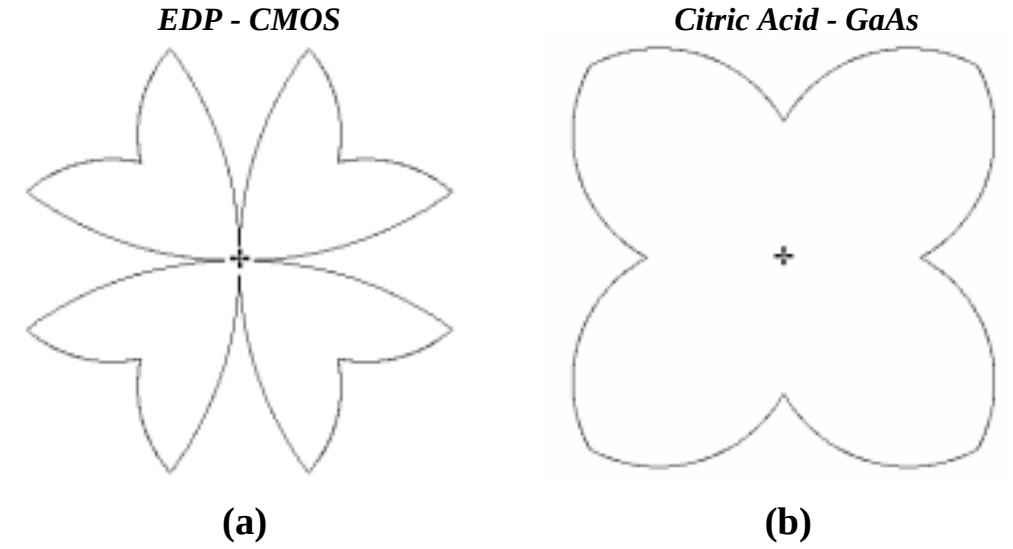


Fig. 6.9 - Surface etching rate polar diagrams: (a) CMOS-EDP and (b) GaAs-citric acid.

6.5.2 Bulk Etching Simulator for Vertical Profile

Even though the intersection of the etched bulk region with the substrate surface plane can be efficiently predicted through 2D surface etching simulations, as discussed above, in some cases such information is not enough to guarantee the complete suspension of the microstructure and its correct functionality. For instance, as illustrated in Fig. 6.12, the GaAs triangular prism-shaped bridge is obtained before the merging of the surface etched shapes takes place. In fact, when this happens the triangular mass underneath the bridge was totally removed because of underetching. On the other hand, CMOS micromachined bridges are released when the fusion of surface etched shapes occurs. However, an unexpected and undesirable bulk material mass of a pyramidal form could be left under the structure, causing bad functionality of the micromachined device. In both examples a view of the vertical profile is required.

A two-dimensional etching simulator to predict the vertical profile of the etched region has been implemented taking into account an algorithm based on the Wulff-Jaccodine geometrical method, which considers the crystal as a set of crystalline planes, each plane being etched at a specific rate (etch polar diagram) [23]. Considering Fig. 6.13, the points P1 and P2 represent the limits of the etching mask. The origin of the etch rate diagram is placed at P1 and P2, the left side of the diagram being taken for P1, the right side for P2. Vectors normal to the rate vectors D are

then drawn, and they represent in fact potential crystallographic planes. The predicted shape which results from the etching process is then defined by an envelope-of-normals, which consists of all normals or portions of normals that may be reached from the origin without intersecting any others [17][18].

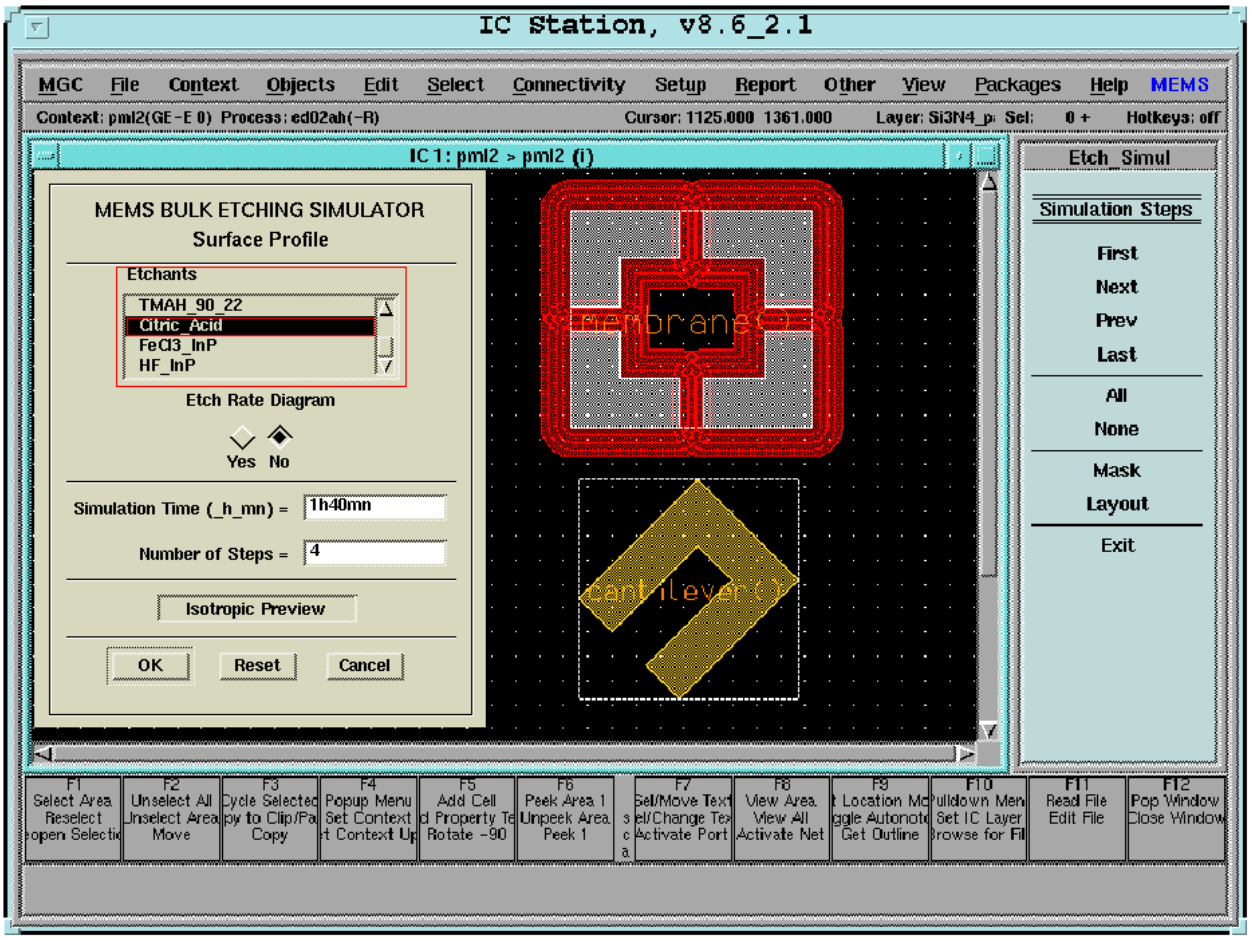
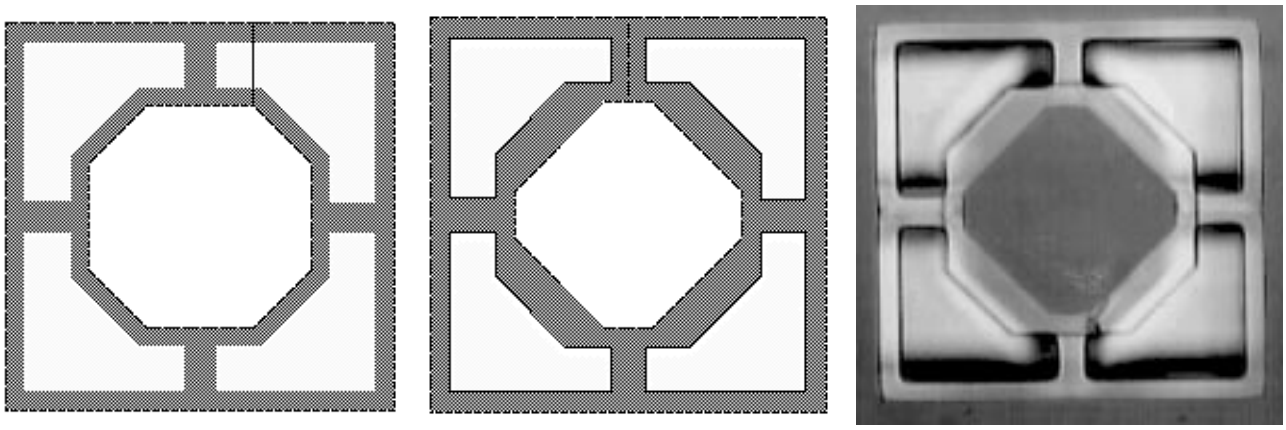


Fig. 6.10 - Surface etching preview tool illustration.

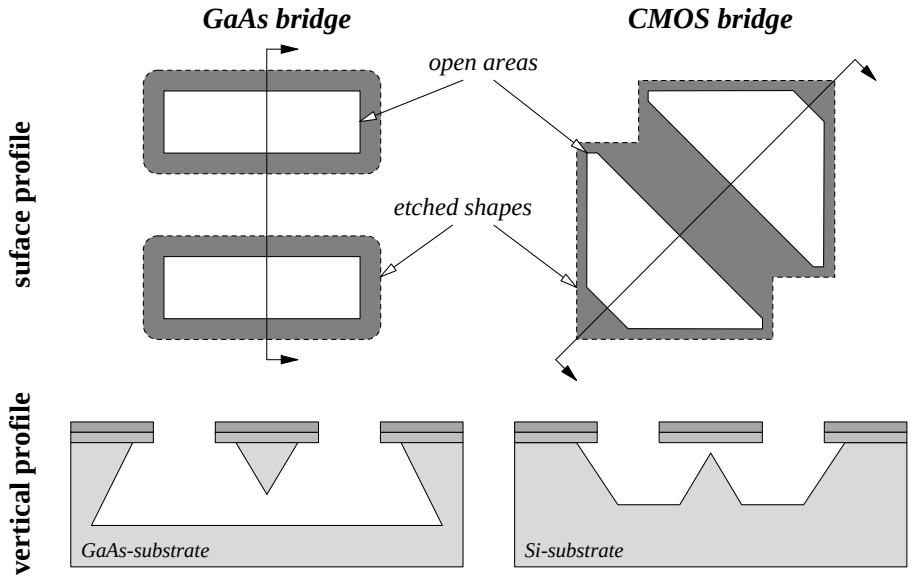
The cross section viewer is used as the output interface to display the results. During the cross section procedure, the existence of open area layers intersecting the cut line is verified, as well as the orientation of their edges in order to associate with them the respective 2D vertical etch diagram. That is, if the edges of a mask shape (open area) are not parallel different diagrams are taken into account for each side. Moreover, the predicted profiles shown are obtained considering that the cut line is perpendicular to the mask edges, and in this first tool version only the edges oriented orthogonally or in 45 degree are evaluated in order to simplify the etch diagram description, defined in the vector form [angle,rate] for etch point. Otherwise, a three-dimensional polar diagram is required. Note that, the minima and the regions immediately adjacent to them on the polar diagram are the principal responsibles for the final shape. A great number of etch rates

could give a closed profile, but increasing certainly the computing time. Finally, as with the surface etching preview, the interfacing dialog box of the simulator allows the definition of start simulation time, step time and number of simulations (see Fig. 6.14).



(a) (b) (c)

Fig. 6.11 - Surface etched shape comparison: (a) preview, (b) simulation and (c) photograph.



(a) (b)

Fig. 6.12 - Bridges in GaAs (a) and CMOS (b) compatible micromachining.

An important assumption of such a kind of 2D vertical method is that the edges are considered infinite, i.e., the influence of the etching originated from adjacent open areas not present in the cut view plane, commonly observed for membranes and in the extremity of cantilevers, cannot be taken into account. For this, a 3D anisotropic etching simulator is demanded [24]-[26].

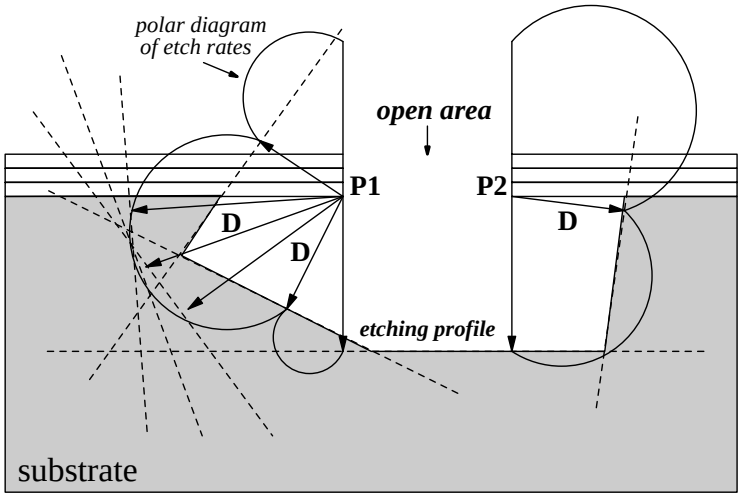


Fig. 6.13 - The 2D Wulff-Jaccodine prediction method [18].

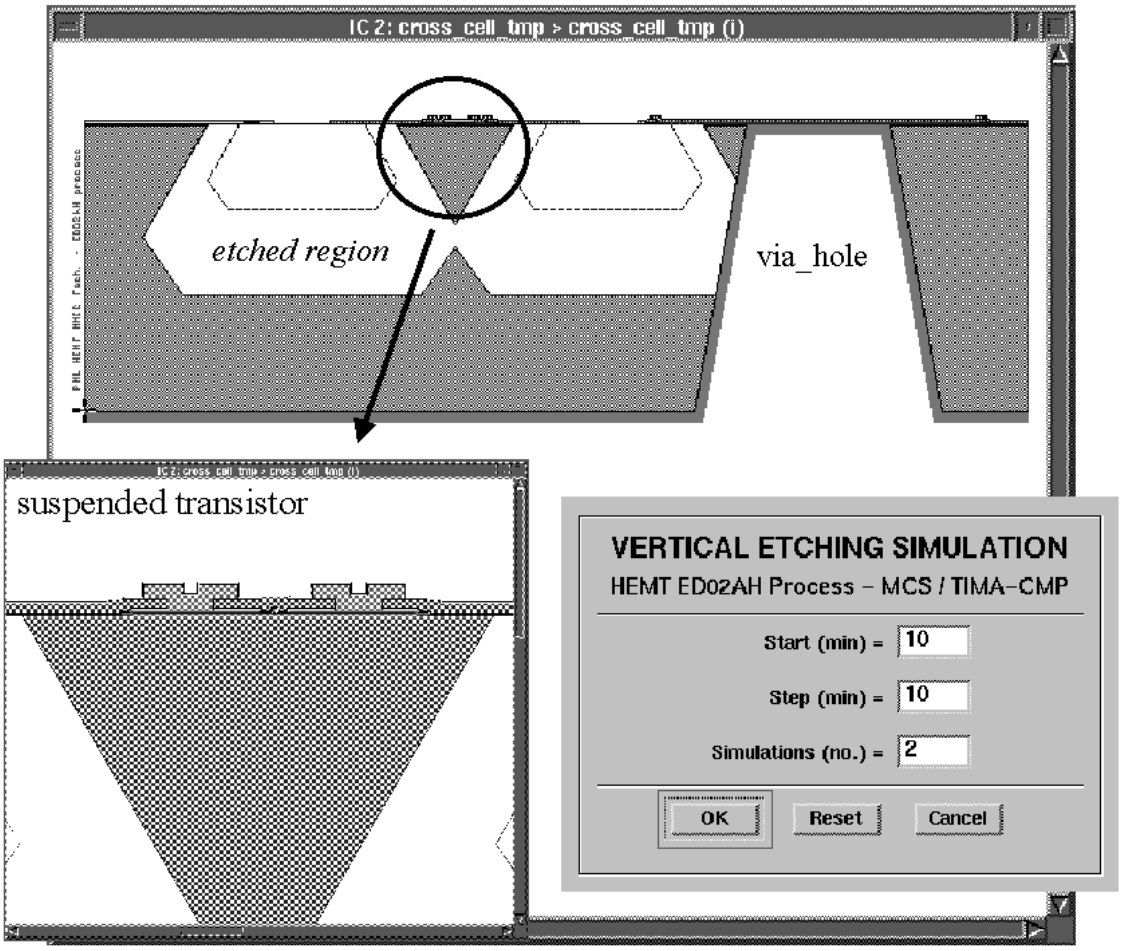


Fig. 6.14 - Anisotropic etching simulator for 2D vertical profile.

6.6 MENTOR GRAPHICS ENVIRONMENT AND SUMMARY

The set of tools, described in this chapter, are independent of the technology and they have been included in the MEMS engineering kit for the Mentor Graphics environment, for both CMOS and GaAs processes (see Fig. 6.15). In summary, with the back-end design flow is possible to : (a) run a single electronic and micromachining design rules checking; (b) create automatically several types of electronic and micromachined devices using layout generators; (c) obtain cross section views in any direction and position of the layout; (d) create a three-dimensional layout representation for illustration or solid model FEM simulation; (e) visualize the etch rate polar diagrams; (f) predict the surface etched shape through a fast preview (isotropic etching) or using the anisotropic etching simulator ACESIM, with the visualization of results on the original layout or in a new layout window; (g) predict the vertical profile of etched bulk regions; and, finally, (h) convert automatically open areas to real layers and vice-versa.

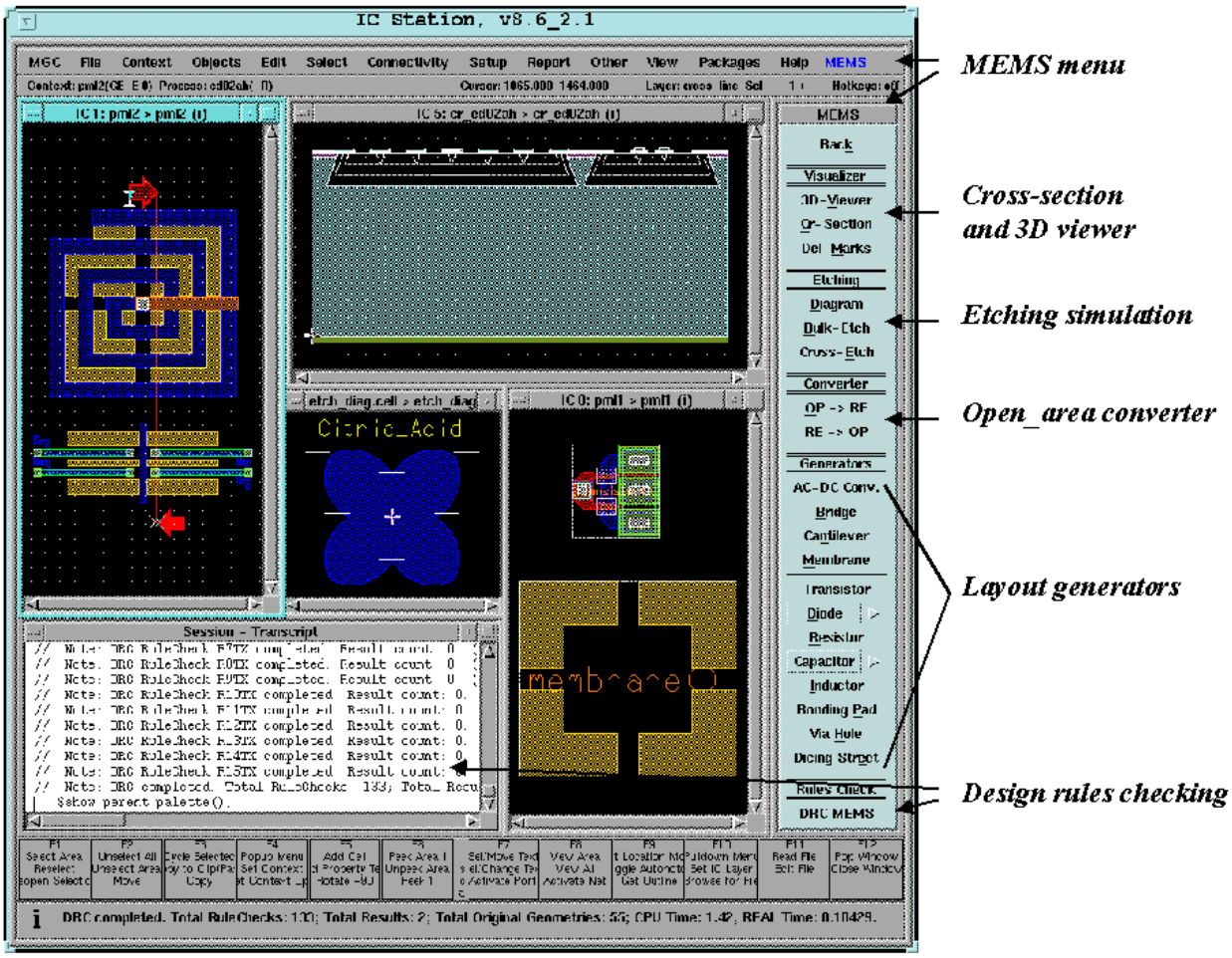


Fig. 6.15 - MEMS design kit front-end on the Mentor Graphics IC Station.

In terms of the front-end design flow, work is being carried out at TIMA laboratory, including schematic capture, HDL-A models of microelectromechanical devices for electrical simulation, and SDL (Schematic Driven Layout) linked to the layout generators. This part of the design flow is also technology independent, being easily configured for the GaAs micromachining approach, discussed in this work.

As future developments, it is necessary to consider the improvement of the layout extraction to the 3D solid model FEM simulation including automatic meshing, a 3D anisotropic etching simulator, and the integration of a thermal simulator like SISSI that takes into account micromachined devices [15]. Moreover, particularly to MMIC processes, like PML ED02AH, it is important to provide microwave simulators, such as MDS, in CAD microelectronics environments.

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Chapter 7
CONCLUSIONS AND PERSPECTIVES

"Though our work from day to day may seem insignificant in size, together our work is grand in purpose... A science grows by the unfettered competition of ideas, not people... People should be free to suggest and work on the new. Unfortunately it is easy to disdain the unfamiliar..." W. Trimmer [1]

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7.1 SUMMARY AND SCIENTIFIC CONTRIBUTIONS

Firstly, in the presented work, the interest in using GaAs material and related technologies, rather than the cheaper and well developed silicon ones, was clearly outlined. Physical properties, mechanical and thermal characteristics, and microelectronics process facilities, associated with the number of compatible III-V ternary alloys, justify the use of such material in microsystems. Although still more expensive than standard CMOS, GaAs based IC processes are commercially available today for high-frequency digital and analog systems as well as monolithic microwave and millimeter-wave circuits, representing a promising possibility for smart sensors in which the integration of electronics represents the basic requirement [2][3].

Many GaAs micromachining techniques have been proposed in the literature and rely on the numerous suitable etchants available for selective etching, considering different etch stop layers, and for anisotropic or preferential etching, in order to create the unique triangular prism-shaped bridge. Herein, the well-known maskless front-side bulk micromachining compatible with standard microelectronics technologies, which represents perhaps the fastest and most efficient way of designing MEMS, has been successfully extended to GaAs processes.

In fact, like already observed in CMOS [4], such micromachining approach presents as the main drawback problems related to eventual residual layers over the exposed substrate surface regions, causing irregularities in the post-process wet etching or even impeding the release of the structure. This is because the stack of dielectric openings needed to create open areas is generally not expected by microelectronics foundries, during the IC fabrication. Such a problem was strongly verified in the Vitesse MESFET H-GaAs III dies, and even after discussions with the foundry engineers and the various pre-cleaning techniques applied, no real solution has been found to solve it. In the case of the PML HEMT D02AH chips, on the other hand, such residual layers were observed to be much less critical, allowing reliable open areas with dimensions down to 4 μm. Thus, this process was taken into account for etching characterization and investigation of potential applications [5].

In Chapter 3, an extensive review about wet chemical etchants for GaAs was realized in order to evaluate them for this micromachining purpose. Note that, the aim of this work was not to develop new etching solutions, but determinate the most appropriate existent ones in terms of damage in the surface layers, undercutting and depth etch rates, and both surface and vertical profiles of the etched bulk regions. The feasibility of suspended microstructures was proven and three etching solutions appeared to be well suited: the citric acid for selective etching, and the NH_4OH and H_3PO_4 (at 0°C) based solutions for preferential etching behavior [6]. Other etchants

showed damage on the exposed pad metallization (e.g. Br-based solution), while NH_4OH etchant for selective etching of GaAs with respect to AlGaAs seemed to attack the dielectric layers (SiO_2 and Si_3N_4).

Since GaAs transistors are able to operate at temperatures up to 350°C or more (due to the large bandgap of GaAs) and because of high thermal resistivity and high Seebeck coefficient, thermal based devices are very attractive for GaAs micromachining. Moreover, the triangular-shaped structure allows building efficient thermally isolated active and passive electronic devices, as demonstrated in Chapter 4. Although GaAs-metal thermocouples are possible in PML HEMT technology, the use of the thick gold layer as a thermocouple material reduces significantly the thermopile self-generated voltage due to its very low Seebeck coefficient and excellent thermal conductivity. As a result, in applications where silicon structures could be applied, it is somewhat difficult to justify the use of such a more expensive alternative. On the other hand, thermopile based microwave power sensors are very useful for MMIC design, as provided by PML [7].

Furthermore, micromachined microwave passive devices have been widely investigated nowadays due to the emerging wireless communication systems. Suspended transmission lines show significant improvements in performance because of the elimination of high frequency parasitic capacitance effects and associated losses. The possibility of using small open areas in PML HEMT allowed not only free-standing microstrips but also a novel planar rectangular spiral inductor with each segment suspended individually as proposed in Chapter 5 [8][9]. This new inductor structure presented improvements up to 150% in self-resonant frequency and quality factor for a 12 nH inductor. The usefulness of such approach was also demonstrated through a micromachined planar transformer, composed by two interleaved spiral inductors [10]. Mechanical and thermal constraints of these devices were briefly evaluated through FEM simulations.

Finally, in Chapter 6, a straightforward strategy to allow micromachining design rules verification was proposed based on the use of a fictitious layer, called open area. On the other hand, specific and mechanical rules were discussed to be important as well, but they require appropriate etching and mechanical simulators, intensive experimental characterization and design experience to be determined. Moreover, CAD tools for MEMS were developed in the Mentor Graphics environment at the layout level (back-end design flow), including viewer tools (cross section and three-dimensional representations for layout analysis and illustration), etching simulators (vertical profile and isotropic preview) and layout generators for basic suspended structures, micromachined applications and electronics components. This set of tools can be configured for any technology and was validated herein taken into account the PML (E)D02AH processes.

It must be pointed out that the greatest difficulty of such a kind of work, where industrial IC technologies are addressed for microsystems, is the fact that the chip fabrication depends on the prototyping runs offered by multi-project services. In the case of PML HEMT, for example, which might be considered as an expensive technology in comparison to CMOS and, it is in general exclusively used for MMIC design, and a few fabrication runs are available from CMP service, i.e., around two runs per year. In addition, for this particular process, the designer waits approximately six months between the dates of layout submission and return of the dies, which commonly coincides with the next run deadline. Therefore, to profit the next consecutive run, a new layout design cannot take into account the experimental results and complete evaluation of the last fabricated circuit. Note that, such a problem had great influence in the study about thermal devices (see Chapter 4), while in the case of micromachined microwave devices, presented in Chapter 5, it was not so critical due to the simplicity of the etching procedure, where no constraints of selective and preferential etching were required.

7.2 STATE OF THE WORK AND FUTURE DEVELOPMENTS

Of course, complementary information about the etching kinetics as well as mechanical and thermal properties of concerned layers is necessary to control all factors involved in the front-side bulk micromachining. Although general assumptions can be obtained from the presented results, specific micromachining evaluation is always required for each particular targeted GaAs IC process, since the available surface layers and the composition of III-V ternary alloys, if they exist, have great influence on the post-process etching and potential applications.

The etching characterization realized herein can be considered enough for micromachined devices where selective and preferential etching behavior is not demanded. Otherwise, future studies must be carried out taken into account the suitable etchants listed herein. However, as mentioned, to generate three-dimensional etch rate polar diagrams and to know more about the selectivity for such specific purpose, additional experiments should be realized at the wafer level, with different orientations; at the die level, in special for the chip dimensions provided by PML in the HEMT process, such a task is almost impractical. Furthermore, studies concerning back-side micromachining have started, because the PML foundry is giving the possibility to use inside the layout the CS (*chip-select*) layer, normally restricted to dicing street structures for chip separation. Such layer is equivalent to an opening in the back-side metal plate with minimum width of 50 µm. So, suspended big masses of bulk GaAs material for pressure sensors and accelerometers, for example, are expected to be released using this additional facility. And why not considering silicon dioxide as a sacrificial layer in surface micromachining using PML HEMT [11] ?

At the present time, the GaAs technologies offered to the CMP users are the Vitesse MESFET H-GaAs IV and PML HEMT ED02AH processes [12][13]. The update of IC processes is an important factor and could represent a considerable effort to validate them for microelectronics compatible micromachining. In this last Vitesse MESFET version, since the transistors have only scaled down to 0.5 μm effective gate length, the problems of residual layers, not solved for the H-GaAs III process, are expected to be similar. On the other hand, the PML ED02AH process is basically different from the D02AH one since both enhancement and depletion mode HEMTs are available. So, almost nothing should change with respect to the results presented here. A chip test is being fabricated.

Certainly, several other micromachined devices and interesting applications, not treated in this work, should be investigated as well. For example, the very small and reliable open area allowed in PML HEMT, associated with the thick metal layer used for interconnection, could perhaps be exploited to build microelectromechanical devices, such as comb drives, resonators and mechanical filters, normally obtained by means of silicon surface micromachining [11][14].

Moreover, piezoelectric and piezoresistive devices, specially considering the triangular prism-shaped bridge, because of the significant bulk mass that it can suspend, seems to be efficiently implemented in GaAs [15]-[18]. The GaAs piezoelectric effect has been shown to be as good as that observed in quartz, although few practical devices have been presented in the literature.

Optoelectronic devices are accepted today as perhaps the only way to increase the performance of systems, and in this case silicon is practically dismissed by III-V materials. Micro-optical-electro-mechanical systems (MOEMS) have also found their place in the research world [19]-[21]. However, MOEMS compatible with standard microelectronics technologies are only possible in IC processes that provide integrated light sources and detectors, which is not the case of Vitesse MESFET and PML HEMT. Remember that no modification in the fabrication steps are allowed using the proposed micromachining approach.

As the last example of interesting area of investigation, magnetic devices should be mentioned [22]. Though they are not really micromachined structures, magnetic based structures could be used for multi-sensor chip design [3]. Note that MESFET and HEMT based technologies have allowed to build Hall sensors with high sensitivity and low thermal drift because of the higher GaAs carrier mobility [23]-[25].

In terms of micromachined microwave devices, the good results obtained here with planar

spiral inductors and transformers suggest to go towards MMIC applications, like filters, mixers, oscillators, low-noise and tuned amplifiers. Suspended MIM and interdigited capacitors have also been sent to fabrication for characterization. Moreover, another promising feature of using a MMIC process is its compatibility with microstrip antenna technology [26][27]. It could be thought that two chips containing sensing elements are able to communicate without physical connection. For several applications in medical area, harsh environments and others, where the connection of wires to the sensing chip is somewhat difficult, microstrip antennas could be very useful for data transmission and power supply.

Finally, CAD environments for MEMS are just in the beginning of their development around the world. Many players such as MEMSCAP, Microcosm, Intellisense and others are pushing further the state-of-the-art in CAD of MEMS. In future developments related to the back-end, additional efforts should be directed towards a 3D anisotropic bulk etching simulator as well as a 3D layout representation that illustrates the surface relief presented by the real integrated circuits.

The goals targeted in this thesis have been successfully attained. To the author's knowledge, it represents a pioneering work in front-side bulk micromachining using industrial production line processes other than the silicon based ones. This work tried to give the basis for the post-process etching and design rules (technology part), the potential micromachined devices and applications (design part), and a set of tools for MEMS development (CAD part). Moreover, a number of directions for new research and projects are clearly suggested, demonstrating that it does not represent a finished work but the beginning of interesting and promising investigations and developments [28].

MEMS will have profound impact in the future society. It is necessary to continue and enhance research activities in both fundamental and application-oriented areas. Fusion of knowledge in different disciplines is essential for well-balanced and accelerated growth of the technology. The research world is living in this decade the real starting of a new generation of microthings, already predicted by Richard Feynman in his two famous lectures, "There's Plenty of Room at the Bottom" in 1960 [29] and "Infinitesimal Machinery" in 1983 [30], although even he did not believe in the usefulness of such microstructures : *"I also talked in the 1960 lecture about small machinery, and was able to suggest no particular use for the small machines. You will see there has been no progress in that respect."* - R. Feynman [30].

Imagine the great number of applications and areas that can be improved today and in the next future with very small and reliable microsystems and all kind of microsensors and

microactuators. Be sure, it is going on...

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