An Embedded Compact PCI Computer System for a Synthetic Aperture Sonar Towfish

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Abstract: This paper describes the embedded computer system used in the towfish of the KiwiSAS-IV synthetic aperture sonar being developed by the Acoustics Research Group at the University of Canterbury. The sonar is designed for high-resolution seafloor imagery and bathymetry, requiring eighteen receiver channels to be simultaneously sampled and twenty four independent waveforms to be generated. The computer system is based on Compact PCI backplane and allows data to be streamed in real-time up the tow-cable to computers on the towboat for storage, image reconstruction, and display.

Keywords: Compact PCI, Data-Acquisition, Delta-Sigma ADC, FPGA

1. INTRODUCTION

The Acoustics Research Group within the Department of Electrical and Computer Engineering at the University of Canterbury have for many years been developing synthetic aperture sonars. The goal is to use aperture synthesis techniques to generate high-resolution imagery and bathymetry [1, 2] of the seafloor, in particular within shallow water harbour environments.

The current sonar in development is our most ambitious to date. This sonar has multiple receiver transducers (hydrophones) to provide faster to speeds and longer ranges. It also has multiple transmitter transducers (projectors) for steering of the transmitted beam. In total there are eighteen hydrophones and seventy two projector elements that need to be interfaced. The signals from the hydrophones need to be simultaneously sampled and streamed from the towfish up the tow-cable to computers on the towboat for storage, image reconstruction [3, 4], and display. At the same time, individual transmit signals for each projector transducer need to be generated and correctly phased to control the direction of the transmitted acoustic beam.

The paper starts with an overview of the system design requirements, discusses the Compact PCI computer chosen for the towfish, looks in more detail at a custom signal acquisition/generation Compact PCI card being developed, briefly describes the interface between the towfish and towboat computers, followed by short description of the system software, and conclusion.

2. SYSTEM DESIGN

The towfish of the previous sonar (KiwiSAS-III) shown in Figure 1 is similar to the new sonar being constructed (KiwiSAS-IV). The major visible differences are that the new sonar has the projector arrays in the centre of the towfish, has a keel containing nine additional hydrophones, and is slightly longer.

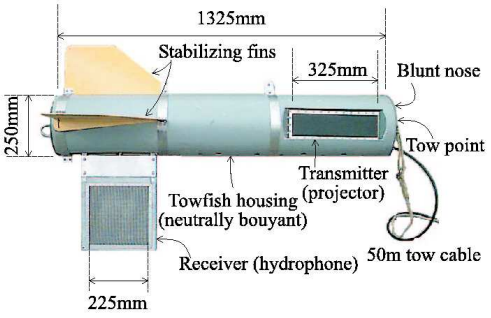

Figure 1: KiwiSAS-III towfish. The KiwiSAS-IV towfish is similar but with the projector moved to the centre and with an additional hydrophone array keel.

KiwiSAS-III used a single waveform generated on the towboat and sent as an analogue signal to the towfish for driving all projector elements together. Similarly, the three hydrophone signals were amplified within the towfish and sent as analogue signals to the towboat for sampling and storage[5]. Apart from a navigation card[6] within the sonar, the towfish electronics was entirely analogue (see Figure 2). The waveforms were generated and sampled using custom electronics on the towboat (see Figure 3). However, this system is no longer feasible with the new system requirements, so the waveform generation and sampling now has to be performed within the towfish and digitally transmitted to the towboat computer.

To support the data rate requirements of the new sonar it was realised that a powerful embedded computer was required. This must be rugged since it was to be mounted in an underwater pressure housing. A modular commercial system was preferred and a 3U Compact PCI system was found to meet most requirements. Unfortunately, off-the-shelf cards could not be found to meet the initial design requirements for the signal acquisition and generation, listed in Table 1 and Table 2. The most important requirements being that the 18 input channels could be sampled continuously with no loss of data and that the channels were matched with minimal phase distortion.

Table 1: Signal acquisition requirements.

- 18 input channels
- 120 kHz bandwidth/channel
- continuous sampling
- large dynamic range
- minimal phase distortion (channels matched)
- differential inputs

Table 2: Signal generation requirements.

- 72 output channels
- 120 kHz bandwidth/channel
- arbitrary waveforms/channel
- periodic waveform repetition
- low-order reconstruction filters
- differential outputs

It was envisaged that separate custom acquisition and generation boards would be used, however, a single design was chosen to simplify development and maintenance. It was also realised that 72 output channels was ambitious, especially since these channels had to be well oversampled so that low-order reconstruction filters could be used. The initial figure of 72 channels was derived from having to support two projectors (port and starboard) each comprising 36 elements arranged in three rows of twelve. It was desired that each element could be driven independently to provide beam steering and aperture apodisation. As a compromise, it was decided to drive each column of transducers as a group. While vertical beam steering was desirable for roll compensation at high frequencies, it was more important to provide horizontal aperture apodisation and to provide horizontal beam steering for spotlight operation. With the number of output channels reduced to 24, a configuration of three cards each supporting 6 input channels and 8 output channels was chosen. The primary constraint was the number of ADCs that could be fitted on the chosen Compact PCI 3U form factor.

3. COMPUTER SYSTEM

The computer system used within the towfish is based on a 3U Compact PCI bus. Compact PCI is an adaption of the Peripheral Component Interconnect (PCI) bus for industrial computers. It is electrically compatible with the PCI bus found in most PCs and workstation computers but physically it is more rugged, with 2 mm hard metric, 110 pin plug and socket connectors. Each card, including the processor, has a 3U Eurocard form factor of 160×100 mm.

The computer system must fit within a pressure housing. This consists of a length of PVC tube with machined aluminium endcaps fitted with o-rings for sealing. A primary design criteria of the towfish is that it must be able to be deployed by two people without a crane. Moreover, the towfish must be slightly positively buoyant. This places a restriction on the size of the pressure housing and thus a restriction on the size of the computer system. The larger the housing the larger the towfish and moreover the greater the additional weight required to ensure that it is not too buoyant. We also did not want to change the dimensions of the current sonar since this has proved to be hydrodynamically stable. This fixed the internal diameter of the pressure housing to 205 mm.

We chose a commercial six-slot Compact PCI backplane. This is the largest backplane that fits within the pressure housing. The backplane has lugs for power supplied from four switch-mode (Vicor) power supplies (3.3 V, 5 V, $\pm$12 V) that operate off 24 V DC supplied from batteries on the towboat. The power supplies are small enough to be mounted on the aluminium end-cap of the pressure housing and switch well above the maximum sonar signal frequency of 120 kHz.

The processor card we selected was a Pentium-III

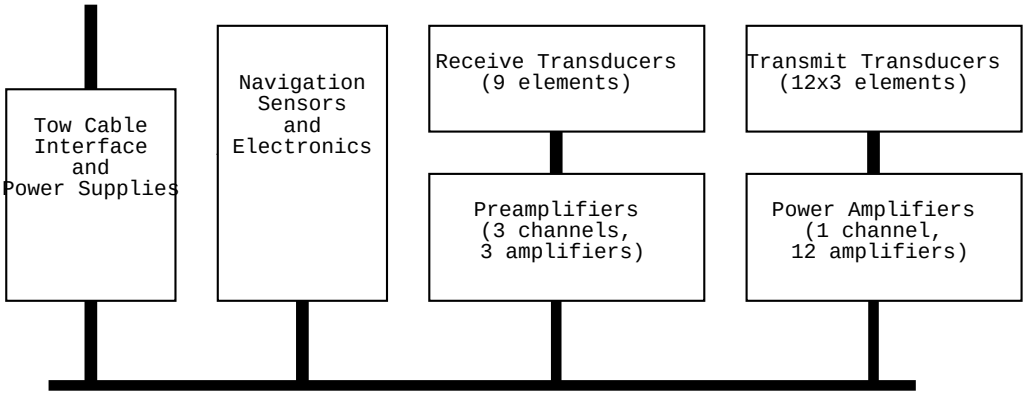

Figure 2: Block diagram of KiwiSAS-III towfish electronics.

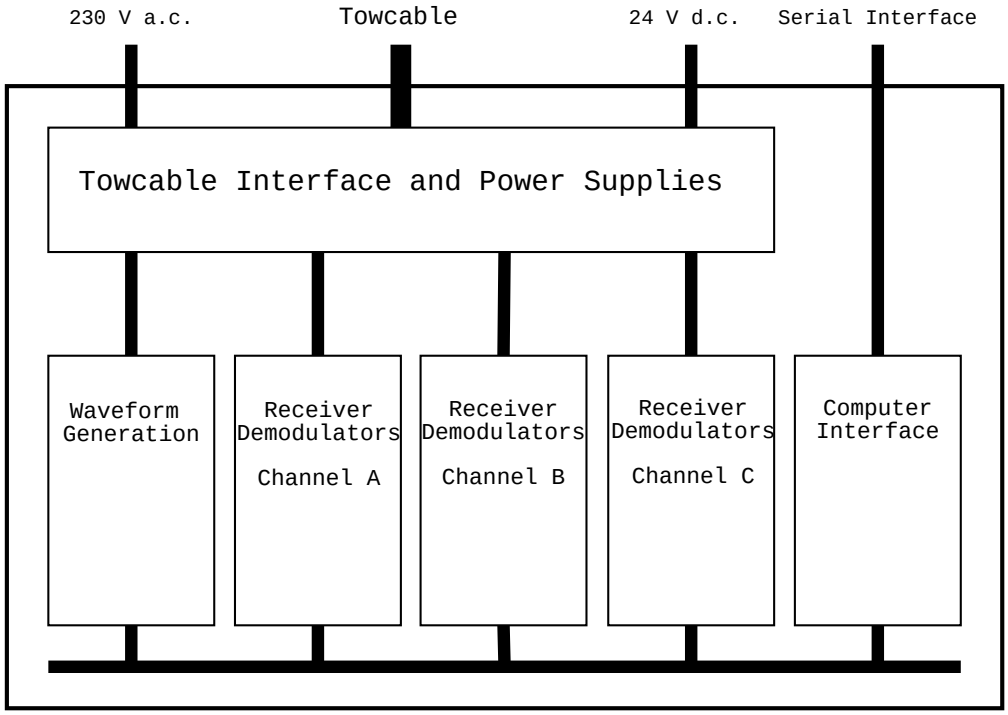

Figure 3: Block diagram of KiwiSAS-III towboat electronics.

based card called RAVE-5 made by a German company EKF. The card has 256 MB of SDRAM, a 10/100 Mbit Ethernet port, two USB 1.1 ports, a DVI video port (supporting both digital and analogue monitors), an IDE interface, and a CompactFlash connector. There is a companion card (ACID-6) that provides keyboard, serial port, parallel port, and optional IDE disk. This module allows the processor to be powered on the bench with a keyboard, mouse, and monitor simplifying testing and software development. Obviously, in normal operation these peripherals are not required.

A Pentium-III CPU was chosen for compatibility with the towboat computers to simplify software development. This allows a standard Linux distribution to be run on both the towfish and towboat computers. Moreover, since the towfish computer is diskless, it could be booted from the towboat computer using a shared file system and shared system files.

4. SIGNAL ACQUISITION/GENERATION CARDS

The signal acquisition/generation cards each provide six input channels and eight output channels. All input and output analogue signals are differential to reject common-mode interference. A block diagram of the card is shown in Figure 5.

4.1 Timing and Control

A Xilinx Spartan-II Field Programmable Gate Array (FPGA) controls the system timing and implements a

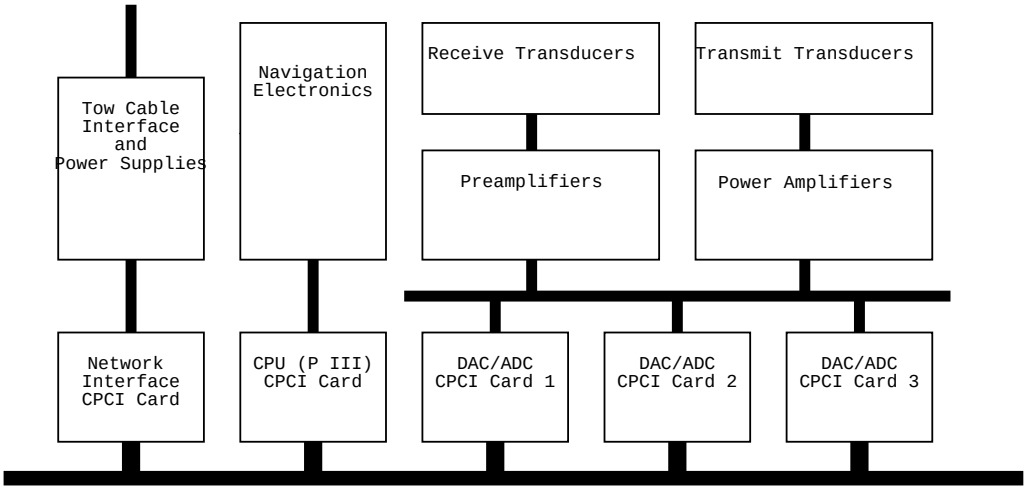

Figure 4: Block diagram of KiwiSAS-IV towfish electronics showing the main modules.

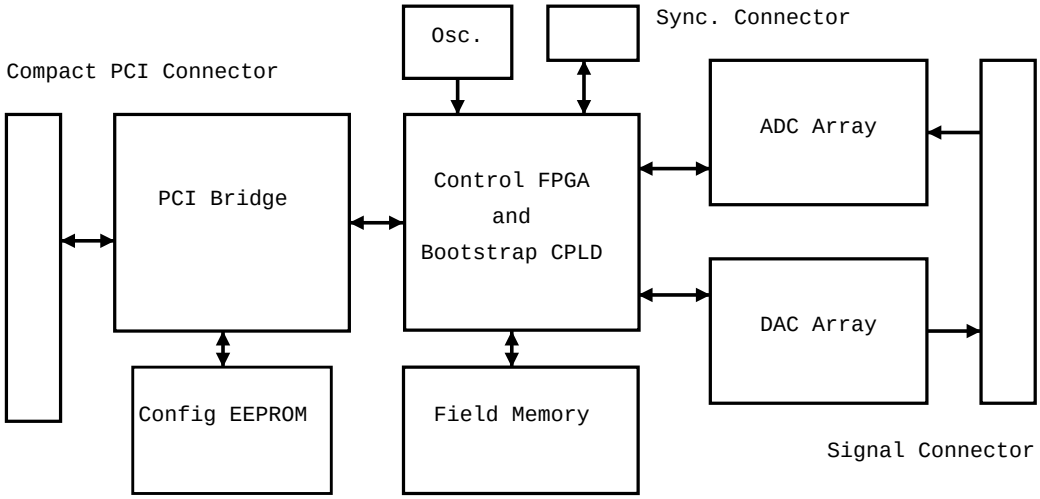

Figure 5: Block diagram of signal acquistion/generation card electronics.

FIFO for each channel. The data is then streamed into memory on the processor board using a PCI bridge (PLX PCI9054) with a scatter-gather mode DMA controller.

The FPGAs are programmed in VHDL and can be configured from the PCI bus via the PCI bridge. The logic required for the interfacing is provided by a small Xilinx CPLD (this is initially programmed via a JTAG interface). Thus the firmware can be remotely upgraded without having to open the pressure housing the computer is mounted within.

4.2 Waveform Acquisition

Each input channel utilises a 16-bit delta-sigma ADC (AD7723), sampling at 20 MHz giving a sampled signal bandwidth of 450 kHz. Delta-sigma ADCs were chosen to simplify the anti-aliasing filter specification minimising phase shifts between the channels. The AD7223 oversamples at 16 or 32 times the desired output rate and thus only a low-order anti-aliasing filter is required.

The AD7723 has differential inputs, buffered by high speed differential amplifiers (THS4141) with unity gain. These amplifiers provide a low impedance drive and reduce the level of switching signals from the ADCs being coupled back into the preamplifiers. They also provide a single pole low-pass filter for anti-aliasing.

While the AD7723 has an internal 2.5 V bandgap voltage reference, an external 3 V reference (AD780) was selected to drive all six ADCs giving better temperature and drift characteristics and a slightly better SNR.

The AD7723 has both parallel and serial output configurations; the serial configuration was chosen since fewer tracks need to be routed to the FPGA. To further reduce the number of tracks, the ADCs are commonly clocked with one master chip providing the synchronisation signals. Even though the FPGA uses 3.3 V

LVTLL logic and the AD7723 uses 5 V TTL logic, the devices are electrically compatible except for the input clock. This requires 5 V CMOS logic levels and so a level shifter (74LVC4245A) was employed for this signal. Separate buffers were used for each ADC with series termination to reduce clock jitter caused by multiple reflections.

4.3 Waveform Generation

The output signals are generated using serial 12-bit DACs (TVL5636) connected to a (MSM51822A) field memory, with sampling rates of 1.25 MHz/channel. The field memory can be programmed with arbitrary waveforms from the processor via the PCI bridge and FPGA controller. The output signals are used to drive the array of transducer elements comprising the sonar projector array. Each channel uses independent waveforms allowing the transmit beam to be steered.

The field memory provides 256 Kbytes of storage with independent 8-bit input and output ports. It is similar to a FIFO memory but has read and write pointers that can be independently reset. Thus a sequence of time multiplexed waveforms can be stored in the memory and then repeatedly clocked out. Internally the field memory uses a large DRAM array with small caching SRAM buffers so recently written data can be quickly read back. Unfortunately, there is a potential ambiguity when reading data; it is possible to inadvertently read data recently cached in SRAM and not the desired data in DRAM. This aspect is poorly explained in the MSM51822A data sheet and a programming sequence had to be heuristically developed to deal with this problem.

4.4 Synchronisation

Each card has its own 40 MHz crystal oscillator module that provides a local clock for each FPGA. When programmed as a master, the local clock drives the system clock signal, common to all the acquisition/generation cards, using a short ribbon cable interface. To reduce clock skew, the master uses the system clock for its timing rather than its local clock. The master FPGA also provides a synchronisation signal to drive the slave cards.

4.5 Compact PCI Interface

The Compact PCI interface is controlled by a PCI9054 PCI bridge chip from PLX Technology. This is a 32-bit, 33 MHz, bus-mastering PCI bridge, with a local bus of 50 MHz. This device was used successfully with the KiwiSAS-III system for high speed data transfer from the towboat electronics to the towboat computer.

The PCI9054 provides two local memory-spaces: one is used for programming of the FPGA and the other is used to access the control/status registers implemented within the FPGA. The initial configuration of the bridge, in particular the PCI Vendor and PCI Device IDs can be stored in an optional EEPROM, otherwise default values are used.

The PCI9054 has a scatter-gather mode (chaining) DMA (direct memory access) engine. This reads descriptors from either the PCI bus or the local bus to load its control/status registers at the start of each block transfer. Thus the CPU can prepare a linked list of DMA descriptors that the DMA controller processes independently of the CPU. When each transfer has completed, the CPU can be notified by an interrupt. Thus the DMA controller can continuously stream data into memory with only a pause while it reloads its registers from the next DMA descriptor. During this reload period a FIFO buffer is required to avoid the loss of data.

Three known quirks of the PCI9054 that are not well documented are:

1. A weak pull-down is required on the READY line.
2. Samples can be lost in DMA mode when the PCI9054 reloads its registers at the start of a chained transfer. This problem can be avoided using a FIFO to buffer the recorded data.
3. Sometimes the PCI9054 generates a DMA acknowledge even though no DMA request was asserted. One solution is to always keep at least one sample in the FIFO.

4.6 Power Supplies

Each card uses six independent power supplies. The Compact PCI 5 V supply powers the field memory and the ADC digital circuitry while the 3.3 V supply powers the PCI bridge and FPGA I/O. The 3.3 V supply is also regulated to 2.5 V for the FPGA core. Two additional 5 V supplies are derived from the 12 V Compact PCI supply to provide separate analogue supplies for the ADCs and the DACs. These supplies use linear regulators with feed-through capacitors to improve high frequency regulation. Low ESR decoupling capacitors are used throughout to reduce high frequency switching currents.

4.7 Printed Circuit Board

The prototype cards are constructed entirely using surface mount devices on a two-layer printed circuit board. Separate power supplies are used for the digital logic, ADCs, and DACs with extensive isolated

ground-planes to reduce interference. Test headers are provided for connection to logic analysers for debugging.

5. TOWBOAT INTERFACE

The tow-cable of the KiwiSAS-III sonar employs four shielded twisted pairs within an overall shield. This is going to be retained for the new sonar although in the future it may be replaced with a fibre/copper cable. Two of the pairs provide a 100 Mbit/s Ethernet connection between the towfish and towboat computers, one of the pairs provides 24 V d.c. for the towfish, and the final pair provides a high speed data link using a custom modem matched to the characteristics of the tow cable [7].

6. SOFTWARE

The towfish computer runs a standard RedHat distribution of the Linux kernel and is booted using an Ethernet connection from the towboat computer. The data acquisition and sonar control program used for KiwiSAS-III sonar is being ported to run on the new system. Essentially this program uses three threads: the first to read the sampled echo data, the second to write (and possibly compress) the sampled echo data to the towboat computer, and the third for the user interface. The program is controlled by the main graphical user interface program running on the towboat computer and is designed to log the echo and navigation data even if the graphical user program fails.

The data acquisition and sonar control program interfaces to the signal acquisition/generation cards through a custom Linux loadable device driver module. This driver has been written to support multiple cards. For each card there are two ring buffers; one to write data to the field memory and the other to read the sampled echo data. The DMA engine on the PCI bridge is configured to automatically fill this second ring buffer to achieve maximum throughput with minimum CPU overhead. Typically four DMA descriptors are used, linked together in a ring, to fill the four quarters of the ring buffer. When a new quarter is filled, the DMA engine informs the device driver through an interrupt. This then wakes the blocked thread waiting to read data from the ring buffer.

7. CONCLUSION

The paper has presented an overview an embedded Compact PCI computer system for a synthetic aperture sonar towfish and has focused on a custom signal acquisition/generation card that is being developed. Three of these cards will be used together to synchronously generate 24 arbitrary transmit signals and to sample 18 echo signals. A key design requirement was that the data could be continuously streamed so a bus mastering PCI bridge was selected. Oversampling techniques have been employed to lower the order of the anti-aliasing and reconstruction filters. Not only has this reduced the component count but has reduced phase shifts in the passband. Finally, care has been taken to minimise noise and interference by using differential analogue signals, well decoupled multiple power supplies with separate ground planes, impedance matching of fast digital signals, and careful layout.

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