WRDC-TR-90-4135
ADA235223

INVESTIGATION OF POLYBENZOCYCLOBUTENE RESINS IN MULTILAYER THIN FILMS FOR ELECTRONIC PACKAGING

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February 1991

Final Report Period for January 1989 – September 1990

MATERIALS LABORATORY
WRIGHT RESEARCH AND DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433-6533

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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S) WRDC-TR-90-4135
6a. NAME OF PERFORMING ORGANIZATION Hughes Aircraft Company Electro-Optical and Data Systems 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Materials Laboratory (AFSC) Wright Research and Development Center
6c. ADDRESS (City, State, and ZIP Code) El Segundo, CA 90245	7b. ADDRESS (City, State, and ZIP Code) WRDC/MLBP Wright-Patterson AFB, OH 45433-6533
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F33615-88-C-5509
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT ACCESSION NO.
62102F	2423	01	A2

11. TITLE (Include Security Classification)

Investigation of Polybenzocyclobutene Resins in Multilayer Thin Films for Electronic Packaging

12. PERSONAL AUTHOR(S)

S.O. Fong, Dr. J.W. Peters

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM 1/89 TO 9/90	2/22/91	54

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Electronic Packaging, Benzocyclobutene Resins Composite Materials, Coatings
1109	01		
1104	02		

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Polybenzocyclobutene dielectric films were found to exhibit significant advantages compared to polyimides for multichip multilayer packaging applications. Although PBCB films must be cured in an oxygen-free environment and are somewhat more sensitive to warpage/stress than polyimides, they are significantly superior with respect to moisture resistance, lower dielectric constant and leveling or planarization over rough surface topography. The adhesion of PBCB films to copper, aluminum and silicon without adhesion promoters is excellent. Tests to date with PBCB as a multilevel dielectric with both a counter/decoder circuit and an analog circuit, in conjunction with via post interconnects, reveal the potential for the reliable fabrication of high speed and high density multichip/multilayer modules.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	Unclassified

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL
B.A. Reinhardt	513-255-9162	WRDC/MLBP

DD Form 1473, JUN 86 *Previous editions are obsolete.*

SECURITY CLASSIFICATION OF THIS PAGE

Unclassified

FOREWORD

This report covers research performed by Hughes Aircraft Company, Technology Support Division, Electro-Optical and Data Systems Group, El Segundo, California 90245, on Contract F33615-88-C-5509, "Investigation of Polybenzocyclobutene Resins in Multilayer Thin Films for Electronic Packaging." This period of research covered was from January 1989 to September 1990.

This research was performed by S. O. Fong, Principal Investigator, under the direction of Dr J. W. Peters, the Program Manager. This effort was sponsored by the Polymer Branch (WRDC/MLBP), Nonmetallic Materials Division, Materials Laboratory, Wright Research and Development Center, Wright-Patterson Air Force Base, Ohio. Fred Hedberg and Bruce Reinhardt were the Project Engineers.

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1.0 INTRODUCTION

There are many electronic modules which require the interconnection of standard IC's which heretofore have been assembled together using discrete wiring. These IC's can be wafer reconstructed using a multilayer dielectric/metal interconnection. Such wafer scale reconstruction of IC devices makes it possible to achieve electronic multi-chip modules which are higher density, lighter weight and faster speed than their discrete wiring counterparts (1-5). Future avionics and space systems which require high speed and light weight dictate the need for these multi-chip modules.

Intrinsic properties of the dielectric such as dielectric constant, moisture absorption and planarizability are important for both the fabrication and the electronic speeds of the multilayer modules. Lower dielectric constant and lower moisture absorption give lower capacitance interconnects and thereby higher electronic speeds. Planarizing dielectrics give reliable multilayer interfaces. PBCB appears to have superior dielectric constant, moisture absorption and planarizability properties among others, and therefore is well suited for multilayer/substrate fabrication.

1.1 OBJECTIVE.

The objective of this program was to investigate the properties, processing characteristics, functional performance, and environmental resistance of polybenzocyclobutene (PBCB) resins as dielectric coatings in multilayer thin films for electronic packaging.

1.2 APPROACH.

This program consists of two consecutive phases as described below:

Phase I. Investigation of PBCB Coatings

Task 1. Application of PBCB Coatings to Silicon

Task 2. Fabrication of Multilayer Thin Film Circuits

Task 3. Measurement of Properties of PBCB Coatings

Phase II. Fabrication and Test of Multilayer Thin Film Circuitry

Task 1. Fabrication and Test of Analog Circuit

Task 2. Develop Via Hole Process

Task 3. Assess Merits of PBCB

Both Phase I and II have been completed and the results are summarized in this Final Report.

1.3 MULTILEVEL STRUCTURE.

Figure 1 illustrates the basic concept used throughout this program. Silicon wafers were used as the basic substrate. Layers of PBCB (10 microns thick) were used as dielectric between chromium-copper-chromium (3 microns thick) conductor levels. Via posts of chromium-copper-chromium provided the multilevel interconnections.

During Phase I, a 4-level counter-decoder circuit was fabricated having 3-mil line widths and 0.0075 inch diameter via posts with 5-micron thick PBCB as the dielectric. For Phase II, a more challenging circuit with 1-mil lines, 4-mil spaces, and 10 micron thick via posts and 10 micron thick PBCB for the dielectric was fabricated.

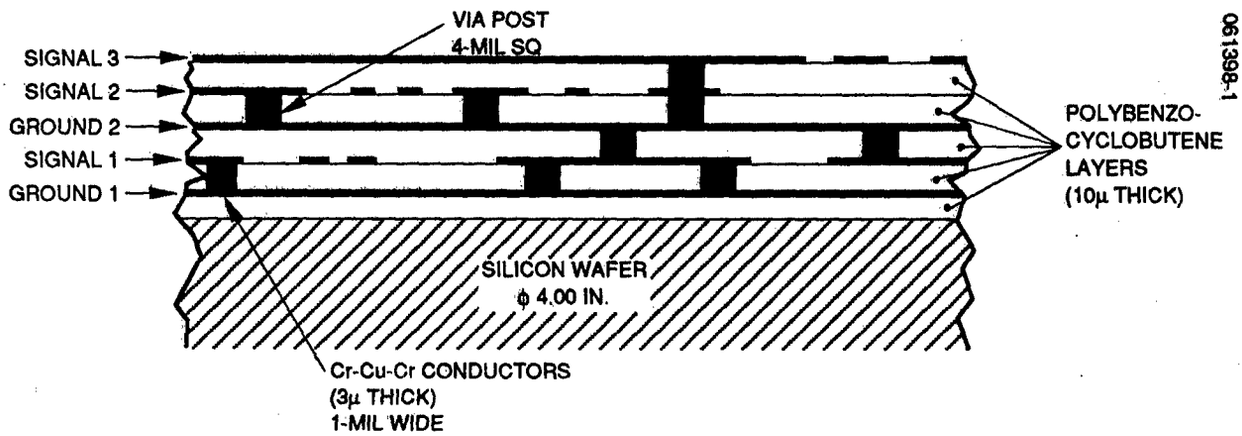

Figure 1. Cross section of analog test circuit.

2.0 PROGRAM SCHEDULE

Figure 2 shows the basic program. All tasks in Phase I and II have been completed.

PROGRAM INVESTIGATION OF PBCB RESINS

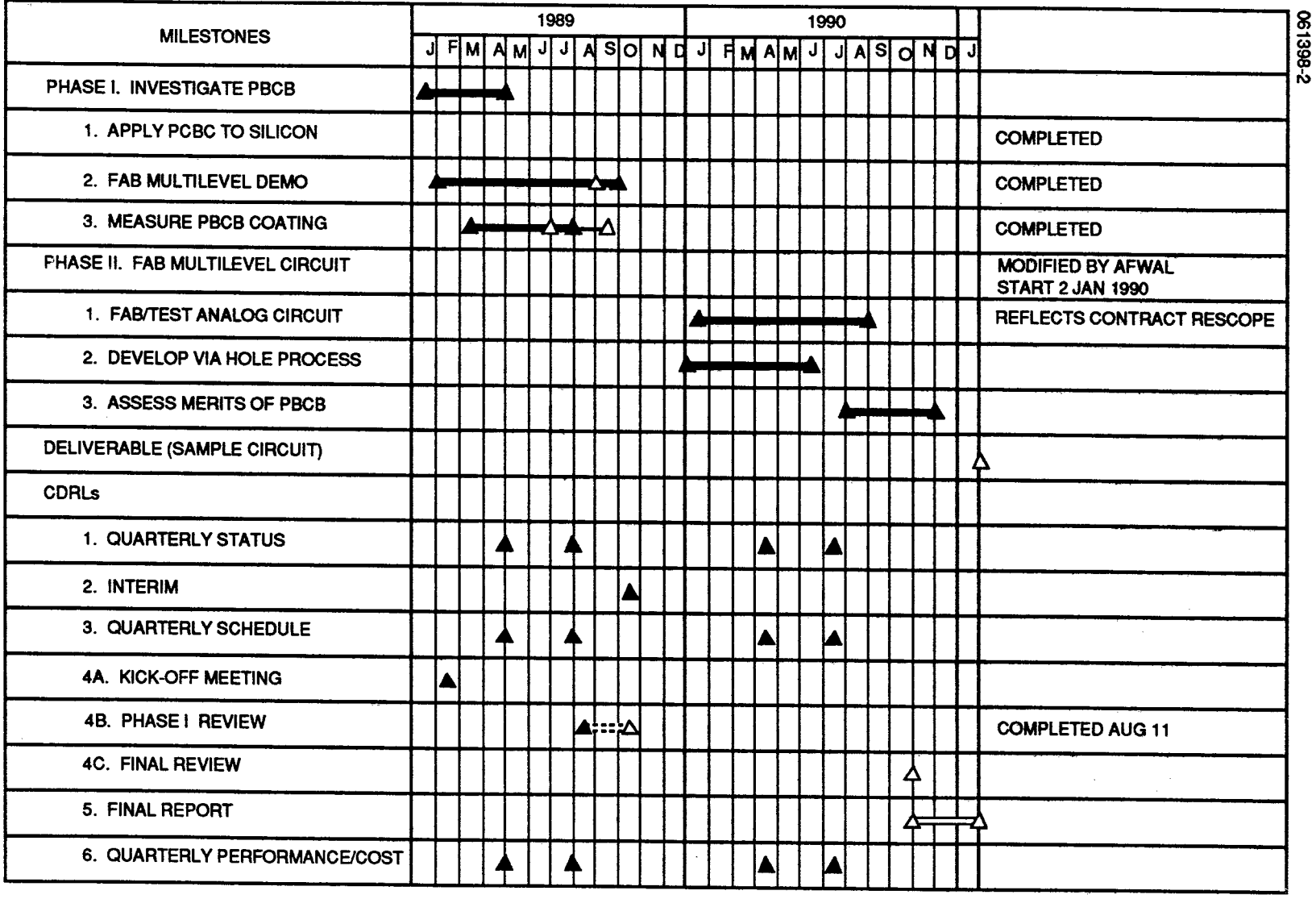

Figure 2. Program schedule.

3.0 PHASE I RESULTS: INVESTIGATION OF PBCB COATINGS.

The significant results of the three tasks in Phase I including: 1) the measurement and properties of PBCB Coatings, 2) the application of PBCB Coatings to silicon, and 3) fabrication of multilayer thin film circuits are summarized in Section 3.0.

3.1 MEASUREMENT AND PROPERTIES OF PBCB COATINGS

Polybenzocyclobutenes (PBCB) are a general class of thermoset resins derived from bisbenzocyclobutene monomers of the generic form shown in Figure 3. The properties of the polymer may be tailored for particular applications by altering the R Group which has been reported previously by DOW Chemical Company (6). In the subject application of PBCB as a multilevel dielectric, the R Group is [-CHCHSi$(CH_3)_2$OSi$(CH_3)_2$CHCH-].

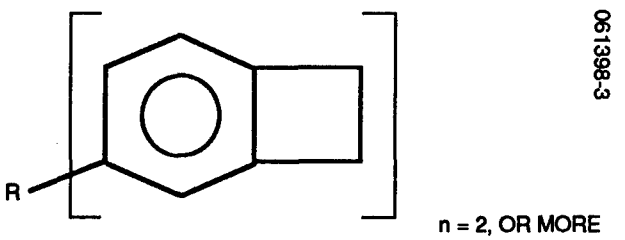

Figure 3. Generic bisbenzocyclobutene monomer.

Benzocyclobutene (BCB) prepolymer was supplied directly to Hughes by DOW Chemical after "b-staging," or partial polymerization of the bisbenzocyclobutene monomer incorporating the previously designated R substituent group. After the spin application of the BCB prepolymer to the silicon wafer, the material was cured in pure nitrogen at 250°C. The material polymerizes in a thermally activated self reaction without catalysts and without the release of volatiles during the cure.

3.1.1 Water Absorption

Water Absorption of water by dielectric films can significantly increase the dielectric constant and thus alter the desired line impedance and packing density of interconnect lines. Following the exposure of a 5.23 micron PBCB film to moisture using a Mitsubishi Moisture Analyzer at 85°C and 85 percent humidity for 168 hours, moisture absorption was 0.023 percent by weight indicating excellent moisture resistance.

3.1.2 Outgassing

No Outgassing tests on PBCB were actually conducted, however residual gas analysis (RGA) tests on Dupont 2611D polyimide films were done by the Hughes Industrial Electronics Group (7). The water vapor levels inside a hermetic package containing polyimide films was less than 1000 p/m. This passes the MIL-STD-883-C, Method 5011 which requires less than 3000 p/m. Since the moisture absorption of 2611D is 0.34 percent and that of PBCB is 0.023 percent, no problem is anticipated with PBCB in a hermetic package environment.

3.1.3 Chemical Stability

PBCB films exhibit excellent chemical stability and resistance to typical metal etching processes including chromium, copper, nickel and gold etchants as well as photoresist stripper, xylene, trichloroethane and isopropyl alcohol. PBCB can be plasma etched in $SF_6/0_2$. These results have been verified by Hughes.

3.1.4 Thermomechanical-Mechanical Properties

The thermomechanical properties of interlevel dielectric materials influence the electrical and mechanical performance of multilevel structures. Table 1 shows the thermomechanical properties of PBCB measured by MCC (7).

TABLE 1. MECHANICAL PROPERTIES
POLYMER DIELECTRICS

PROPERTY	PBCB
FLEXURAL STRENGTH (MPa)	40
FLEXURAL MODULUS (GPa)	3.4
COEFFICIENT OF THERM, EXPANSION [(p/m)/°C])	64

Stress. Because stresses between materials are related to both coefficient of thermal expansion (CTE) differences and moduli, it is possible to have combinations of materials which have equal thermally generated stress levels but difference CTE mismatches. Although the CTE of PBCB is significantly different from silicon [4 (p/m)/°C] or copper [16 (p/m)/°C], the unusually compliant property of PBCB, indicated by its low flex modulus of 3.3 GPa, enables it to tolerate dimensional changes without generating high stress levels.

Table 2 shows stress various polyimides and PBCB. Low stress is one advantage of DuPont 2611 polyimide. Figure 4 is a stress vs. temperature profile for a 25 micron thick PBCB film on a silicon wafer. This data is unique with MCC (8) and is measured in an oven using two laser beams.

TABLE 2. STRESS TEST RESULTS
(COURTESY OF MCC, AUSTIN, TEXAS)

MATERIAL	STRESS (MPa)
PBCB	40
DUPONT 2525	38
**TORAY	38
**CIBA GIEGY 87707	38
PARYLENE C	34
HITACHI L110	10
DUPONT 2611	4

**PHOTOIMAGIBLE POLYIMIDE

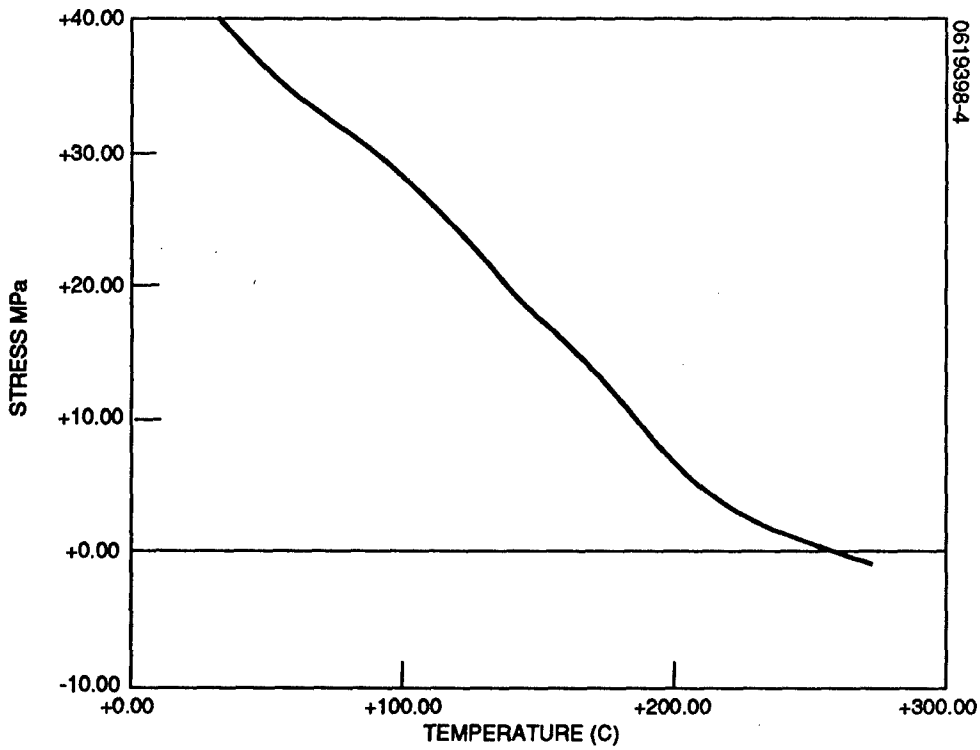

Figure 4. Stress versus temperature for a 25 micron PBCB film on silicon

180° Shear Test. To conduct this test, a silicon wafer is coated with PBCB, broken in half and then one half is peeled back over the other at 180° . The film should remain intact. As a further measure of adhesion and flexibility PBCB films passed the 180° shear test.

Warpage. Warpage of the silicon wafer induced by the cure shrinkage of PBCB films was determined from a test specimen consisting of a silicon wafer (0.021 inch thick x 4 inch diameter) on top of which was deposited five each alternating layers of chromium-copper-chromium (3 microns thick) and PBCB (10 microns). The recorded warpage of 0.032 inches was somewhat greater than the warpage produced with polyimide but still considered satisfactory.

3.1.5 Electrical Properties

The dielectric constant and dissipation factor of PBCB films on silicon wafers were measured at five different frequencies (1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz) before and after relative humidity/temperature exposure (85 percent RH, 85°C, 168 hours). The capacitor test pattern consisted of 1 micron thick aluminum top and bottom electrodes and 5.1 micron thick PBCB dielectric film. The variation in dielectric constant before and after humidity exposure as functions of frequency is shown in Figure 5. After aging the capacitors for 168 hours at 85°C/85 percent RH the dielectric constant changed from 3.0 to 2.7 remaining stable from 1 kHz to 10 MHz. The dissipation factor measured at 10 kHz was 0.0027. DOW has recently reported the dielectric constant and dissipation factor of PBCB at 1 MHz to be 2.7 and 8 x 10^{-4} respectively (9). The PBCB films exhibit a desirable low dielectric constant and due to its moisture resistant nature resists the uptake of water molecules which degrade these electrical properties. Because of the lower dielectric constant of PBCB films, the wave propagation velocity is higher than in materials such as silicon dioxide and polyimides. This property is advantageous for transmission line applications since signal delays are less and capacitance is lower. Table 3 compares critical properties of nine different polyimides with PBCB. PBCB has a lower dielectric constant and lower water absorption than any polyimide, but the coefficient of thermal expansion (CTE) is higher.

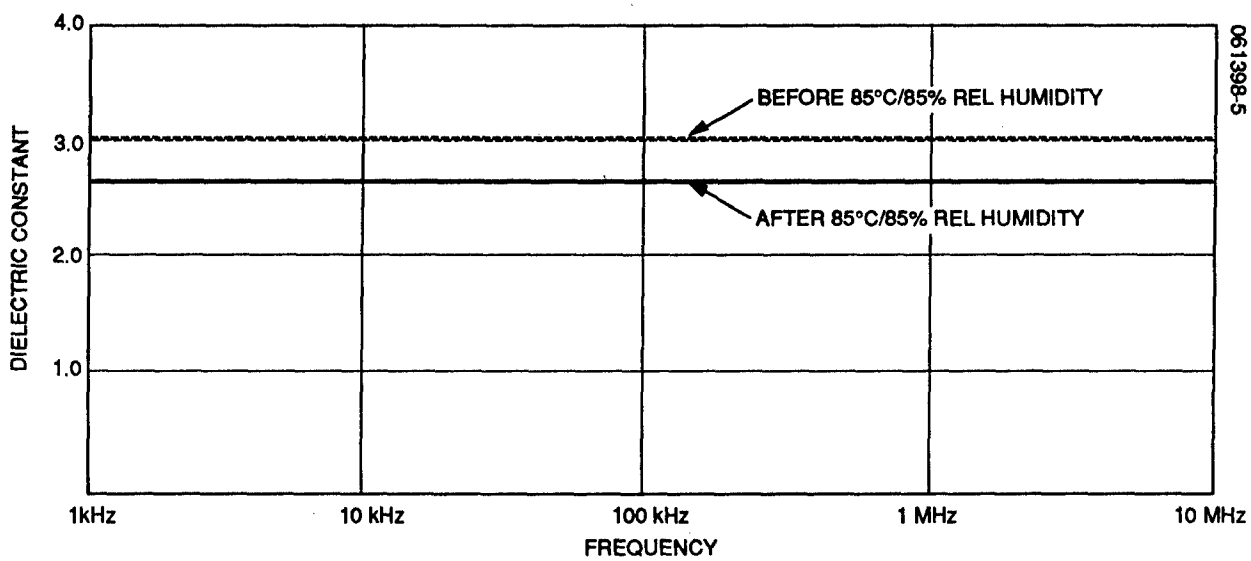

Figure 5. Dielectric constant of PBCB

TABLE 3. PBCB AND POLYIMIDES PROPERTY COMPARISON

POLYIMIDE TYPE	DIELECTRIC CONSTANT (3.9 MAXIMUM AT 1000 Hz, 25°C)	CTE (ppm/°C)	WATER ABSORPTION (MINIMUM PERCENT BY WEIGHT)	WARPAGE (MINIMUM IN MM)	ADHESION PROMOTER (INTERNAL OR SPIN DRY IF EXTERNAL)
CIBA GEIGY 293	3.30	28	4.80		EXTERNAL/SPIN DRY
DUPONT 2525	3.60	40	1.36		EXTERNAL/SPIN DRY
DUPONT 2555	3.60	40	2.52		EXTERNAL/SPIN DRY
DUPONT 2574D	3.60	40	1.68	0.15	INTERNAL
DUPONT 2611D	2.90	3	0.34	0.028	EXTERNAL/SPIN DRY
HITACHI PIQ-L100	3.10	3	1.56		EXTERNAL/350°C BAKE
HITACHI PIX-L110	3.40	5	0.55	0.048	INTERNAL
NATIONAL STARCH	2.80	30-50	2.00		EXTERNAL/350°C BAKE
TORAY SP-840	3.40	30	1.55		INTERNAL
PBCB	2.66	64	0.18	0.13	NOT REQUIRED

3.2 APPLICATION OF PBCB COATINGS TO SILICON

The compatibility of PBCB with silicon wafer processing was evaluated by examining 1) the adhesion of the films with various conductors and silicon, 2) the spin application to wafer substrates, 3) the curing characteristics of the films, 4) the planarization of the films over irregular surfaces and 5) the coating uniformity of the films.

3.2.1 Adhesion

Adhesion tape tests were conducted by applying a strip of 3M # 5910 tape to the film. The tape was then peeled off and examined for evidence of any PBCB or metal adhesion of PBCB to other metal films. Table 4 shows the results of adhesion of PBCB to other metal films. Table 5 shows the results of adhesion of metal films to PBCB. In both cases results are compared to Hitachi L110 polyimide. Adhesion of PBCB coatings on silicon and metals were satisfactory. All metal coatings over PBCB were satisfactory.

Sebastian PIN testing was done by epoxy bonding a small pin head (2.7 mm diameter) to the film and peeling the pin normal to the bonded surface at a preset rate. Table 6 shows the PIN test results of PBCB and two different polyimides spin coated on various metal films. Table 7 shows the similar results of metal films deposited on PBCB and on the two different polyimides.

TABLE 4. TAPE TEST RESULTS, ADHESION OF PBCB TO OTHER MATERIALS

MATERIAL	PBCB		HITACHI L110	
	PASS	FAIL	PASS	FAIL
SILICON	X		X	
Cr/Cu FILM	X			X
Cu FILM	X			X
Al FILM	X		X	
Cr FILM	X		X	

TABLE 5. TAPE TEST RESULTS, ADHESION OF METAL FILMS TO PBCB AND L110 POLYIMIDE

METAL FILM	PBCB		HITACHI L110 POLYIMIDE	
	PASS	FAIL	PASS	FAIL
COPPER	X		X	
ALUMINUM	X		X	
CHROMIUM-COPPER	X		X	

TABLE 6. SEBASTIAN PIN TEST RESULTS, PBCB AND POLYIMIDE TO METAL FILMS

MATERIAL	PBCB (MPa)	DUPONT 2611 POLYIMIDE (MPa)	HITACHI L110 POLYIMIDE (MPa)
COPPER	24.1	–	–
Cr/Cu/Cr	22.0	–	–
ALUMINUM	–	29.5	20.5
SILICON	46.8	30.0	16.6

TABLE 7. SEBASTIAN PIN TEST RESULTS (METAL FILMS TO PBCB AND POLYIMIDE)

MATERIAL	PBCB (MPa)	DUPONT 2611 POLYIMIDE (MPa)	HITACHI L110 POLYIMIDE (MPa)
ALUMINUM	21.4	40.7	35.0
Ti/W/Au	–	35.2	22.1
COPPER	50.3	–	–
Cr/Cu	31.0	–	–

3.2.2 Spin Application of PBCB to Silicon

PBCB films were applied to silicon wafers by spinning using a photoresist spinner. Table 8 shows the variation of film thickness with spinning rate. The results are comparable with polyimides. The PBCB was applied as a 55 percent solution in xylene. The kinematic viscosity of PBCB at 24°C using a Cannon-Manning Semi-Micro calibrated viscometer was 119 centistokes.

TABLE 8. SPINNING SPEED VERSUS FILM THICKNESS

SPINNING SPEED (r/min)	PBCB THICKNESS (μm)
1500	10.00
3000	5.23
5000	4.42
7000	3.98

3.2.3 Curing of PBCB Films

Unlike polyimide films, PBCB is very sensitive to oxygen and must be cured in a pure nitrogen atmosphere. If too much oxygen is introduced into the PBCB during the cure cycle, several important properties are adversely affected including dielectric constant, chemical resistance, and flexibility. The PBCB was typically cured at 250°C for 60 minutes in nitrogen containing less than 0.05 percent of oxygen. Figure 6 is a Fourier Transform Infrared (FTIR) spectrum of PBCB. The oxygen peak is at 1701.2 cm-1. If the oxygen peak of the cured PBCB film is less than 70 percent transmittance, the films are unsatisfactory.

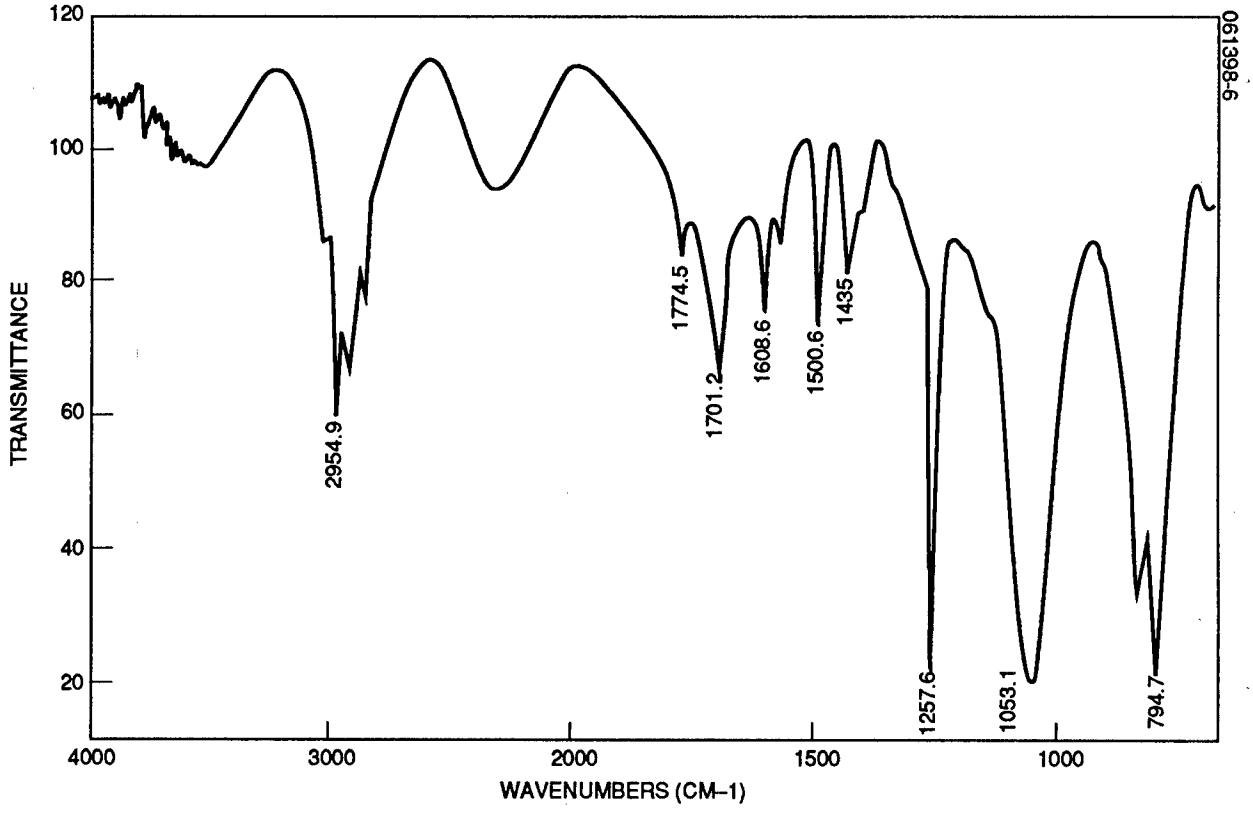

Figure 6. FTIR spectrum of PBCB film on silicon

3.2.4 Planarization

The ability of the dielectric film to planarize (or smooth out) a rough, irregular surface is important for processing multilevel circuits, particularly those with four or more conductor levels. The surface roughness (non planarity) of a 10 micron thick PBCB layer over a series of rough copper surfaces (3 microns) was determined using a Sloan Dektak II A Surface Analyzer.

The surface was planar to within 600 Angstroms. Figure 7 contrasts the superior planarization of PBCB with Hitachi L110 polyimide which was only planar to within 32,000 Angstroms. The rougher the surface, the more probability of shorts or opens with the subsequent dielectric/conductor levels.

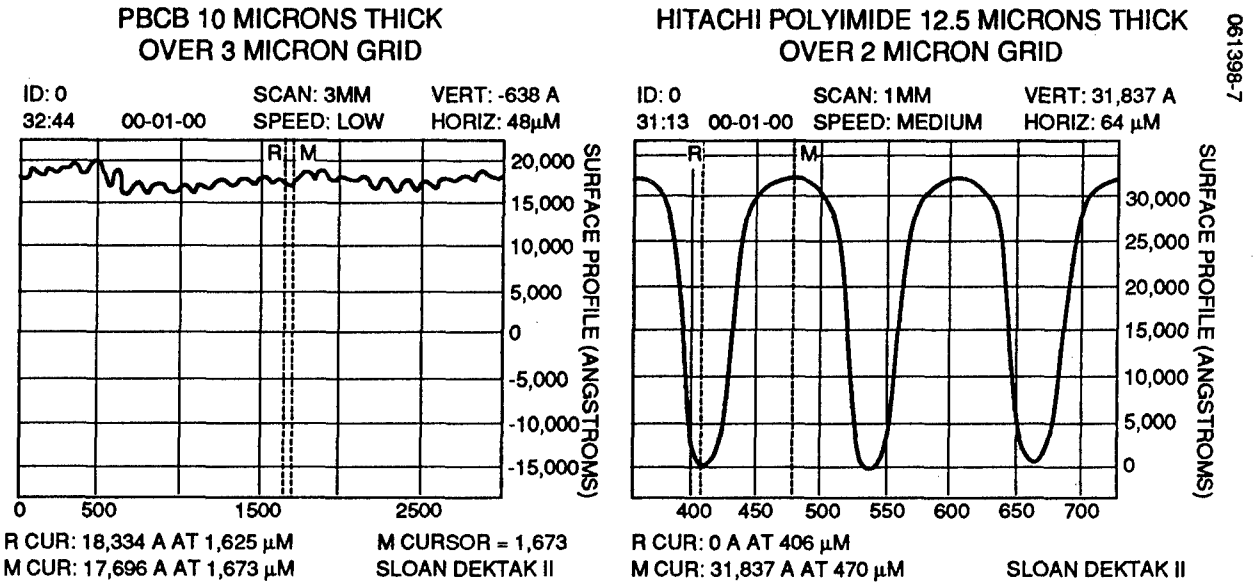

Figure 7. PBCB and polyimide planarizability

3.2.5 Coating Uniformity

Another property related to planarization is uniformity. Table 9, courtesy of Dow Chemical, shows the coating uniformity data on a 5 inch wafer. The coating thickness was measured by a profilometer. The table describes the amount of PBCB dispensed, spin conditions used and the number of measurements taken for determining the mean thickness. Table 9 also shows the effect of spread cycle (500 r/min) and spin time when using the spread cycle. Thicker coatings were obtained when the spread cycle was used and thickness increased with an increase in time for the spread cycle. However, in all cases, the coating uniformity was very good, with a standard deviation < 1.4 percent.

3.3 FABRICATION OF MULTILAYER THIN FILM CIRCUITS

PBCB Multilayer films were evaluated for electronic packaging using a simple counter/decoder circuit width of 76.2 μm (0.003 inch) and line spacing 177.8 μm (0.007 inch). The circuit utilized via post interconnects in contrast to via holes. Figure 1 illustrates the via post

TABLE 9. PBCB (55 PERCENT) COATING UNIFORMITY ON 5 INCH WAFER

# DETERMINATIONS	11	7	10
MEAN THICKNESS (μM)	7.25	6.80	6.63
% STANDARD DEVIATION	1.0	1.4	1.4
DISPENSE VOLUME (cc)	3.0	3.0	3.0
SPIN CONDITION (30 sec/3000 rpm)	10 sec SP CYCLE	5 sec SP CYCLE	NO SP CYCLE

interconnection layout. PBCB is a suitable multilevel dielectric; it survived all of the normal multilevel processing steps. However, the counter/decoder was not particularly difficult to fabricate from the standpoint of line width and spacing.

3.3.1 Counter/Decoder Circuit

The parameters for the counter/decoder circuit are listed in Table 10. PBCB dielectric films exhibited the capability of nearly completely planarizing the via post needed for level to level interconnect. Some undercutting of the copper post beneath the chrome top led to a minor photoresist shadowing difficulty which was overcome by re-exposing a second application of photoresist with the post line pattern to eliminate possible undercutting at the edge. Figure 8 shows a typical via post. The post height is designed to match the dielectric thickness so that level to level interconnection is completely planar. The via posts are made of chromium-copper-chromium deposited by electron beam evaporation.

TABLE 10. PARAMETERS FOR COUNTER/DECODER CIRCUIT

CIRCUIT PARAMETERS	COUNTER/DECODER CIRCUIT
LINE WIDTH	0.003 IN.
LINE SPACING	0.007 IN.
VIA POST SIZE	0.0075 IN.
CIRCUIT SIZE	1-1/2 IN. SQ.
NO. OF ACTIVE CHIPS/CIRCUIT	6
NO. OF PASSIVE CHIPS/CIRCUIT	0
NO. OF CONDUCTOR LEVELS	4
POLYIMIDE THICKNESS	0.00054 IN.
CIRCUITS PER 4 IN. WAFER	4

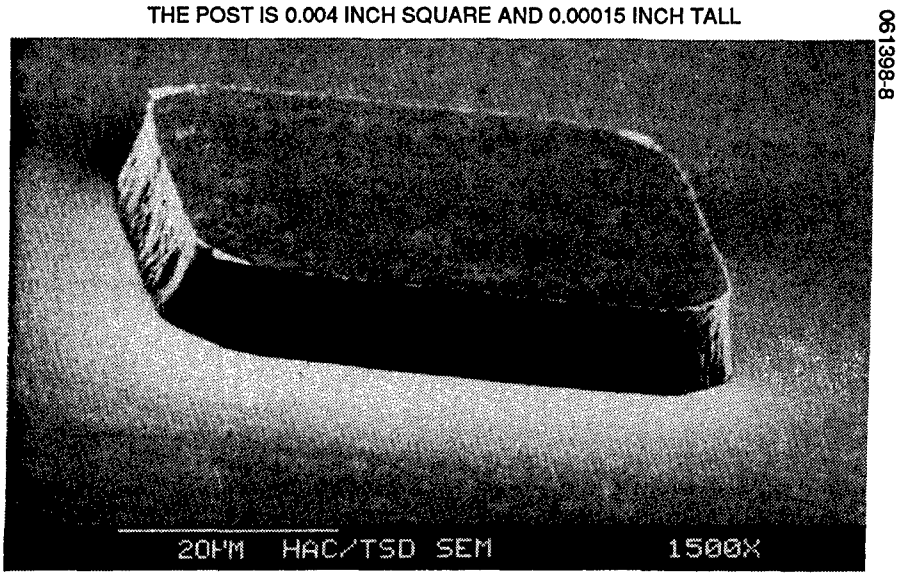

Figure 8. Scanning electron microscope picture of copper via post at 1500 X magnification.

3.3.2 Circuit Fabrication

Two counter/decoder wafers were processed to completion through all four conductor levels. On this initial attempt, the yield was low, with 78 percent of the conductors/vias surviving. The predominant failure modes were conductor opens and via post opens. However, none of these failures were related to the use of PBCB.

Figure 9 shows a 4-inch diameter silicon wafer with the ground plane, signal level No. 1, and signal level No. 2 intact. The top conductor level, which is basically chip die attach pads and wire bond pads, had not been processed on this particular wafer.

Die attach and wire bonding pads were formed from 5 microns of electroplated gold on chromium-copper-chromium with 0.4 microns of nickel as a barrier beneath the gold. Figure 10 depicts a typical pad. Metallographic sectioning was performed on a typical via post interconnection to the top signal level as shown in Figure 11 which also depicts the absence of voids in the PBCB. A void is a potential path for an electrical short circuit between adjacent conductor levels. It appears that the PBCB to PBCB wettability renders the material void-free compared to certain polyimides.

Electrical resistance of the chromium-copper conductor was measured to be 0.01 ohms per square. This sheet resistance is adequate for viable layer to layer interconnect in high speed processors.

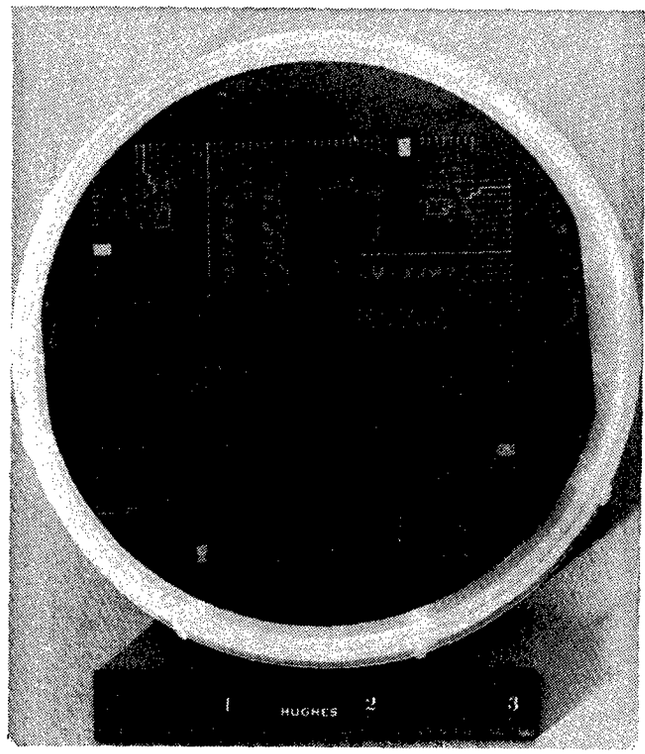

Figure 9. Counter decoder circuit.

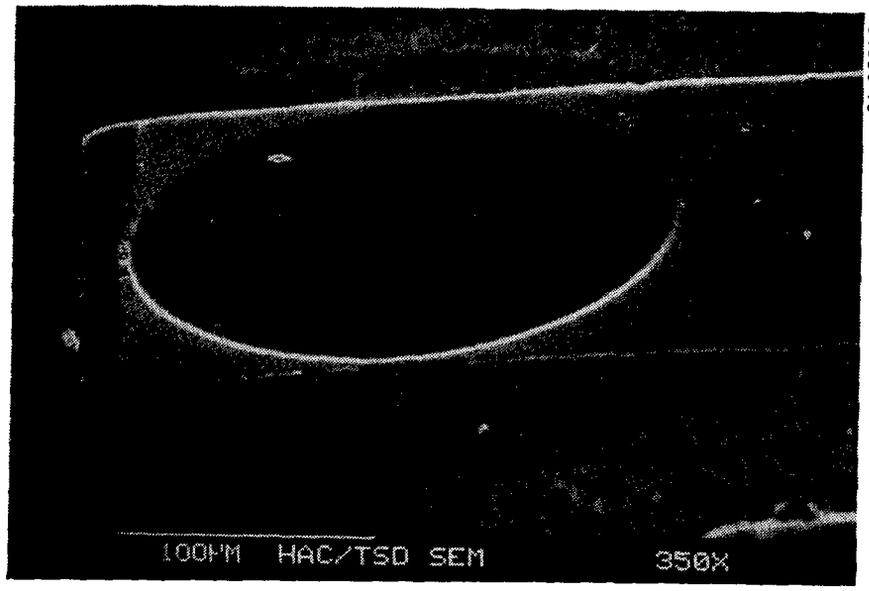

Figure 10. Scanning electron microscope picture of top level wire bond pad and via interconnect.

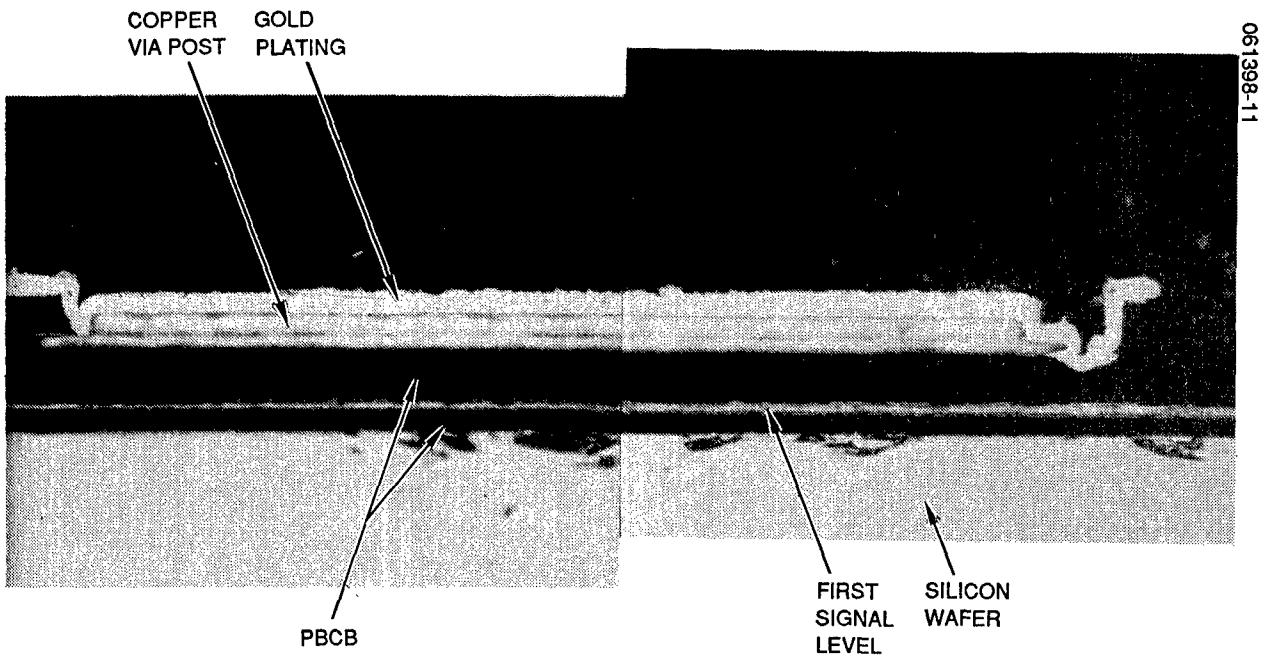

Figure 11. Metallographic section of gold plated via post in 4-level circuit at 1000 X.

Die shear tests were performed on simulated chips (80 x 80 mil die) bonded to gold plated pads (90 x 90 mil) on multilevel PBCB coated silicon wafers. Ablestik 606-2 conductive epoxy used for die attach yielded an average die shear strength of 8.98 kilograms in the MIL-STD-883 Method 2019.3 test. This strength exceeded the 2.5 kilograms needed for passing the test and demonstrates that PBCB is viable for die attach applications.

Wire bond test were performed by pull testing jumper bonds on gold plated pads formed on the fourth conductor level of the PBCB multilayer silicon substrate. Thermosonic bonds were made using 1 mil diameter aluminum wire. Pull tests yielded 11.2 grams and 6.7 grams respectively for ultrasonic and thermosonic bonds per MIL-STD-883, Method 2011.4. The pull test strength on PBCB exceeds the minimum preseal bond strength for aluminum wire of 2.5 grams and gold wire of 3.0 grams.

3.3.3 Circuit Fabrication and PBCB Characteristics

During the counter-decoder circuit fabrication several important properties of PBCB films were verified. It was discovered that a relatively pure N_2 environment during baking was necessary to achieve the low dielectric constant and the necessary chemical resistance of the dielectric films. This is not a difficult requirement and it can be fulfilled using any N_2 purged oven which can sustain 250°C during N_2 flow. During this period it became apparent that PBCB adheres well to copper and vice versa. This is in contradistination to a host of polyimides which would

not adhere to copper. Other metals including aluminum can adhere to PBCB. The single most important and different aspect of PBCB with respect to adhesion is that no adhesion promoter is necessary for processing PBCB.

Planarization. In the course of previous work on fabricating multilayer circuits using Hitachi L110 it was discovered that Hitachi polyimides among others will delaminate from solid ground planes. Therefore, a gridded ground plane was designed to avert delamination when coated with polyimide. The gridded ground plane, however was not planarized and the degree of non-planarization was replicated from layer to layer causing metal coverage difficulties. It was quite surprising to note that when the gridded ground plane was coated with PBCB planarization was nearly complete (~98 percent).

With Hitachi L110 polyimide, the nonplanar topography of the 3 micron grid was reproduced after 12.5 microns of Hitachi L110 polyimide coverage. The same grid was planarized to within 600 angstroms by a 10 micron thick PBCB film. This represents a factor of 50 reduction in topography contour difference.

Before the inception of the current program it was envisioned that an alternate interconnection scheme from one dielectric layer to another dielectric layer would require via posts. However in the implementation of via post interconnect it was discovered that the 9.5 micron high post, needed to connect through 12.5 microns of polyimide, was not planarized by Hitachi L110. The accumulation of polyimide resulted in excessive polyimide etching time during via window opening. After all the polyimide on top of the post was etched, a trench around the post was found to have formed making connection across the post extremely difficult. PBCB, however was found not to accumulate on top of the post and the small fraction of 1 micron PBCB remaining on the post top through 10 microns of PBCB coating was easily etched without trench formation. The planarizing property of PBCB removed the most difficult aspect of layer to layer interconnection.

4.0 PHASE II RESULTS: FABRICATION OF MULTLAYER THIN FILM CIRCUITRY

The results of the three tasks in Phase II including: 1) development of via hole process, 2) fabrication and test of analog circuit and 3) assessment of merits of PBCB are documented in Section 4.0.

4.1 DEVELOPMENTAL OF VIA HOLE PROCESS

For complex interconnection and distribution of signals through the use of multilayer metal and polyimide, interconnections from layer to layer can be made through vias as shown in Figure 12.

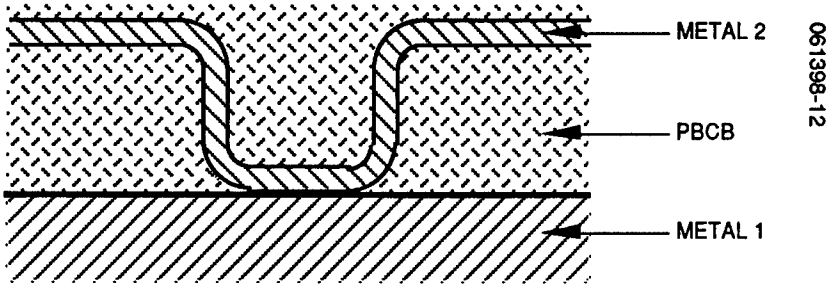

Figure 12. Via hole interconnect

With polyimide, a via can be formed by sputter depositing SiO_2 onto polyimide followed by plasma (CF_4) etching to open a via window in the SiO_2 and then plasma etching the polyimide using pure oxygen. Since barrel etching is an isotropic process a smooth transition slope is obtained at the via rim when the via window in SiO_2 is etched. This smooth edge is imprinted onto the polyimide during the etch in oxygen.

For dielectric layers employing PBCB, masking cannot be made from SiO_2 alone since the fluorine component needed to etch PBCB also etches SiO_2. In attempting to preserve a smooth transition edge at the via rim, masking is made from SiO_2 capped with aluminum. Photolithography and wet etching are used to open via windows in the aluminum masks. This is followed by plasma etching of SiO_2 using O_2/SF6 which sequentially etches the PBCB beneath the SiO_2. When the PBCB is completely etched as evidenced by seeing the underlying metal through the via, the SiO_2 and aluminum masks are removed. This completed the via hole process employing the PBCB dielectric. A flow diagram describing the via hole process with the PBCB dielectric is shown in Figure 13.

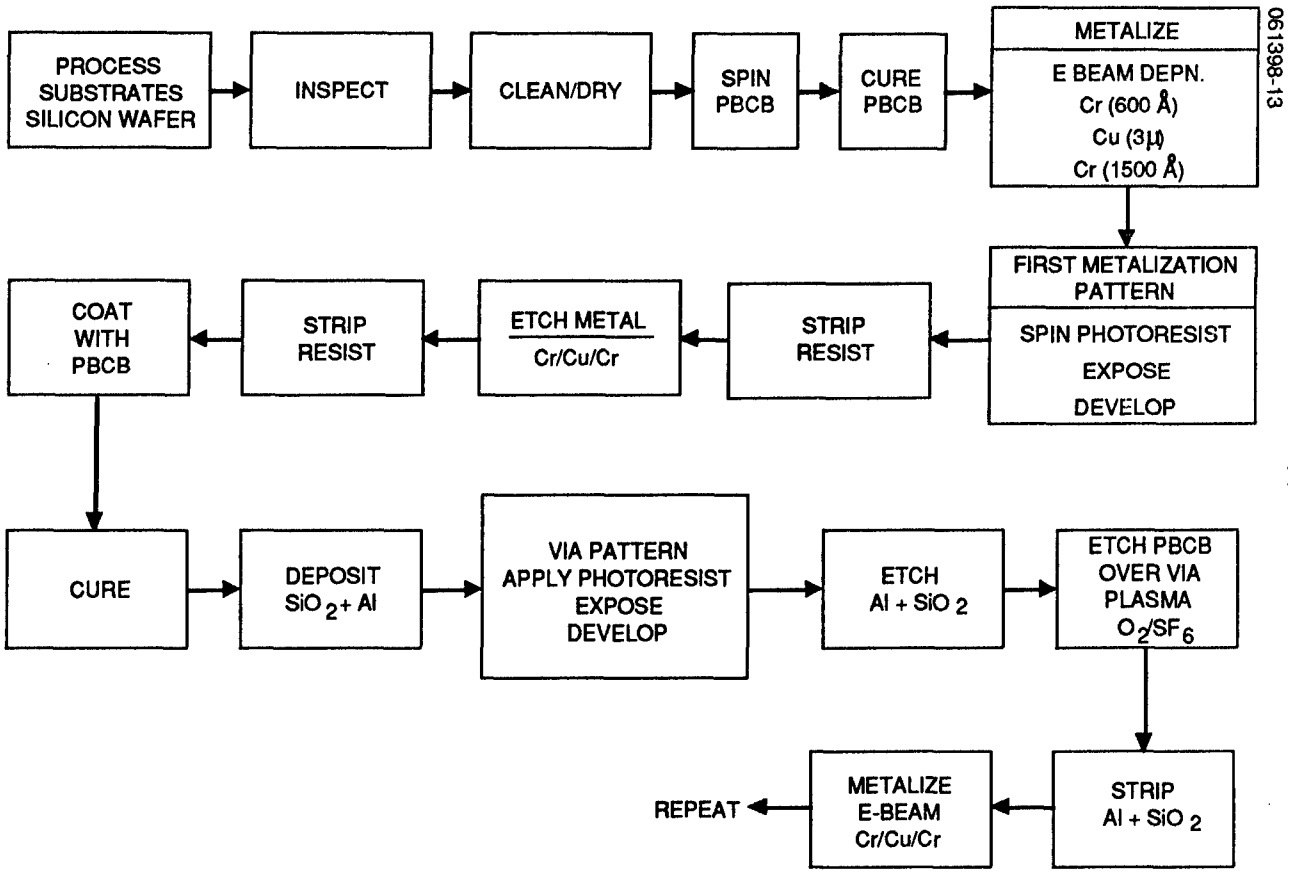

Figure 13. Etched-back via process

4.1.1 Via Hole Fabrication

The conventional via hole interconnect method was accomplished by the following process steps. Cr/Cu/Cr was deposited on the silicon wafer to form the ground plane. Ten microns of PBCB was deposited onto this wafer. To form the mask 300 A of SiO_2 and 10,000 A of A1 were sequentially deposited onto the wafer. SiO_2 deposited using RF sputtering, is used to enhance the slope formation in the PBCB during plasma etch. Aluminum is used to protect the SiO_2, which is readily eroded away by the fluorine compound in the plasma etching gas. Photolithography is performed using a via mask to open up windows in the A1 layer. O_2/SF6 plasma etching readily etches through the SiO_2 and the PBCB. Mask removal was followed by the deposition of interconnect metal. Photolithography was performed to define the interconnect path linking the vias.

4.1.2 Via Hole/PBCB Results

Via resistance was measure to be 0.3 ohms. This resistance can be considerably reduced if RF sputtering deposition instead of electron beam evaporation is employed to form the interconnection metal. Figure 14 shows the sloped via hole profile. A DekTak profilometer trace of the same via reveals the cross sectioning profile in Figure 15. It is concluded that both via hole and via post processes are viable for interconnection through PBCB although via post interconnects are particularly suited for thick dielectric layers necessary for lower capacitance.

4.2 FABRICATION AND TEST OF ANALOG CIRCUIT

The compatibility of PBCB multilayer thin films were evaluated with a significantly more complex and challenging analog circuit. The relevant circuit parameters are shown in Table 11. This circuit comprises 5 conductor levels (3 signal levels and 2 ground planes) and 5 PBCB layers with a 10 micron dielectric thickness. Signal levels 1,2 and 3 are shown in Figures 16, 17 and 18 respectively. Interconnection was accomplished using via posts as shown in Figure 1. Figure 19 is composite view of this circuit showing signal levels 1,2, and 3 superimposed on top of one another revealing the density of lines. A photograph of a fully fabricated five level analog circuit is shown in Figure 20. Temperature cycling from -55°C to 125°C, 10 cycles, according to MIL-STD-883, Method 1010.5B was conducted on a circuit with two intermediate conductor levels. No detrimental effect from temperature cycling was evident following measurement of DC line resistance.

It became apparent during the fabrication of the analog circuit that PBCB is unique in its planarization property. Fabrication with Hitachi L110 polyimide was attempted using via post interconnects. It was found that for a 12.5 micron dielectric thickness an equivalent thickness of Hitachi L110 was found remaining at the post top. The successful removal of all the polyimide from the post top entails the creation of a moat at the post bottom. This resulted in questionable connection at the post. PBCB was able to completely planarize the post tops leaving a very minute amount of dielectric which could be rapidly etched away without creation of the moat. Line to post connection enabled level to level connection. Lines 1 mil in width were routinely achievable. In situations where sharp corners were encountered unbroken 1 mil lines were possible. This is in contradistinction to the situation using Hitachi L110 where 1 mil lines broke over sharp corners in grids and at the trenches around posts. PBCB planarization also permitted the preservation of the connection to the post in the metal etch step. Using the more demanding feature sizes of the analog circuit it was demonstrated that PBCB was compatible within fine and closely spaced line configurations and that surface irregularities can be completely smoothed out for highly reliable connection between layers.

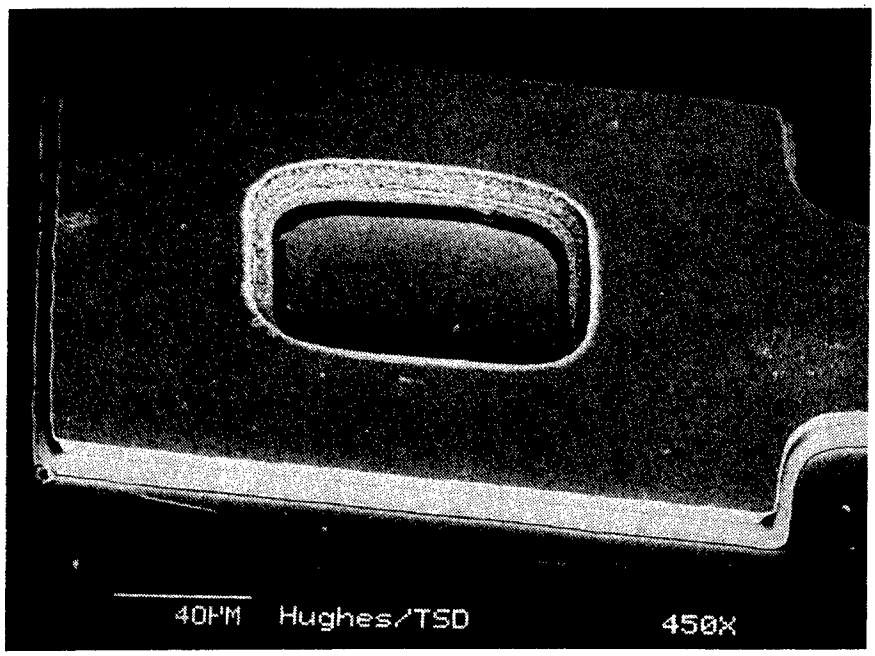

Figure 14. Scanning electron micrograph of via hole with PBCB.

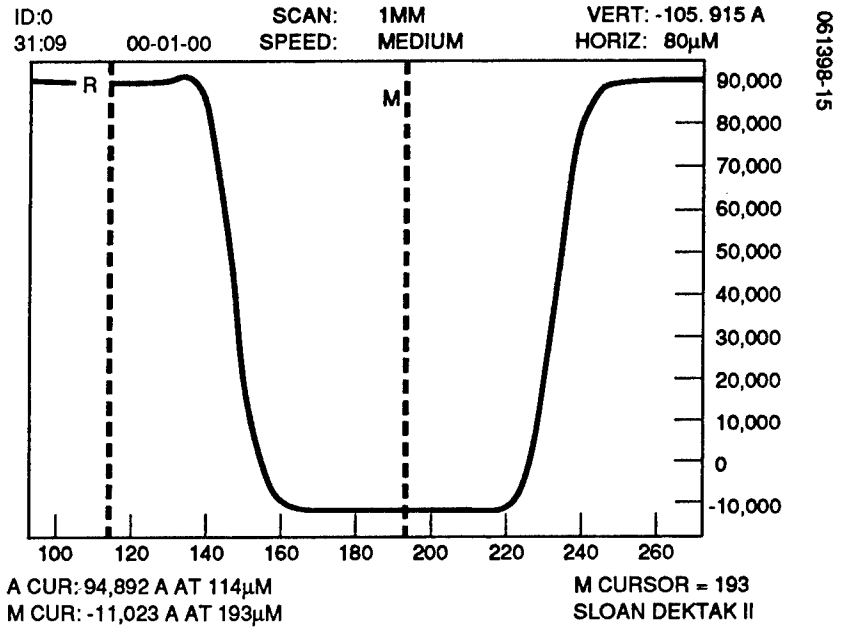

Figure 15. Via hole profile with 10 micron PBCB

TABLE 11. PARAMETERS FOR ANALOG TEST CIRCUIT

PARAMETERS	SIZE/MATERIAL
LINE WIDTH	0.001 INCH
SPACING BETWEEN LINES	0.004 INCH
VIA POST SIZE	0.004 X 0.004 INCH
CIRCUIT SIZE	2.0 X 2.0 INCH
NO. OF CONDUCTOR LEVELS	5
NO. OF PBCB LEVELS	5
SUBSTRATE SIZE	4 INCH DIAMETER
SUBSTRATE MATERIAL	SILICON
PBCB DIELECTRIC THICKNESS	10μm
CONDUCTOR MATERIAL	COPPER
CONDUCTOR THICKNESS	3μm

4.2.1 Analog Circuit Fabrication Process

A 4-inch silicon wafer is cleaned dried and loaded onto a spinner to receive PBCB. Approximately 10 cm^3 of PBCB (55 percent in xylene) is dispensed onto the wafer and allowed to spread to the edge of the wafer. The spinner is set to spin at 1500 r/min for 20 seconds. This is followed by curing in a nitrogen oven, 30 minutes at 100°C, 30 minutes at 150°C and 1 hour at 250°C. Alternatively the PBCB can be cured at 230°C for 4 hours to a final thickness of 10 microns. The PBCB coated wafer is loaded into an electron beam evaporator for successive coatings of Cr/Cu/Cr/Cu/Cr. The first copper coating is 3 microns and the second is 7 microns. The chromium coating, used as adhesion layer and stop etch layer is nominally 1000A. The metallized wafer is coated with negative resist and soft baked. The first signal level to ground plane connection/via post mask is used to expose the photoresist and the photoresist is developed to give the via post image. The wafer is post baked and then successive layers of chromium and copper are wet etched. The wafer is thoroughly rinsed and dried for negative resist coating. The photoresist step above is repeated replacing the via post mask with the ground plane mask. After the post bake step in the above photolithography process, successive layers of Cr/Cu/Cr are wet etched to define the ground plane. The wafer is thoroughly rinsed and bake dried for the dispensation, in the manner mentioned above, of the second PBCB layer. After curing of the PBCB, the wafer is loaded into the electron beam evaporator for the deposition of 1 micron of aluminum which is used as plasma dry etch mask. Negative photoresist is used to produce window images for subsequent etching of windows in the via post positions on the aluminum mask. Plasma etching in O_2/SF6 is used to erode the PBCB until the via post top is exposed and free of debris. The aluminum mask is then stripped and the wafer is bake dried. Multilayers of Cr/Cu/Cr/Cu/Cr

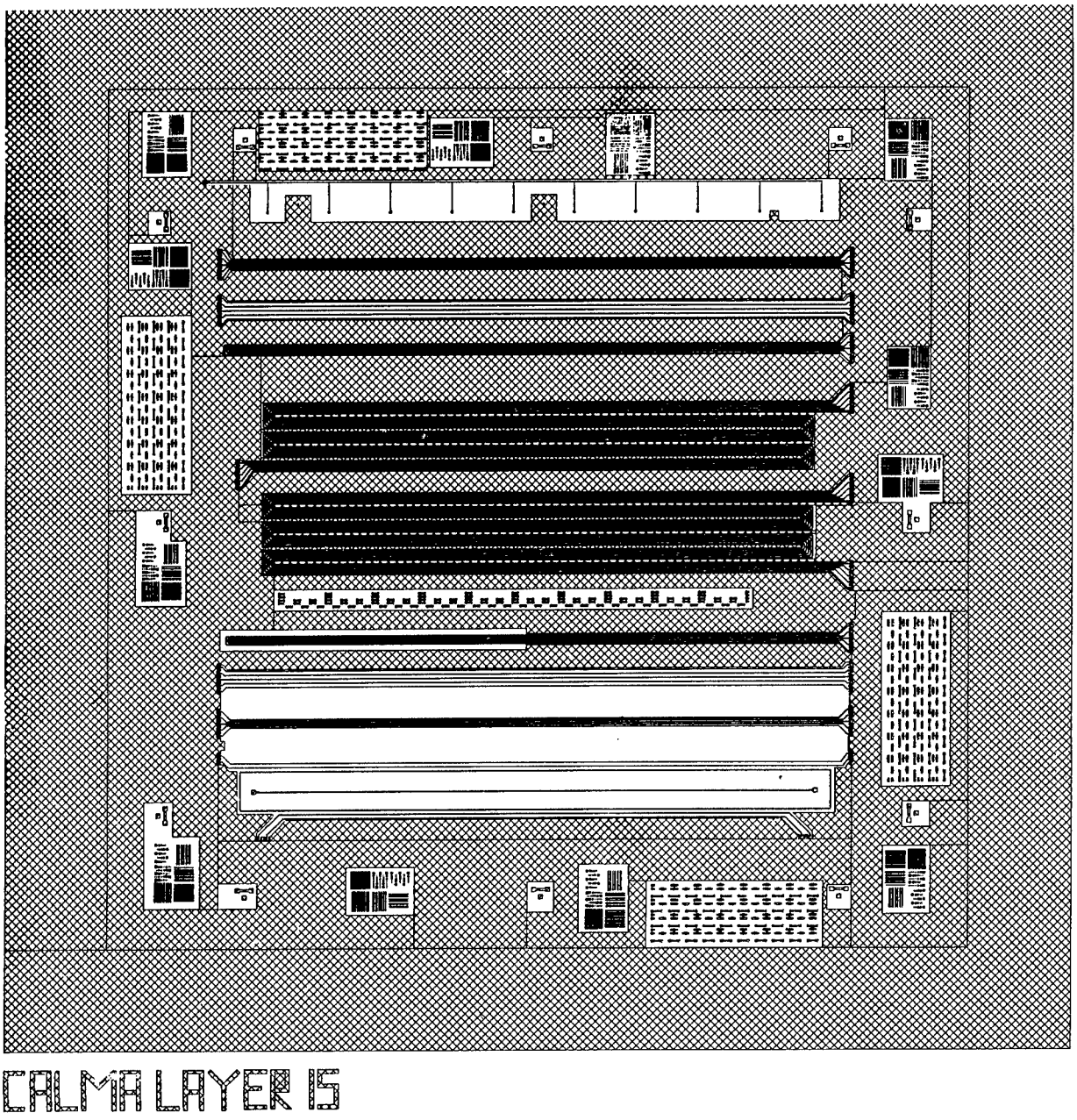

Figure 16. Analog test circuit signal Level 1.

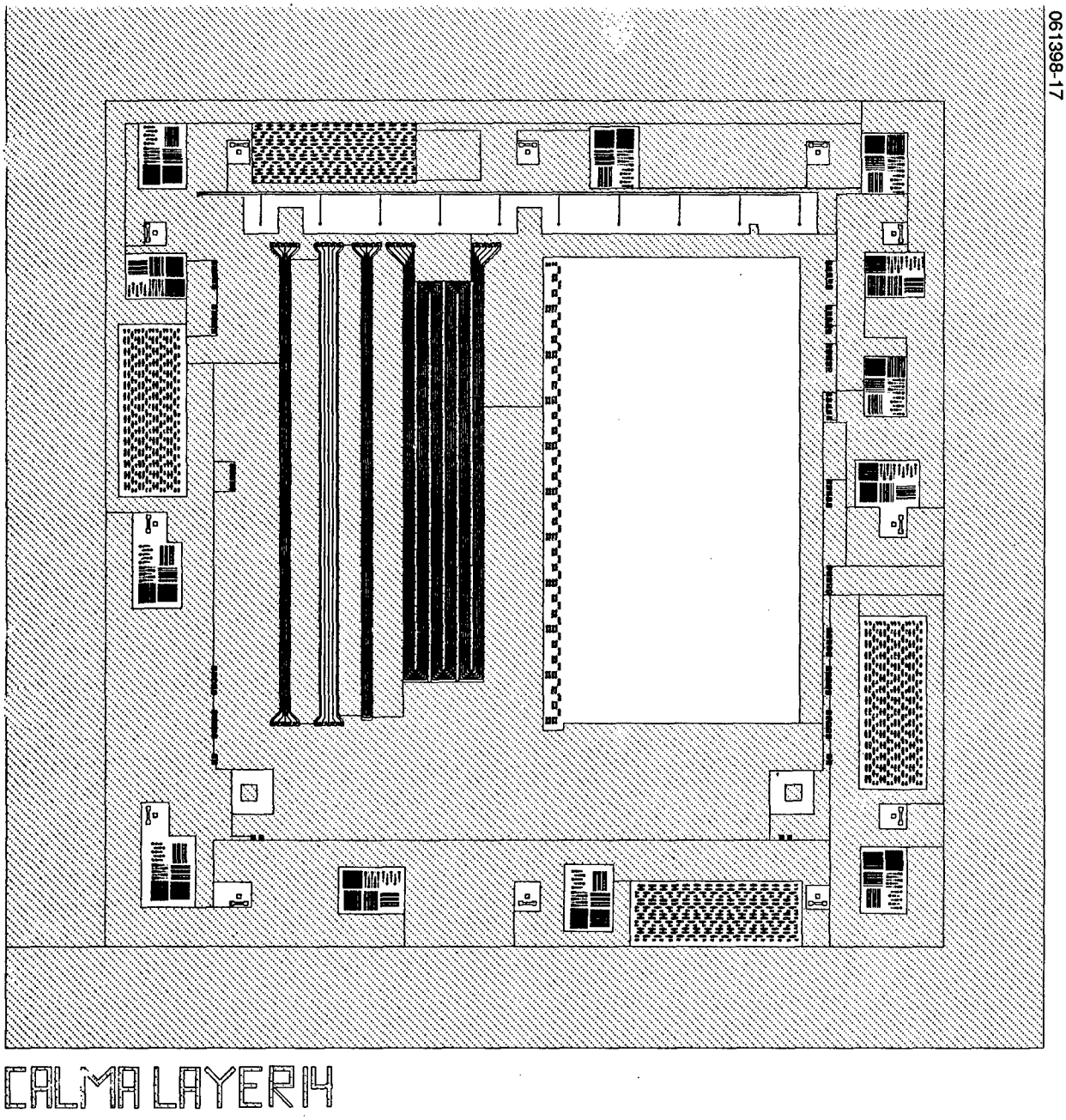

Figure 17. Analog test circuit signal Level 2.

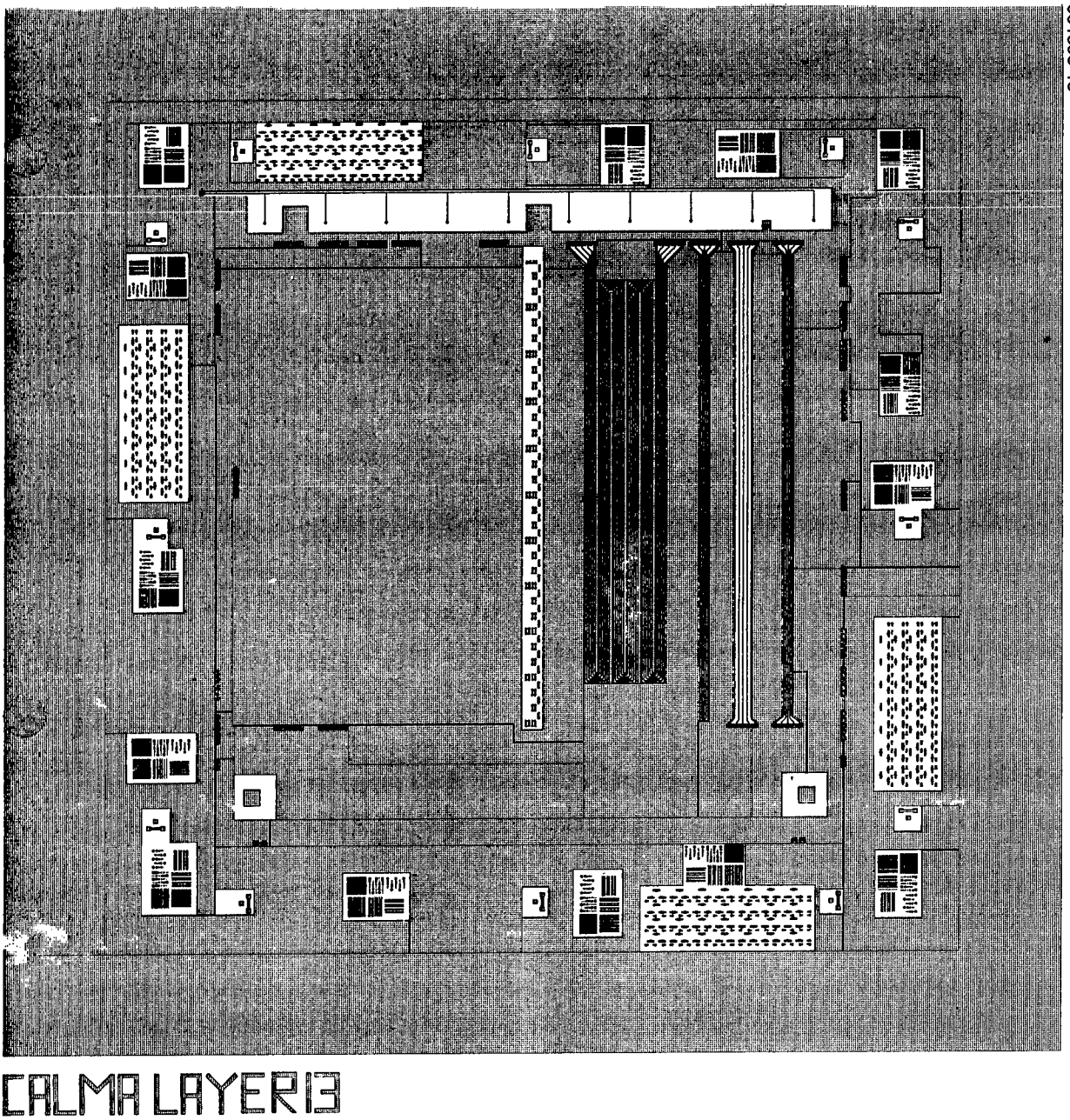

Figure 18. Analog test circuit signal Level 3.

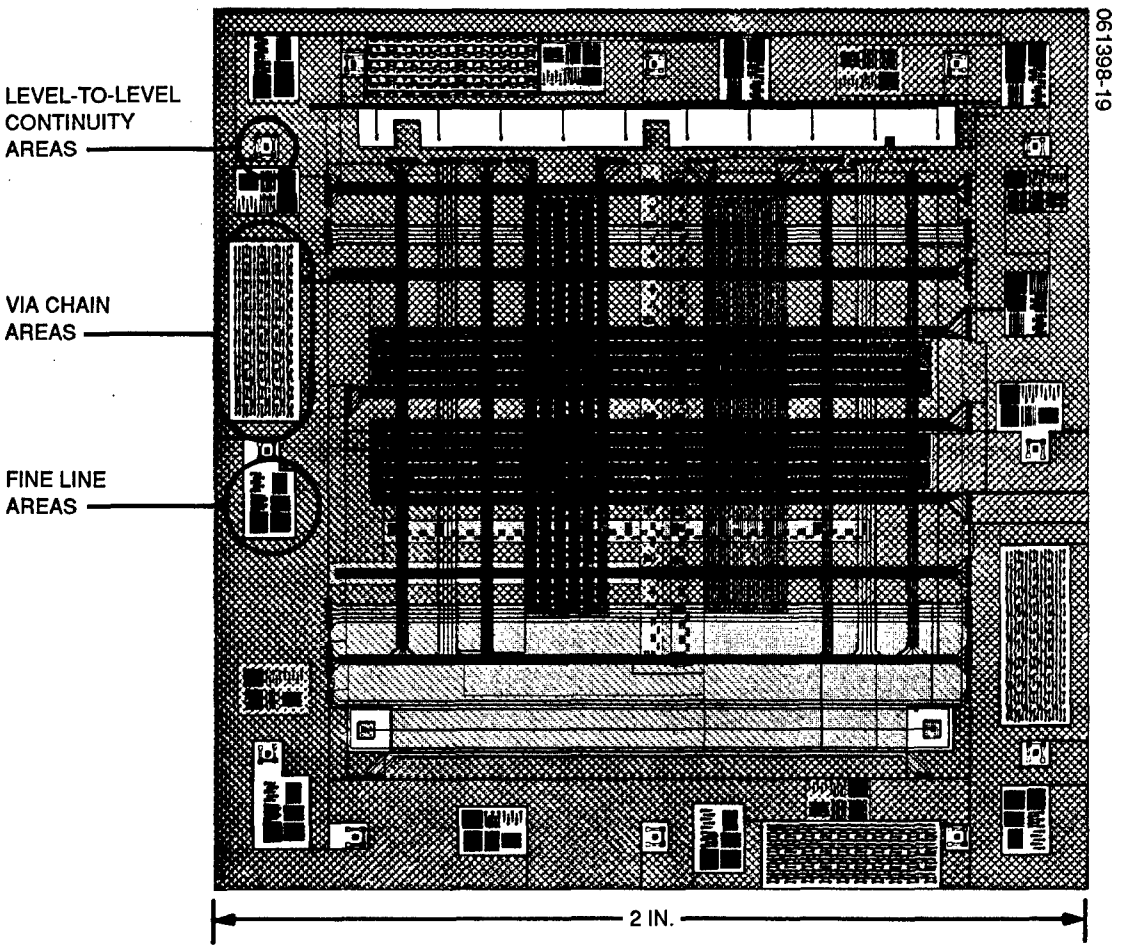

Figure 19. Analog test circuit signal 3 levels composite.

are deposited using the electron beam evaporator. Via post etching and Cr/Cu/Cr etching are carried out in the manner described above to form the first signal layer. Similarly, in the manner described above, five conductor levels are fabricated to interconnect between five PBCB levels in the analog circuit.

4.2.2 Via Post Continuity

The continuity of level to level interconnect was demonstrated using via posts. The via post technology was used to alleviate the difficulties involved in cases of interconnect across thick dielectric layers through increasingly small holes. In these cases where the aspect ratio of dielectric thickness versus the via hole size is very high, the next level of metallization may not reach the bottom metallization before the via filling is complete. The via post allows the bottom metallization to reach through to the metal layer above in all cases. PBCB coverage of the post

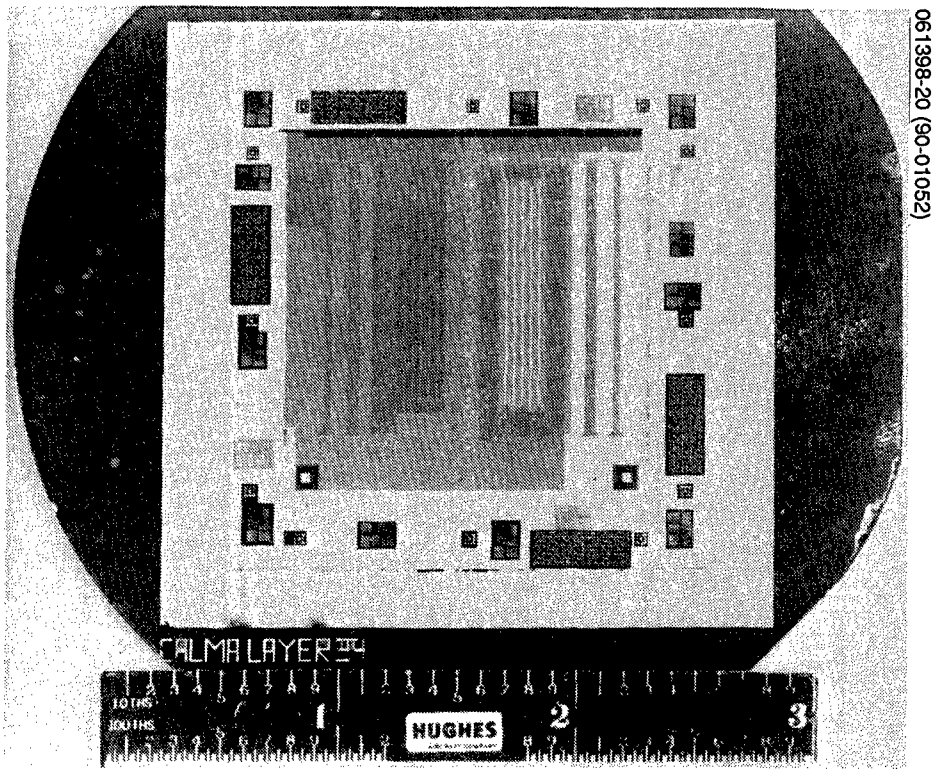

Figure 20. Analog test circuit (5 conductor level).

was completely planarizing and the small amount of PBCB remaining on top of the post was readily removed in the O_2/SF6 plasma etch. Via posts currently yields a nominal interconnect resistance of 0.3 ohms. This resistance can be lowered only if the interconnect site, in this case the top of the post can be cleaned before metal deposition in vacuum. This can be accomplished by replacing the e-beam evaporation of the Cr/Cu/Cr with a sputtered Cr/Cu/Cr process making possible an in-situ sputter clean of the post top removing residual ash.

4.2.3 Analog Circuit Testing Concept and Approach

Developments in device and interconnect technologies have lead to rapid increases in functional density at the board level. Multichip module technologies are pushing densities even higher. High density multilayer interconnect (HDMI) substrates developed at Hughes Aircraft Company use thin film metallization on multilayers of low dielectric constant spin-on polymer. Thin film substrates offer controlled characteristic impedance environments and fine routing features which allow high packing densities at high speeds.

To meet the goals of HDMI multichip modules, a new process was developed which allowed the deposition of altering layers of thin film metallization using chrome/copper/chrome and

spun-on polymer. Multilayer substrates require excellent planarization qualities in the polymer. Existing polyimides do not meet these requirements. A new polymer material, polybenzocyclobutene (PBCB), has demonstrated superior planarization characterization. To understand the operating envelope of PBCB, a five conductor layer analog test circuit was fabricated. The analog test circuit was design to acquisition of electrical data using controlled impedance probes. The analog test circuit when used in conjunction with Tektronix P9600 high frequency probes can support frequency measurements into the 4 GHz frequency range. The analog test circuit was measured using a Tektronix CSA 308 Signal Analyzer. The Tektronix CSA 308 has a time domain reflectometer (TDR) function capable of generating and measuring at least 40 GHz bandwidth as shown in Figure 21.

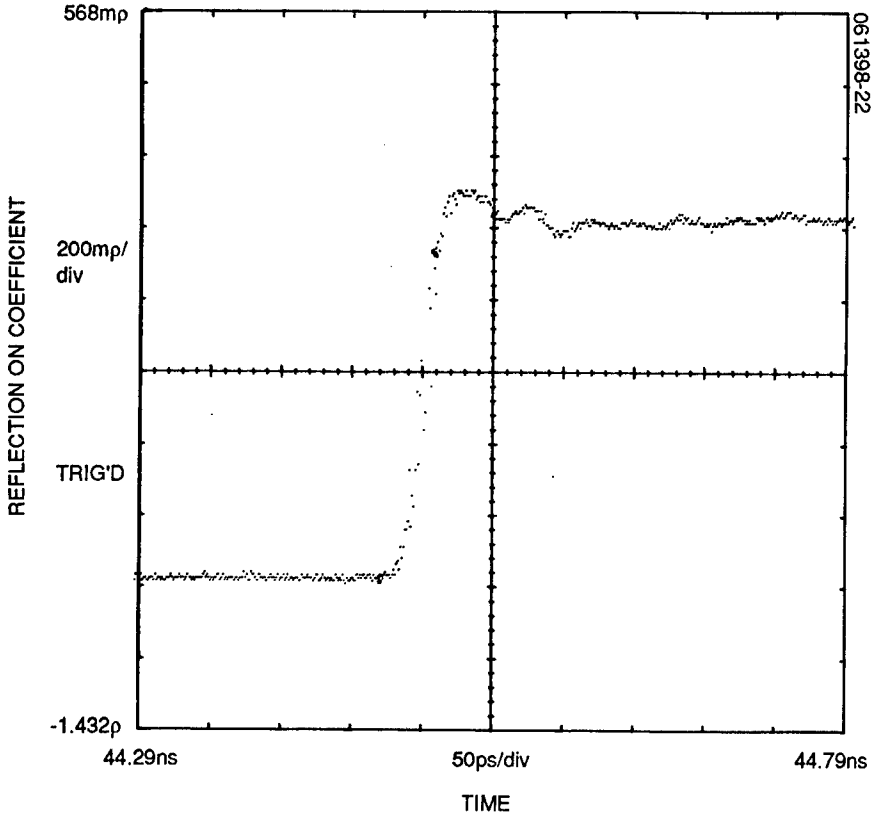

Figure 21. Rise time of TDR output pulse at 40 GHz.

When the CSA 308 is used in conjunction with the Tektronix High Frequency Probes P9600 and with high quality, air-dielectric coaxial cables, a TDR measuring system capable of at least 40 GHz is formed. This high bandwidth allows for very fine resolution of characteristic impedance discontinuities. The output signal in Figure 21 has a rise time of 25 ps or a frequency bandwidth of 40 GHz. The input signal has an amplitude of 250 mV. The structures fabricated

on the analog test substrate have closed mathematical solutions and can be fully analyzed. Comparison between theoretical and measured values is possible.

The analog test circuit features several unique features. The analog test circuit consists of 50 ohm transmission lines with one space and two space design rule separation. A single serpentine is present to generate a mutual inductance test cell, which allows the separation of the self-inductance component from the mutual inductance component. The multiple serpentine allows for accurate determination of crosstalk, skin resistance, dissipation factor, and coupling coefficients. Multiple pad rows are included for testing wire—bondability. The span of the wire-bond pairs follows a 1 to 5 ratio. By varying the span lengths of the wirebonds, the coupling coefficient of parallel wirebonds or ribbons can be determined. A box-like pattern represents a coaxial cable, and lines on both sides of the outside conductor of the coaxial cable determine signal leakage factor. Near the border of the substrate are resolution patterns to assist the operator in determining process parameters and process quality. A via chain resides in four places on the border and is functional at each process level.

A series of electrical test were performed to understand the electrical properties of the new multilayer dielectric material. These tests were performed using time domain measurement. This testing allows acquisition of performance data in a manner compatible with the usage of the PBCB material in a multilayer module.

Characteristic impedance (Z_0) is an important electrical parameter in determining the performance of high speed designs. Each transmission line has capacitance, and inductance that combine to form the characteristic impedance. The characteristic impedance of a transmission line is determined by conductor's geometry and the surrounding dielectric's properties. Capacitance is influenced by conductor distance from the ground plane, conductor width, and dielectric constant. Inductance is a function of conductor width, conductor thickness, and conductor separation from return current path. The transmission line has three basic configurations as compared to coaxial cable: microstrip, embedded microstrip, stripline. Microstrip is a conductor mounted on a dielectric material over a ground plane. Embedded microstrip is a conductor embedded in a dielectric material over a ground plane. Stripline is a conductor embedded in a dielectric material between two ground planes. The analog test circuit configuration with TDR probes is shown in Figure 22. This figure also depicts the inherent distributed capacitance of the transmission line. The test configuration with the TDR probes on the analog test circuit is illustrated in Figure 23. This figure also illustrates the reflected AC impedance.

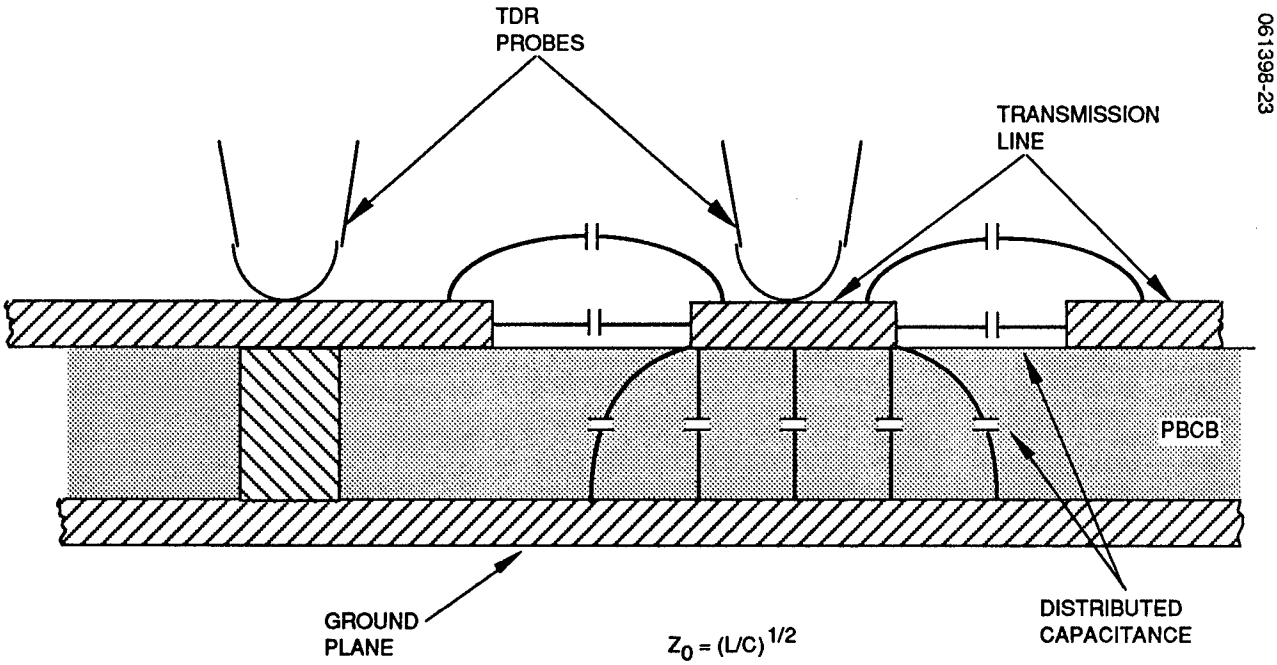

Figure 22. Analog test circuit configuration with TDR probes.

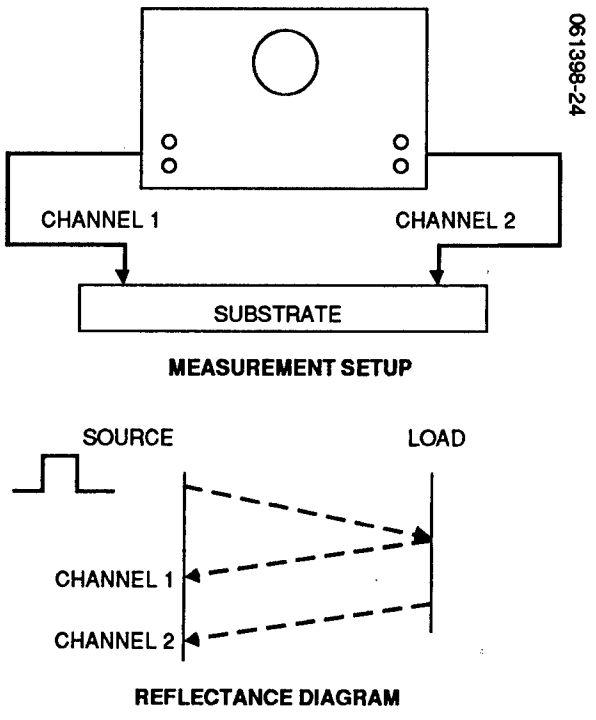

Figure 23. AC impedance/reflectance diagram.

The relationship between capacitance, inductance and impedance can be expressed as:

$$Z_0 = (L/C)^{1/2}$$

where

C = capacitance per unit length

L = inductance per unit length

Although the equation is simple, applying it to circuit design is very difficult. Capacitance has the greatest effect and is easily varied either by altering conductor width or by changing dielectric thickness or dielectric constant.

Velocity of propagation (Vp) is determined by the square root of the dielectric constant. The highest velocity of propagation (12 inch per nanosecond) occurs in a conductor completely surrounded by a vacuum. The velocity of propagation in a microstrip configuration must account for the air above the conductor and the dielectric material beneath.

A time domain reflectometer (TDR) is an instrument used to characterize impedance and discontinuities in a circuit. The TDR displays reflections from a circuit under test on an oscilloscope screen. The waveform conveys information about the structure of the circuit. Although a useful instrument, practically the TDR is limited to measuring the impedance of a uniform circuit and determining the location of simple discontinuities in the circuit. A complex, non-uniform transmission line will have a reflection waveform obscured by the superposition of multiple reflections.

The TDR consists of a sampling oscilloscope with a built-in step signal generator. The generator injects a very fast rise-time step into the circuit under test through an internal resistor of 50 ohms. This value is called the characteristic impedance of the TDR system. The waveform appearing at the junction of the resistor is monitored by the oscilloscope. Any discontinuities in the circuit are superimposed on the injected waveform.

The TDR screen is calibrated in units of reflection coefficient ρ (rho) on the vertical scale and in time in nanosecond on the horizontal scale. The reflection coefficient is defined so that $\rho = +1$ corresponds to an open circuit, and $\rho = -1$ corresponds to a short circuit. A circuit with matched impedance would have a $\rho = 0$. The impedance of a uniform circuit is given by:

$$Z = Z_O \frac{(1+\rho)}{(1-\rho)}$$

The horizontal distance scale denotes the circuit's propagation velocity by displaying the time from signal injection to distance along the circuit. The time on the TDR screen to any discontinuity is twice the propagation delay, since the injected step must make a round trip for a reflection to appear.

4.2.3.1 Test Results and Discussion. The three wafers were measured for ac impedance, dc resistance, resistivity, and propagation delay. These measurements describe the performance of a dielectric material in a multilayer module application. The analog test circuit contains several test circuits but only some of these circuits were measured. While the design contains five metal layers only the top two layers were accessible. The vias to the other layers were not connected and no measurements to those signal lines could be performed. Only the microstrip line test structure on the top layer could be accessed for high speed measurements.

The design values chosen for the analog test circuit were selected to meet the system requirements of high performance multichip module. The ideal multichip module would have a low resistance conductor exhibiting a constant, controlled characteristic impedance with a low propagation delay value. The use of copper metallization forms the low resistance conductor. The low dielectric constant of the PBCB allows the low propagation delay. The superior planarization qualities of the PBCB material allows for a constant, controlled impedance value after stacking five circuit layers.

For all analog test circuits using PBCB as the dielectric, the TDR display remained constant over the length of the transmission line. This indicates no variation in the capacitance along the line due to variations in dielectric thickness. This highlights the superior planarization properties of PBCB over irregular surface topographies. PBCB's superior planarization is in contrast to similar circuits using polyimide. In polyimide severe TDR discontinuities due to poor planarization qualities are typical.

To describe the capabilities of the analog test circuit, a comparison between the design values and the actual values was made. The design values for the analog test circuit, and the actual values for the analog test circuit are listed in Table 12. The values in Table 12 describe the qualities of the PBCB material as well as the copper via post interconnection.

The time domain reflectometer and ac impedance test results for wafers 1, 2, and 3 are illustrated in Figures 24, 25, and 26 respectively. The specific areas of interest in Figures 24, 25, and 26 are designated by the term "electrical length of transmission line."

TABLE 12. ANALOG CIRCUIT TEST RESULTS

	STATED VAULE	MEASURED VALUE		
		WAFER 1	WAFER 2	WAFER 3
LINE WIDTH	2.54×10^{-3} CM	3.08×10^{-3} CM	3.21×10^{-3} CM	3.47×10^{-3} CM
METAL THICKNESS	3×10^{-4}CM		N/A	NA
DIELECTRIC CONSTANT	2.7	2.66	2.66	2.66
DIELECTRIC THICKNESS	10×10^{-4}CM		NA	NA
DC RESISTANCE	66.8Ω	5.90Ω	7.02Ω	11.50Ω
RESISTANCE/CM	2.23Ω	1.9Ω/CM	2.3Ω /CM	3.8Ω /CM
AC IMPEDANCE (Z)	50Ω (Z_0)	49.9Ω	48.8Ω	50.2Ω
PROPAGATION DELAY		80 pSEC/CM	80 pSEC/CM	80 pSEC/CM

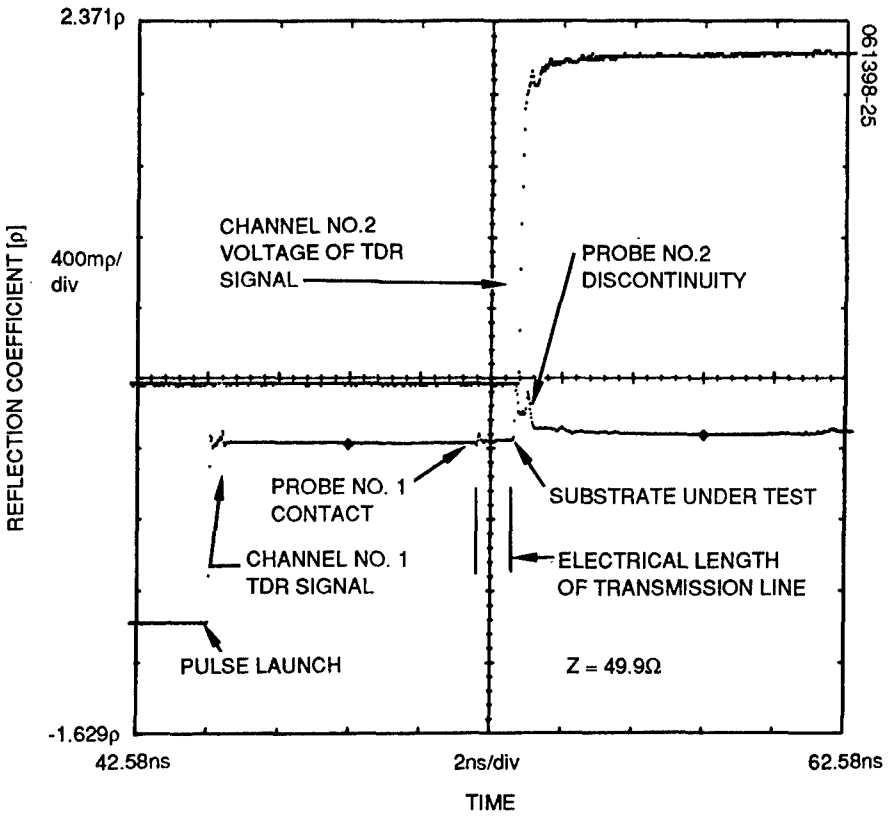

Figure 24. AC Impedance/Wafer 1 at 40 GHz.

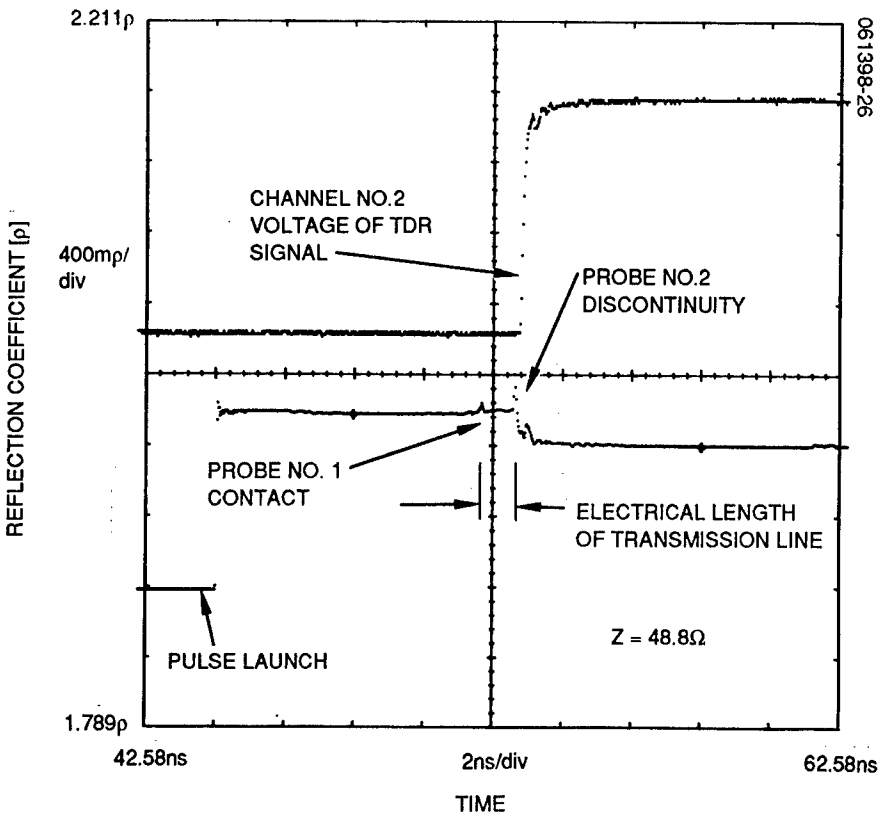

Figure 25. AC Impedance/Wafer 2 at 40 GHz.

In each case the measurement is free of variations in impedance. This confirms the claims of superior planarization and lack of voids in the PBCB dielectric.

Wafer No. 1

The time domain reflectometer (TDR) of Wafer 1 shows the transmission line impedance (Z) of the cables, connectors, and substrate under test. The impedance of the transmission line is 49.9Ω with minimum discontinuities due to superior planarization of PBCB.

Wafer 1 measurements indicated a close correlation between the desired values and the measured values. The dc resistance has a lower than predicted value.

Wafer No. 2

The time domain reflectometer (TDR) of Wafer 2 shows the transmission line impedance (Z) of the cables, connectors, and substrate under test. The impedance of the transmission line is 48.8Ω with minimum discontinuities due to superior planarization of PBCB. The dc resistance of the line agrees closely to the predicted value. While this wafer has a low characteristic

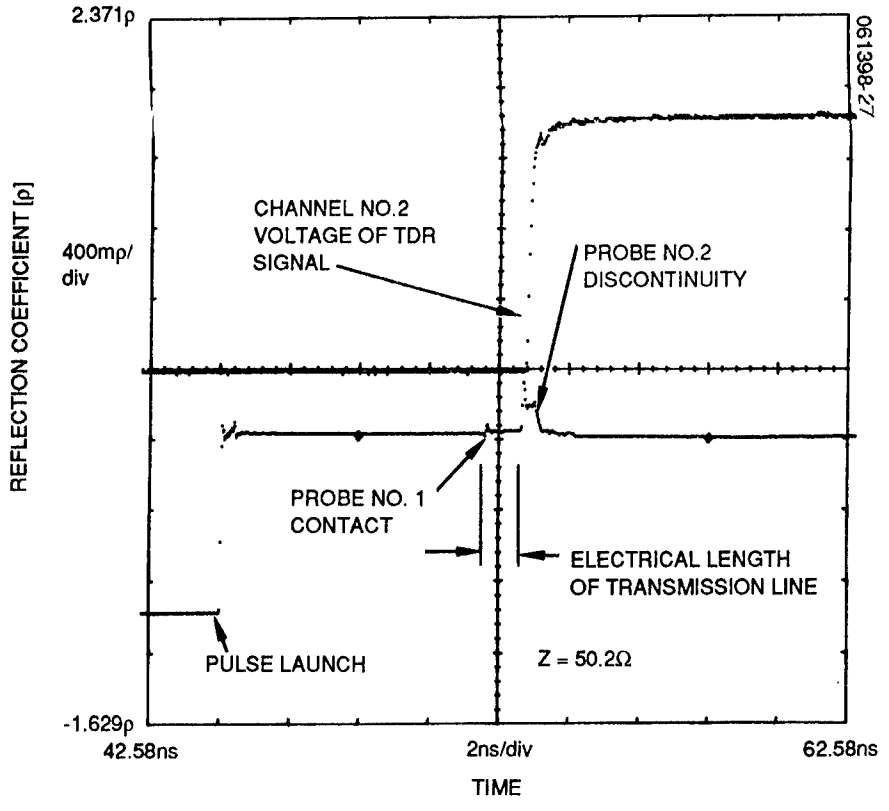

Figure 26. AC Impedance/Wafer 3 at 40 GHz.

impedance value, its TDR plot shows no discontinuities indicating excellent planarization of the PBCB material. The dielectric constant of the PBCB material allows for a low propagation delay.

Wafer No. 3

The time domain reflectometer (TDR) of Wafer 3 shows the transmission line impedance (Z) of the cables, connectors, and substrate under test. The impedance of the transmission line is 50.2Ω with minimum discontinuities due to superior planarization of PBCB.

Wafer 3 measurements indicate excellent agreement between the desired value and actual value of the characteristic impedance. This close agreement indicates accurate equations for calculating characteristic impedance in thin film fabrication processes. The close agreement also indicates excellent planarization of the PBCB material. The measured lines cross many lines without any detectable discontinuities being observed in the TDR waveform. A constant, characteristic impedance has importance since the characteristic impedance value has high sensitivity to separation distance between the conductor and ground plane. The dielectric constant of the PBCB material allows for a low propagation delay. The higher dc resistance indicates a thinner copper than desired.

4.2.3.2 Environmental Testing. Three analog test circuits were subjected to temperature cycling -55°C to +125°C for 15 cycles followed by temperature storage for 500 hours at 125°C according to MIL-STD-883, Method 1010.5B. No visual detrimental effect from these tests was observed. However, attempts to remeasure ac line impedance using the TDR probes were unsuccessful.

It was not possible to achieve electrical contact with the probes on the analog test circuit contact pads. This problem was due to surface contamination following 500 hour/125°C exposure. It was postulated that the severe long term (500 hour) exposure of the chrome surface metallization in an air environment at 125°C may have caused oxidation of the chrome with loss of electrical conductivity

4.2.3.3 Failure Analysis. Auger electron spectroscopy and ESCA were utilized to examine to analog circuit metallization for evidence of the cause of poor conductivity. The Auger spectrum is shown in Figure 27 revealing the presence of chromium oxide 15 angstroms into the surface metallization. Sputtering 400 angstroms into the surface (Figure 28) revealed a normal spectrum for chromium. The Auger sputter profile showed a high concentration of chromium oxide at the surface which was depleted to chromium metal at approximately 200 angstroms as shown in Figure 29. Electron Spectroscopy for Chemical Analysis (ESCA) at 15 angstroms into the surface shows the presence of 57 percent CrO and 43 percent Cr confirming the presence of the Cr(II) oxidation state (Figure 30). In addition the presence of carbon contamination 15 angstroms into the surface is confirmed by Auger in Figure 27. The unprotected analog circuit is not compatible with high temperature storage at 125°C.

4.2.3.4 Metallographic Cross-Sectioning. Metallographic cross-sectioning of the analog circuit clearly revealed the void-free nature of the PBCB dielectric shown in Figure 31. The transmission lines exhibit no discontinuities. This was confirmed by the ac impedance measurements. Metallographic cross-sectioning of the same circuit in the isolated via chain area, showed evidence of broken lines. It is not known whether this was caused by residual stress in the PBCB film or as a result of cross-sectioning procedure. The cross-sectioning procedure also caused delamination of the multilayer structure from the silicon substrate, possibly related to residual stress in the PBCB dielectric.

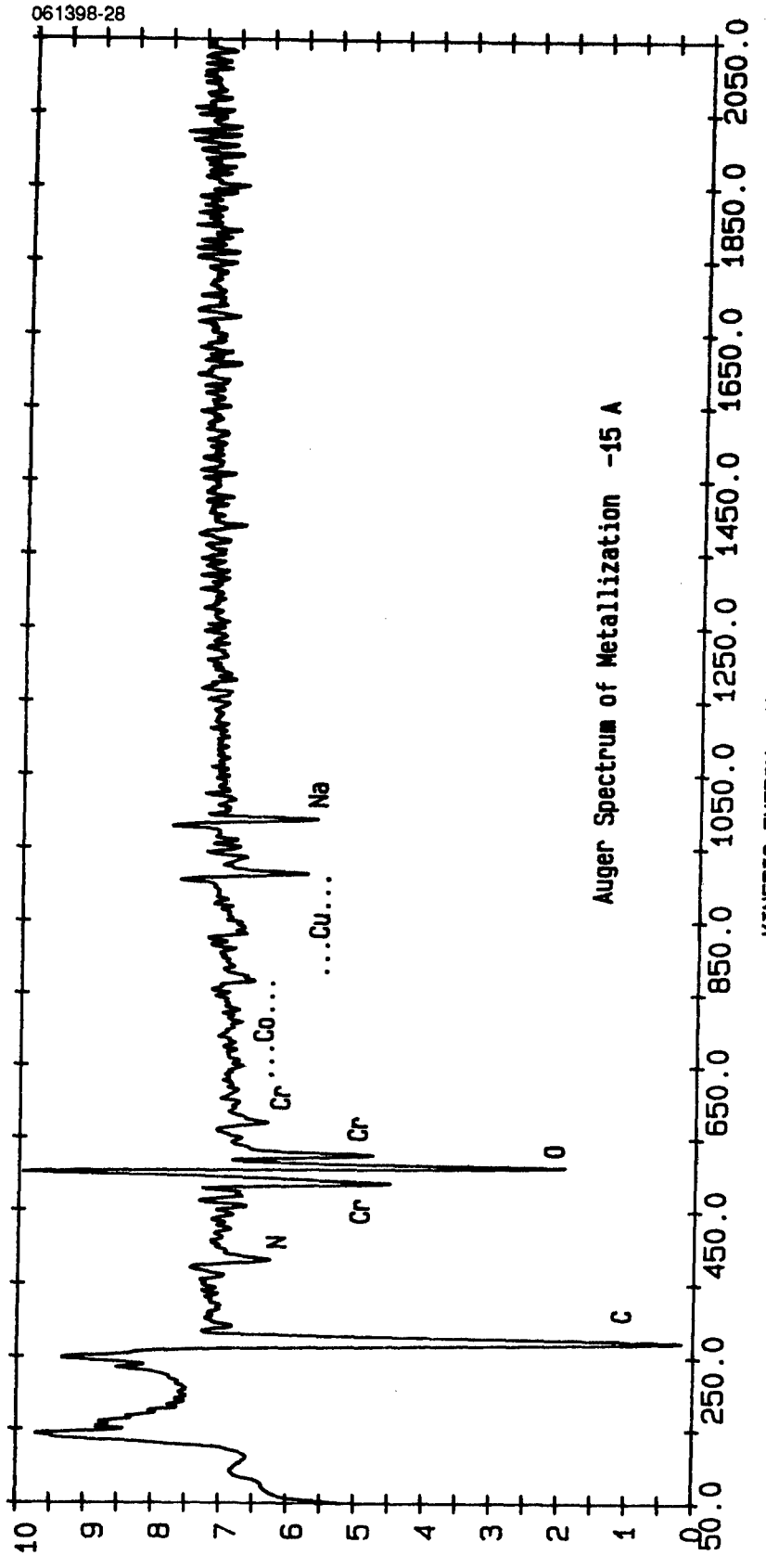

Figure 27. Auger electron spectrum of analog circuit (15A) 500 hours/125°C.

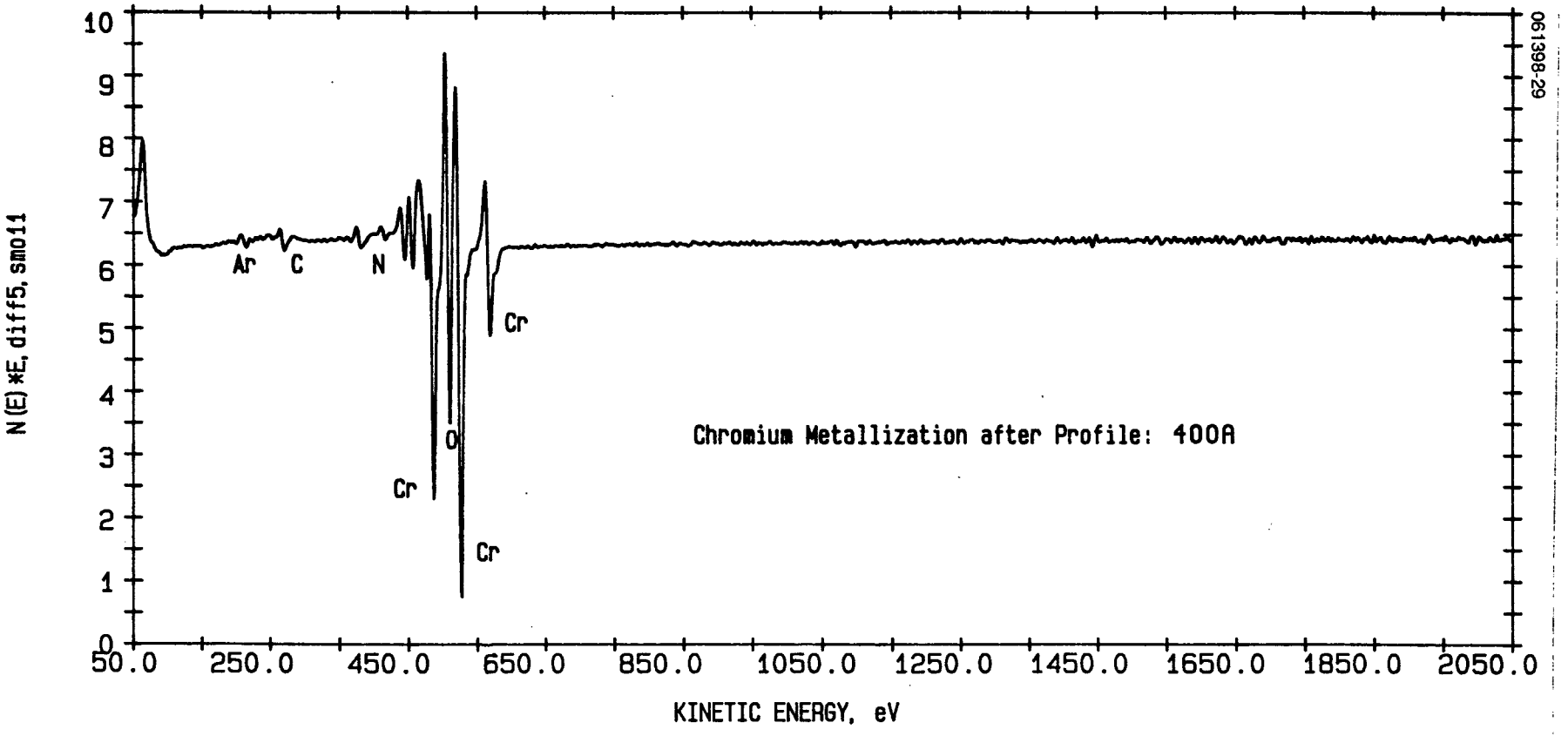

Figure 28. Auger electron spectrum of analog circuit (400A) 500 hours/125°C.

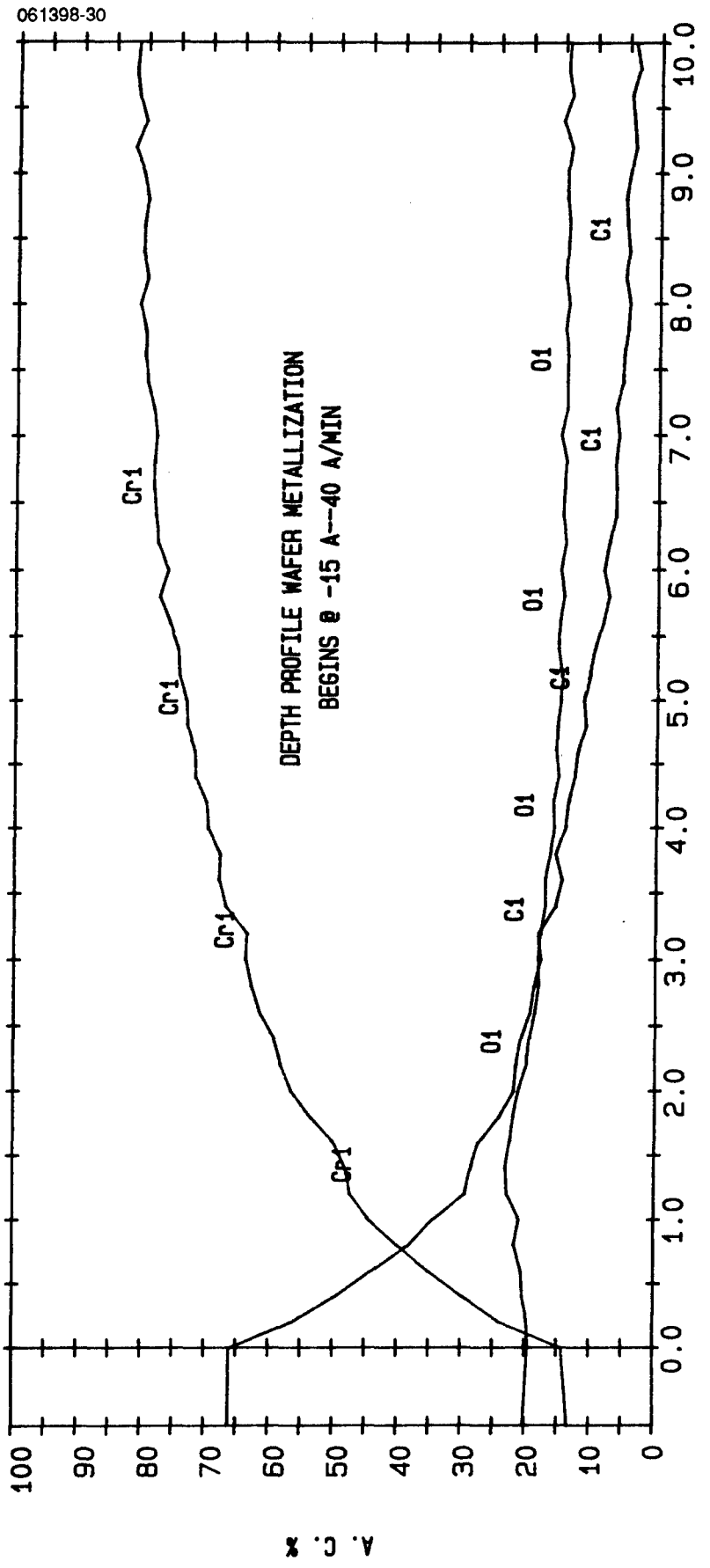

Figure 29. AES profile of analog circuit 500 hours/125°C.

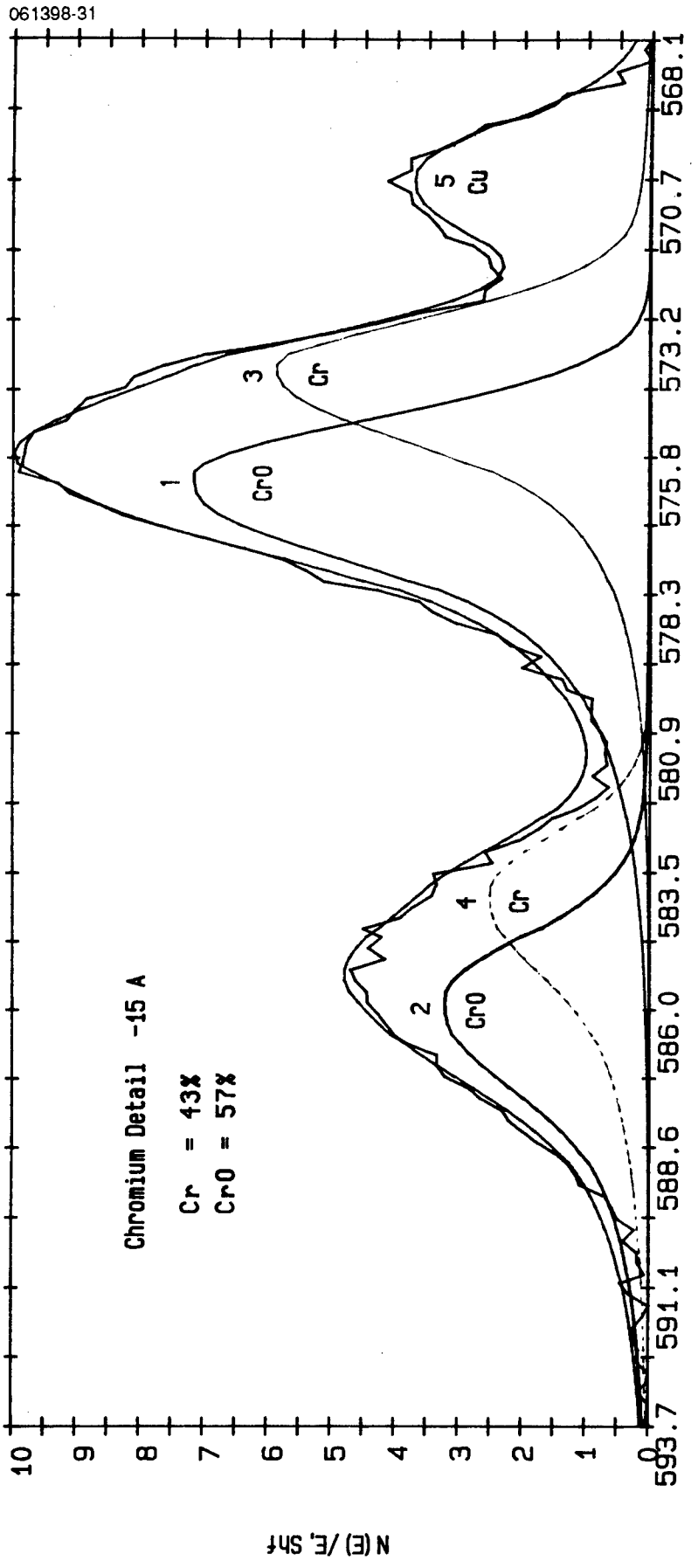

Figure 30. ESCA of analog circuit 500 hours/125°C.

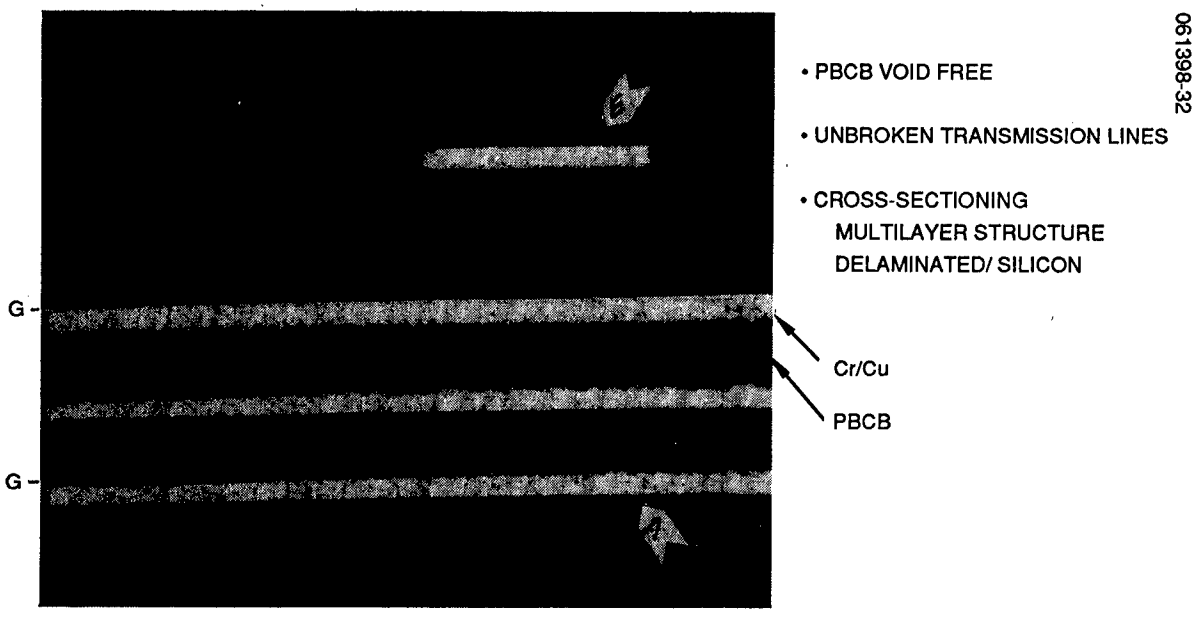

Figure 31. Analog circuit transmission line metallographic section 500 hour/125°C.

4.2.3.5 Test Conclusions Although via post level-to-level continuity was not entirely satisfactory due to unavoidable contamination associated with the electron beam metal deposition/via post process, these problems can be avoided with sputtered metal deposition. Residual stress and/or the metallographic cross-sectioning procedure may have resulted in broken lines in the via chains and delamination of the multi-level structure from the silicon substrate during cross-sectioning.

The test results, however, clearly indicate the superior electrical performance and planarization properties and void-free behavior of PBCB. This was confirmed with measured ac impedance values being nearly identical to the nominal characteristic impedance of the transmission line.

4.3 ASSESSMENT OF MERITS OF PBCB

A comparison of the physical, electrical and processing properties of various polyimides and PBCB is presented within this section followed by an assessment of the relative merits of PBCB polymer dielectric films.

4.3.1 Comparison of PBCB Polyimides and Other Polymer Dielectrics

Coefficient of thermal expansion, dielectric constant and moisture absorption of PBCB and other selected multilevel dielectrics are summarized in Table 13. The table includes commonly employed substrate materials of alumina and silicon as well as typical conductor materials of copper and aluminum for CTE mismatch comparison. Ideally the coefficient of thermal expansion of the dielectric material should closely match that of the substrate to avoid problems such as delamination and warp. The values in parentheses were measured at Hughes. Hughes dielectric constant values were measured at 1 MHz. Hughes moisture absorption was measured after 85C/85 percent relative humidity for 5 days.

TABLE 13. SELECTED PROPERTIES OF PBCB AND OTHER ELECTRONIC MATERIALS

MATERIAL	COEFF OF THERMAL EXPANSION (PPM/°C)	MOISTURE ABSORPTION (PERCENT)	DIELECTRIC CONSTANT
ALUMINA SUBSTRATE	6.5	–	10.0
SILICON SUBSTRATE	2.7	–	11.7
HITACHI L110 POLYIMIDE	5.0	2.0	3.3
DUPONT 2555 POLYIMIDE	40.0	2.5	3.6
POLYBENZOCYCLOBUTENE (PBCB)	64.0	(0.023)	2.66 (3.0)
POLYPHENYLENEQUINOXALINE (PPQ)	60.0	(<0.05)	(2.77)
PARYLENE (POLYXYLENE)	35.0	(<0.05)	(2.76)
THERMID	25.0	<1.0	2.9
COPPER	16.0	–	–
ALUMINUM	25.0	–	–

An extensive comparison of nine different polyimides with PBCB is presented in Table 3. The data was prepared at the Hughes Microelectronics Circuits Division which uses Dupont 2611D (7). PBCB has a lower dielectric constant and lower water absorption than any polyimide, but the CTE is higher. Warp data is for a 25 micrometer thick film.

Recently a more comprehensive summary of physical, electrical and processing properties of PBCB and three different polyimides, which is presented in Tables 14, 15and 16 respectively, was published in *Hybrid Circuit Technology* (10). The physical, electrical and processing properties of two different PBCB dielectrics, identified as BCB XU13005 and BCB XU130028 are shown in these three tables. The work conducted under this contract utilized the PBCB material identified as BCB XU13005. PBCB (BCB XU13005) exhibits the lowest dielectric constant, lowest water absorption and highest degree of planarization than any polyimide, but the

TABLE 14. PHYSICAL PROPERTIES OF THIN FILM POLYMER DIELECTRICS

MATERIAL	Tg C	CTE ppm/C	KPSI FLEXURAL MODULUS	MOISTURE UPTAKE
PI 2555	>320	40	349	1-2%
PI 2611D	>400	3	1203	0.50%
PIQ 13	>400	54	–	0.80%
BCB XU13005	>350	65	480	0.23%
BCB XU130028	>370	27	747	0.87%

TABLE 15. ELECTRICAL PROPERTIES OF THIN FILM POLYMER DIELECTRICS

MATERIAL	DIELECTRIC CONSTANT*	DISSIPATION FACTOR*	BREAKDOWN V/CM	VOL RES OHM-CM
PI 2555	3.5	0.0020	4×10^6	$>10^{16}$
PI 2611D	2.9	0.0020	$>2 \times 10^6$	>10
PIQ 13	3.4	0.0020	3×10^6	$>10^{17}$
BCB XU13005	2.7	0.0008	4×10^6	$>10^{18}$
BCB XU130028	2.7	0.0004	4×10^6	$>10^{19}$

*AT 1 MHz

TABLE 16. PROCESSING PROPERTIES OF THIN FILM POLYMER DIELECTRICS

MATERIAL	SOLIDS CONTENT (%)	VISCOSITY (POISE)	CARRIER SOLVENT	DEGREE OF PLANAR	FILTRATION (MICRONS)	CURE TEMP (C)
PI 2555	20.0	12-16	NMP	<50%	0.2	350
PI 2611D	13.5	110-135	NMP	<50%	1	350
PIQ 13	14.5	11	NMP	<60%	–	350
BCB XU13005	55.0	1	XYL/MES*	>90%	0.2	250
BCB XU130028	55.0	1	XYL/MES*	>70%	0.2	250

*XYLENE OR MESITYLENE

CTE is higher which is counteracted by its flexural modulus. The lower cure temperature of PBCB (250°C) results in a lower thermal stress at 20°C for the film than a polymer film cured at 350-450°C. The inherent tensile stress resulting from the densification of the polymer is usually much less than the thermal stress and can generally be ignored.

A comparison of the wave propagation velocity of PBCB with other materials is illustrated in Figure32. This data was compiled by J.J. Rech (11). Because of the low dielectric constant of PBCB, it has an advantage for transmission line applications. Signal delays are less and capacitance is less.

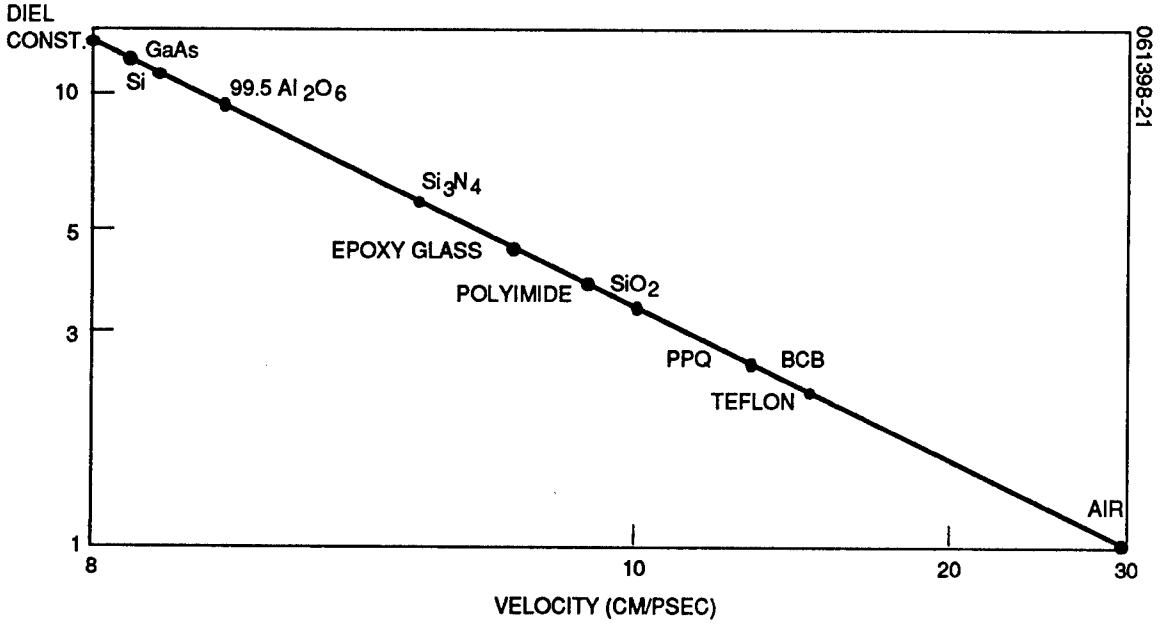

Figure 32. Wave propagation velocity in PBCB and other materials

4.3.2 Relative Merits of PBCB

Based on results of the contract, it can be concluded that:

- PBCB is better than polyimide from the standpoints of moisture absorption, dielectric constant, and planarization.
- PBCB is satisfactory with regards to chemical stability, outgassing, and 180° shear.
- PBCB exhibits more warp and stress than most polyimides. These properties are a function of the thermal coefficient of expansion and flex modulus. A minimum of warp is desired, because excessive warp presents wafer processing problems, such as spinning and vacuum pickup.
- PBCB can be spun on and metallized just like polyimides.

- Adhesion is satisfactory.
- PBCB is oxygen-sensitive and requires a careful cure in a nitrogen atmosphere
- PBCB is compatible with fabrication processes used for multilayer thin film circuits. It survives all of the normal multilevel wafer processing steps.
- PBCB exhibits void free behavior, unlike some polyimides, in 10 micrometer thick layers which are desirable for high speed circuits.
- PBCB films require no adhesion promoters for multilevel circuit fabrication unlike all polyimides.

4.4 DISCUSSION OF PROBLEMS

Electrical measurements revealed cases of high interconnect resistance in via chain serpentine patterns. In certain cases opens occurred. This is attributable to several causes: redeposition of polymer ash during plasma etch, oxidation and inability to clean the post in situ before electron e-beam deposition. The redeposition of polymer ash is intrinsic to the plasma etching process. Oxidation in air of exposed metal on top of the post is unavoidable during wafer transfer from the etching system to the electron beam evaporator. Surface contamination, whether it is from plasma ash or oxidation is unremovable using the electron beam evaporator. For the recommended solution of this particular problem, see discussion in Section 4.5.

Instances of local delamination was also experienced. This is not owing to the lack of adhesion of the PBCB from layer to layer or to the substrate. It appears that compressive spring loaded clips used to hold substrates onto the planetary during metallization in the electron beam evaporator induced local delaminations. This practice was adopted from previous work conducted on polyimide, which exhibits less stress than PBCB. A recommended solution to this problem, is presented in Section 4.5.

4.5 SPECIFIC RECOMMENDATIONS

The appearance of high interconnect resistance needs attention. The technological frame work for the most reliable interconnect has been established using the via post interconnect method. It appears that the sole cause of high interconnect resistance arises from surface contaminants on the post top. This contaminant comes from polymer ashing and redeposition in the plasma etching chamber and possible surface oxidation in air before the next level of metallization is completed. At present the electron beam evaporator cannot be used to clean the post top in situ immediately before the next layer of metallization. However the post top can be back-sputter cleaned inside a sputtering chamber to make the post top atomically clean before depositing the next layer of metallization without breaking vacuum.

Using sputtering also eliminates the need to mount the wafers onto the planetary in the electron beam chamber using spring loaded clips which induce delamination. Wafers can be placed onto the platen without stress during back sputtering and throughout the metallization run.

The advent of the PBCB material for the first time made it possible to interconnect from one metal layer to another metal layer through relatively thick layers reliably. The low dielectric constant of the PBCB allows the designer the intrinsic speed gain from capacitance lowering in the electronic module fabricated. In addition the planarizing property of the PBCB permits thick dielectric layers which drive down the coupling capacitance and enhances speed of the circuit. The via post which is ideally suited to reliably interconnect between layers is planarizable to within a small fraction of a micron by PBCB. It appears that the surface contaminant which prevents the ultimate in low resistance interconnect can be removed using back sputtering in a sputtering chamber.

It is recognized that via hole filling for interconnection is limited to only relatively thin dielectric layers with its concomitant high capacitance and low speed. Thick dielectric layers such as those coated using Hitachi L110 and other polyimides must be polished flat if via post are used. The use of PBCB and via post interconnect promises the most compatible and reliable material and interconnect method combination.

4.5.1 Recommended Follow-on Program

We propose that a program be undertaken to use sputtering for interconnect metallization deposition. This not only provides for atomically clean interconnection from layer to layer in the electronic modules, but the sputtering action gives a more reliable and lower resistance interconnect particularly in non line of sight situations. The PBCB is currently cured at 250°C, a temperature close to that which a specimen can reach during sputtering. It is not clear at this point whether the PBCB would outgas during sputtering and suffer heat related damage. Further work is needed to realize the full benefit of the PBCB/via post interconnect methodology. Sputtering of the metallization can optimize the material and processes involved in the via post interconnection technology utilizing planarizing PBCB.

In any electronic circuit, the designer desires the minimization of propagation delay of signals. Propagation delays are determined by RC (resistance x capacitance) constants. At this point the capacitance of the electronic circuit has been minimized through the low dielectric constant and the low moisture absorption of PBCB and the ability to interconnect across thick layers. The resistance can be lowered by reduction of the contact resistance. This can only be done by sputter deposition. Therefore a program supporting the optimization of the propagation delay

through resistance lowering would allow the realization of the full potential of the PBCB/via post interconnection methodology in the fabrication of high density multilayer electronic modules.

4.6 CONCLUSIONS

Polybenzocyclobutene dielectric films have exhibited significant advantages compared to polyimides for multichip multilayer packaging applications. Although PBCB films must be cured in an oxygen-free environment and are somewhat more sensitive to warpage/stress than polyimides, they are significantly superior with respect to moisture resistance, lower dielectric constant, and leveling or planarization over rough surface topography. The adhesion of PBCB films to copper, aluminum and silicon without adhesion promoters is excellent. Tests to date with PBCB as a multilevel dielectric with both a counter/decoder circuit and an analog circuit, in conjunction with via post interconnects, reveal the potential for the reliable fabrication of high speed and high density multichip/multilayer modules.

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U.S. Government Printing Office 548-076