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SiC Migration Enhanced Embedded Epitaxial (*ME*^{3}) Growth Technology

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Abstract. In this work, we have developed an innovative epitaxial growth process named the "Migration Enhanced Embedded Epitaxial" (*ME*^{3}) growth process. It was found that at elevated growth temperatures, the epitaxial growth at the bottom of the trenches is greatly enhanced compared to growth on the sidewalls. This is attributed to the large surface diffusion length of reactant species mainly due to the higher growth temperature. In addition, it was found that this high temperature *ME*^{3} growth process is not influenced by the crystal-orientation. Similar growth behavior was observed for stripe-trench structures aligned either along the [11-20] or [1-100] directions. No difference was observed in the electrical performance of the pn diodes fabricated on either oriented stripe geometry. The *ME*^{3} process can also be used as an alternative to ion-implantation technology for selective doping process.

1. Introduction

Silicon carbide (SiC) epitaxial growth has been a key device process technology and contributed greatly to the development of SiC power devices despite relatively poor quality of the 4H-SiC substrates. In recent years, the SiC embedded epitaxy process was successfully employed for fabricating SiC switching devices [1-3]. Onda et al. [1] presented a new transistor called the epi-channel field effect transistor (ECFET). In this transistor, a thin n-type channel epitaxial layer was grown on the trench sidewall to improve the metal-oxide-semiconductor (MOS) interface characteristics. Malhan et al. [3] presented the all epitaxial grown junction field effect transistor (JFET), a structure basically similar to ECFET except the MOS interface. The n-type channel and p-type gate layer were grown in the trench to fabricate this all epitaxial JFET structure. Chen et al. [4] found that the growth near the trenches perpendicular to the [11-20] off-direction tends to be highly asymmetric due to the influence of the step-flow growth .

This innovative *ME*^{3} process was developed to realize an all epitaxial normally-off 4H-SiC JFET as shown in Fig. 1. JFET design requires the embedded process of n-type channel and p-type top gate process for planarization. We successfully embedded the deep trenches (aspect ratio 2-4) without voids by the combination of high migration of chemical species on the growing surface and H_2 etching process at relatively high growth temperatures. In this work, we have fabricated all epitaxial normally-off JFET using *ME*^{3} process and carried out the structural and the electrical evaluation of embedded pn junction diode.

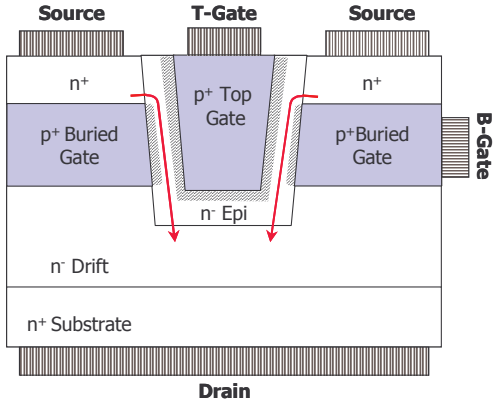

Fig. 1: A schematic cross-section view of double gate normally-off trench SiC-JFET.

2. Experiment

N-type 4H-SiC (0001) off-axis substrates (8-degrees off towards the [11-20] direction) were used in the present investigations. Stripe pattern deep trenches of aspect

ratio about 2 (depth=3.0μm; width=1.5μm) were formed by the ICP dry etching process. The stripe-trench structures were aligned either along the [11-20] or [1-100] directions. A vertical hot-wall CVD reactor was used with typical growth conditions: SiH_4 (3.0 - 7.5sccm) - C_3H_8 (0.8 - 3.0sccm) - H_2 (10.0 - 20.0 slm) and temperature 1500 - 1650 degrees Celsius. Non-doped n-type epitaxial layers were grown under various conditions. The growth temperature, the growth pressure, and C/Si ratio were varied over 1500-1650 degrees Celsius, 200-600 Torr, and 0.8 - 2.0, respectively. The growth behavior inside the narrow trenches and crystal quality of the embedded epitaxial layer were investigated using HRTEM (high resolution transmission electron microscopy). For the characterization of embedded pn junction diodes, all epitaxial JFETs (Fig.1) were fabricated by embedded epitaxial growth on 4H-SiC (0001) $n^+/p^+/n^-/n^+$ off-axis substrates. Striped trenches either along the [11-20] or [1-100] directions with 4.0 μm deep and 3.0 μm width were etched by ICP dry etching. The n-type epitaxial layer (<0.5 μm-thick; N_d: >1 x 10^{16} cm^{-3}) and Al-doped (N_a: >1 x 10^{19} cm^{-3}) p^+ layer were grown on the trenched wafers. The typical active area of the normally-off 4H-SiC JFET pn diode (top p^+gate/ n-channel/ n^+source) is about $5x10^{-4}$ cm^2.

3. Results and Discussion

Fig. 2 shows the cross-sectional SEM images of an n-type trenched substrate aligned along the [11-20] direction grown with a non-doped n-type epitaxial layer at fixed growth condition for 90min., (SiH_4 flow rate=3.0sccm, H_2 flow rate:10slm, C/Si ratio=0.8) except the growth temperature. As the n-type substrates were used, the usual bright and dark regions which corresponds to the p-type epitaxial layer and the n-type substrate, respectively is not observed. Instead, the dotted line indicates the position of trenches before the embedded growth.

For a conventional low temperature epitaxial growth run (1500 degrees Celsius), the growth outside the trench is prominent (Fig. 2a). After 90min. of growth, a high index facet plane (not identified) grows with a large overhanged shape. The ratio of the epitaxial layer thickness on the bottom of the trench to that on the top surface (b/a) is about 0.2 and the one on the sidewall is smaller than the bottom. On the other hand, at the higher temperature of 1600 degrees Celsius (Fig. 2b), the growth outside the trench decreases whereas the b/a ratio increases. At 1650 degrees Celsius temperature (Fig. 2c), epitaxial growth at the bottom of the trenches was enhanced, which may bring a larger surface diffusion length of reactant species compared to lower temperature. In addition, at high growth temperature, the H_2 etching effect dominates outside the trench area, therefore, effectively reducing the growth outside the trench areas. The b/a ratio increases from about 0.2 at growth temperature of 1500 degree Celsius to about 2.7 at 1650 degrees Celsius, respectively.

Generally, the growth profile depends on a balance of the crystal surface energy, gas phase reactant diffusion and surface reactant diffusion. At lower growth temperatures, the growth habit is probably limited by diffusion of reactants to the growing plane and the surface energy is determined by the growing crystal plane, which results in faced formation with overhanged shape. In higher

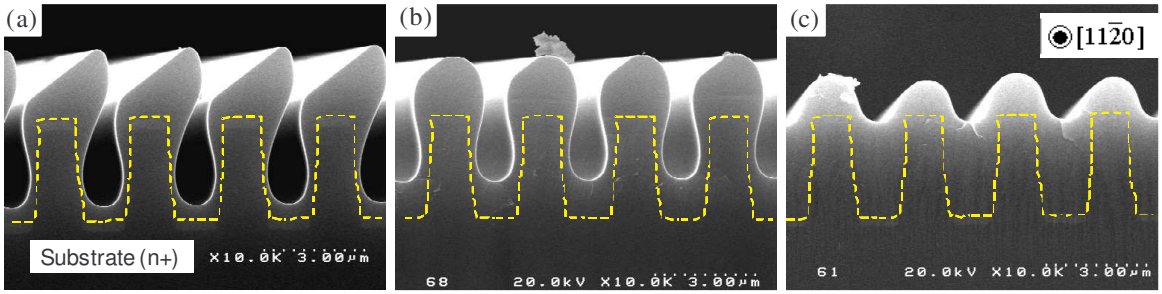

Fig. 2 : Cross sectional SEM images of n-type embedded trenched substrate along the [11-20] direction after 90min growth at various growth temperatures; (a) <1500℃, (b) ~1600℃, and (c) >1600℃

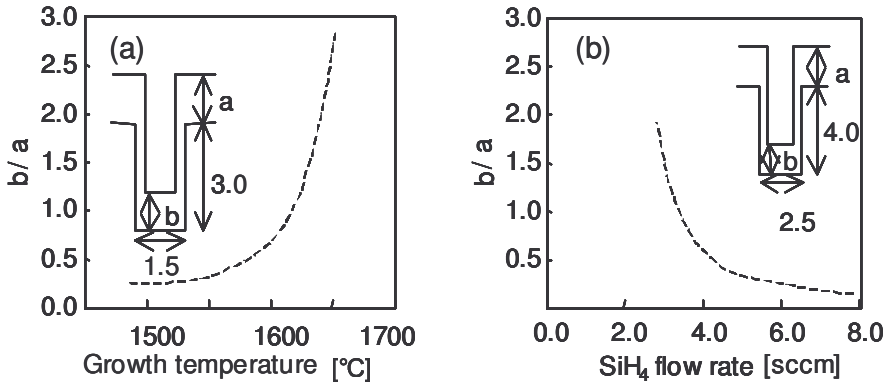

Fig. 3 : Dependence of (a) the growth temperature and (b) the SiH_4 flow rate on the ratio of the epitaxial layer thickness at the bottom and the top surface of trenches.

temperature of more than 1600 degrees Celsius, active surface migration to minimize surface free energy and subsequently the surface area is decreased. This phenomenon rounded the top of the trench corner shape. The outcome of this phenomenon is very much similar to the result of high temperature H_2 etching effect on the trench corners. Finally, at elevated temperatures the overhanged facet shape growth is suppressed and trenches are successfully embedded without voids. The H_2 etching effect actually affects the growth rate outside the trench areas. The growth at the bottom of the trenches is greatly enhanced compared to growth on the surface top under the condition of higher growth temperature. In addition, it is known that the lower C/Si ratio promotes migration of surface reactants due to increased migration length [5]. Fig. 3a shows the dependence of the growth temperature on the ratio of the epitaxial layer thickness at the bottom and the top surface of trenches (b/a). Fig. 3b shows the b/a dependence of SiH_4 flow rate at growth temperature of 1650 degrees Celsius growth. The increase in the SiH_4 flow rate straightforward increases the growth rate outside the trenches, thus the b/a ratio decreases. Also, in this case the growth profile had an overhanged shape, however, not the facet plane growth. In higher SiH_4 flow rate conditions, the amount of migration species from the top surface into the trench seems to depend on both the C/Si ratio and the growth temperature. When the SiH_4 flow rate increases, the growth inside the trench is suppressed relative to outside and forms the overhanged shape. In addition, the balance between the deposition and the H_2 etching outside the trenches also changes in such condition. Accordingly, to achieve the voidless embedded epitaxial growth, it is important that the supply of growth species should not exceed the amount of migration, including the H_2 etching effect. It was also found that this high temp erature *ME*^{3} growth process is not influenced by the crystal-orientation. Similar growth behavior was observed for stripe-trench structures aligned either along the [11-20] or [1-100] directions, which is

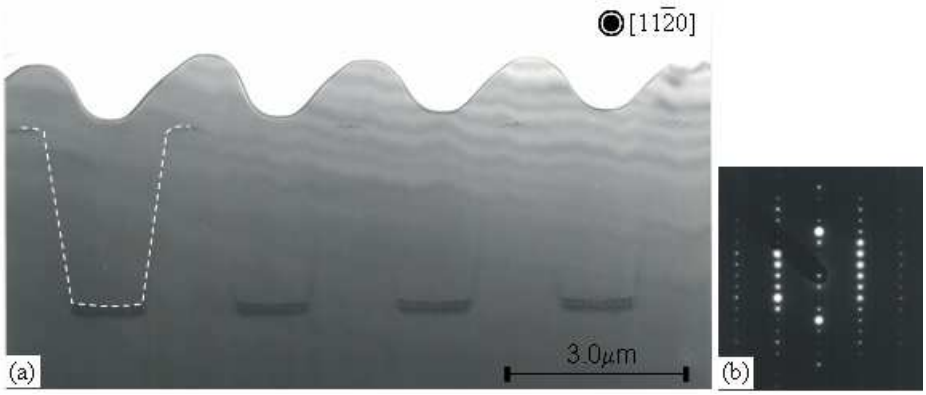

Fig.4: (a) Cross-sectional high-resolution transmission electron microscope image and (b) Electron diffraction pattern confirm the defect free homo-epitaxial growth inside the trench substrate aligned along the [11-20] direction.

not the case in the standard low temperature CVD process as reported by Chen et al. [4]. The cross-sectional HRTEM image and the electron diffraction pattern of the embedded are shown in Fig. 4. The HRTEM image confirms the defect free homo-epitaxial growth inside the trench substrate aligned in the [11-20] direction. The electron diffraction pattern confirms the 4H-SiC growth. Poly-type inclusion was not observed in the *ME*^{3} process.

Electrical properties of pn junctions formed by embedded epitaxial growth during the normally-off 4H-SiC JFET fabrication have been characterized. Fig. 5 shows the pn-diode characteristics of such diodes (top p^+gate/ n-channel/ n^+source) along the [11-20] or [1-100] directions. No difference in the electrical performance of the diodes fabricated along the [11-20] or [1-100] directions were observed. Diodes exhibit good I-V characteristics with an ideality factor of 2.0, which is dominated by recombination. No excess leakage was observed for diodes with trenches parallel to [1-100], which is usually attributed to the poor quality of the epitaxial layers. The high pn diode blocking voltage in both diodes is attributed to the similar doping level of the n-type channel epi-layer under the low C/Si ratio. The reverse leakage current was below $1x10^{-7}Acm^{-2}$ in the measured voltage range. These results endorse the high quality of the embedded SiC layers by *ME*^{3} process.

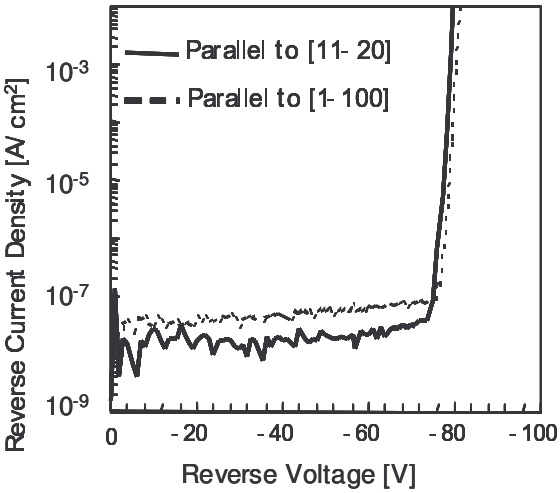

Fig. 5: Reverse characteristics of the pn-diode of the all epitaxial normally- off JFET along the [11-20] and [1-100] trench direction.

4. Conclusion

We developed an innovative epitaxial growth process named "Migration Enhanced Embedded Epitaxial" for all epitaxial normally-off SiC-JFET. Deep and narrow trench structures are successfully embedded using the *ME3* process without any voids in trenches. It was found that at elevated growth temperatures, the epitaxial growth at the bottom of trenches is greatly enhanced compared to growth on the sidewalls under the condition of higher growth temperature of 1650 degrees Celsius and lower C/Si ratio. This process is crystal-orientation independent so it widened the device and process design dimensions. No difference in the electrical performance of the pn diodes fabricated along the [11-20] or [1-100] directions was observed. The *ME*^{3} process can be used as an alternative to ion-implantation technology for selective doping process and it also greatly contributes to the future SiC RESURF technology.

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