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Electrical properties of MOS structures on 4H-SiC (11$\bar{2}$0) face

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Abstract. Threshold voltage (V_{TH}) instability, channel mobility and oxide reliability have been investigated for meta-oxide-semiconductor (MOS) structures on 4H-SiC (11$\bar{2}$0) face using various gate oxidation procedures. Channel mobility of n-channel MOSFET with a gate oxide by pyrogenic oxidation is higher than that by dilute-DRY oxidation followed by a nitrous oxide (N_2O) post-oxidation annealing (POA). On the other hand, oxide reliability for the pyrogenic oxides is poor compared with the dilute-DRY/N_2O oxides. A Hydrogen POA is effective in an improvement of channel mobility for both oxides, but causes a harmful effect on V_{TH} stability. Temperature dependence of V_{TH} instability indicates that MOS structure grown by dilute-DRY followed by N_2O POA is suitable for a practical use of SiC MOS power devices.

Introduction

SiC MOSFETs with low on-resistance and high blocking-voltage have been expected as a key device for next-generation power electronics technology. Especially, trench-gate MOSFETs are one of the promising candidates for power switching devices since drastic decreasing in the on-resistance is possible due to the high cell density and the lack of JFET region [1-3]. In addition, a (11$\bar{2}$0) face, in which high channel mobility was achieved at MOS interface, is available for a trench sidewall of these MOSFETs on widely used 4H-SiC (0001) and (000$\bar{1}$) wafers, resulting in further decrease of the on-resistance. A lot of researches as to MOS structures on the (11$\bar{2}$0) face have been reported [4-8], but oxide reliability and threshold voltage (V_{TH}) instability have been scarcely reported up to now. In this study, we have comprehensively investigated electrical properties of MOS structures formed on 4H-SiC (11$\bar{2}$0) face for a practical use in the trench-gate MOSFETs.

Experimental

N-type and p-type 4H-SiC (11$\bar{2}$0) epitaxial wafers were used for fabrication of n-type MOS capacitors and planar n-channel MOSFETs. Effective carrier density and thickness of the epitaxial layer grown by our group were 1E16 cm^{-3} and 10 μm in both wafers, respectively. Source and drain regions of n-channel MOSFETs were formed by a phosphorus ion implantation at 600ºC to a total dose of 7E15 cm^{-2}, then a post-implantation annealing was conducted at 1600ºC in Ar atmosphere. Gate oxides were thermally grown by four kinds of procedures as shown in Table 1. Pyrogenic and N_2-dilute-DRY(2%-O_2) oxidations were performed at 1100ºC and 1350ºC, respectively. And, N_2O and H_2 post-oxidation annealing (POA) treatments were conducted at 1250ºC and 1000ºC,

Table 1. Equivalent oxide thickness (E_{OT}), peak μ_{FE} of the planar n-channel Al-gate MOSFETs and Q_{BD} of the n-type MOS capacitors measured at 25ºC.

Sample	Gate oxidation condition	E_{OT} [nm]	μ_{FE} [cm^2/Vs]	Q_{BD} [C/cm^2]
(a)	Pyrogenic ox.	47.4	88.6	1.4
(b)	Pyrogenic ox. / H_2 POA	47.7	137.6	3.1
(c)	Dilute-DRY ox. / N_2O POA	40.7	57.2	15.9
(d)	Dilute-DRY ox. / N_2O POA / H_2 POA	40.2	119.6	14.0

respectively. After gate oxidation, aluminum or Poly-Si films were deposited on the samples as a gate electrode. Finally, aluminum was evaporated for source, drain and body electrodes for all the samples. In each measurement, MOSFET performances and oxide reliability were examined from a few MOSFETs and 150 MOS capacitors, respectively.

Results and discussion

Figure 1 shows typical drain current (I_D) - gate voltage (V_G) characteristics of four Al-gate MOSFETs at drain voltage of 0.1 V and 25ºC. All the samples show a normally-off operation and threshold voltage (V_{TH}) at I_D of 100 nA are 2.1, 2.9, 1.7, and 1.0 V in the samples (a), (b), (c) and (d), respectively. The peak field-effect channel mobility (μ_{FE}) is shown in Table 1. The H_2 POA is effective in an improvement of peak μ_{FE} in both the pyrogenic and dilute-DRY/N_2O oxides, resulting in high μ_{FE} of more than 100 cm^2/Vs in the samples (b) and (d). This is due to decrease in interface state density by hydrogen termination of dangling bonds at the oxide/SiC interface during the H_2 POA. The charge-to-breakdown (Q_{BD}) values of MOS capacitors measured from a constant-current stress (7mA/cm^2) time-dependent dielectric breakdown measurement at 25ºC are indicated in Table 1. The dilute-DRY/N_2O oxides indicate higher Q_{BD} value compared with the pyrogenic oxides. The Q_{BD} value of pyrogenic oxides is improved by H_2 POA, which is twice higher than that without H_2 POA. On the other hand, the Q_{BD} values of the dilute-DRY/N_2O oxides without and with H_2 POA are almost the same. The sample (c) has the highest Q_{BD} of 15.9 C/cm^2, which is plotted in a wear-out failure region of Weibull distribution curve, in all the samples. These results indicate the H_2 POA after oxidation is effective in an improvement of channel mobility and oxide reliability for the MOS structure on 4H-SiC $(11\bar{2}0)$ face.

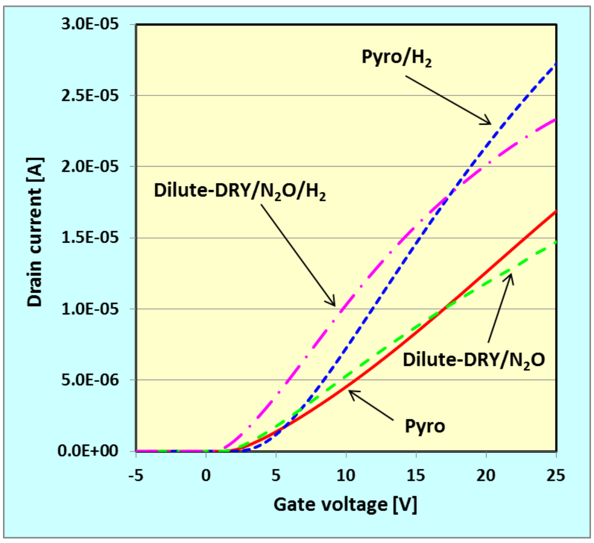

Fig. 1 I_D-V_G characteristics for four planer Al-gate MOSFETs at 25ºC.

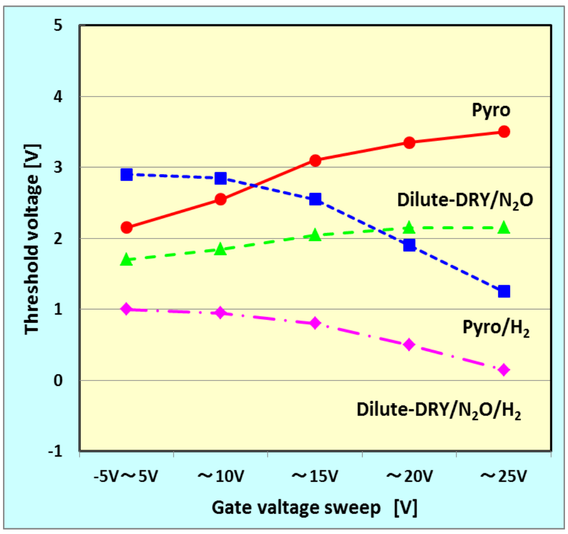

Fig. 2 V_{TH} shifts for four planer Al-gate MOSFETs using repeated I_D-V_G sweep test at 25ºC.

Figure 2 shows shifts of V_{TH} of four Al-gate MOSFETs measured by a repeated I_D-V_G sweep test at 25ºC. The V_G sweep sequence of this test is shown in Fig. 3. In this test, first of all, an I_D-V_G curve was measured by a 1st V_G sweep range from -5 V to 5 V in an as-fabricated MOSFET. Next, in the 2nd V_G sweep range from -5 V to 10 V, it measured I_D-V_G curve again. Then, this repeated I_D-V_G sweep was performed in the same MOSFET until an end point of V_G sweep range became 25 V by an increase voltage step of 5 V. The V_{TH} value was the V_G when the I_D was 100 nA. The positive V_{TH} shifts were observed on the MOSFETs without H_2 POA (samples (a) and (c)), but the negative shifts of V_{TH} were confirmed on those with H_2 POA (samples (b) and (d)). The V_{TH} differences between 1st and 5th V_G sweeps are 1.4 V, -1.7 V, 0.5 V and -0.9 V in the samples (a), (b), (c) and (d), respectively. The V_{TH} difference of the sample (c) is the smallest in all the samples, indicating the best V_{TH} stability in the dilute-DRY/N_2O oxides.

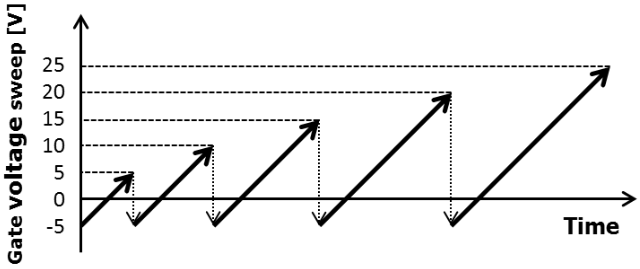

Fig. 3 Gate voltage sweep sequence of repeated I_D-V_G sweep test.

To estimate the V_{TH} instability under a practical device operation condition, V_{TH} shift of a poly-Si-gate MOSFET with dilute-DRY/N_2O oxide was measured at the temperature from -40ºC to 200ºC. Figure 4 shows the V_{TH} shift as a function of stress time for V_D = 1 V and 25ºC. In this figure, the vertical axis in the left side is the V_{TH} value at I_D of 100 nA in the I_D-V_G curve measured by the V_G sweep from -5 V to +10 V, and the right side axis indicates the V_{TH} shift (ΔV_{TH}) from an initial value at a stress time of 0 s. The stress V_G values were +15, -5 and 0 V, and each stress period was 2000 s. The positive V_{TH} shift was observed when the stress V_G of +15 V was applied to the sample. On the contrary, V_{TH} decreases during the negative V_G stress of -5 V. And the negative V_G shifts were confirmed at the stress period of 0 V after both the positive and negative V_G stress periods. These ΔV_{TH} values are extremely small and less than 10 mV. In addition, no degradation of μ_{FE} of MOSFET by this stress cycles at 25ºC was observed. Temperature dependence of V_{TH} instability for the same MOSFET is shown in Fig. 5. In this figure, red curves show results for the stress V_G of +15 V and stress time of 10000 s, while blue ones for the stress V_G of -5 V and stress time of 6000 s. Also, filled and open symbols are V_{TH} and ΔV_{TH}, respectively. Here, the ΔV_{TH} is a shift amount of V_{TH} during the same V_G stress of 2000 s. Both V_{TH} values after the positive and negative V_G stress periods decrease

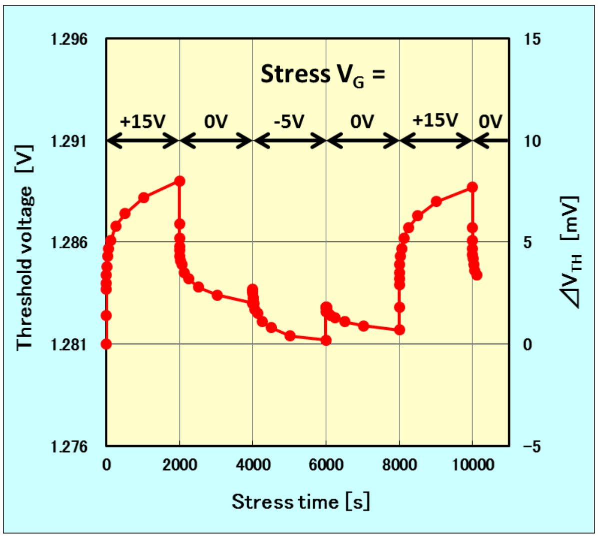

Fig. 4 V_{TH} and ΔV_{TH} variations as a function of stress time for V_D = 1 V and 25ºC.

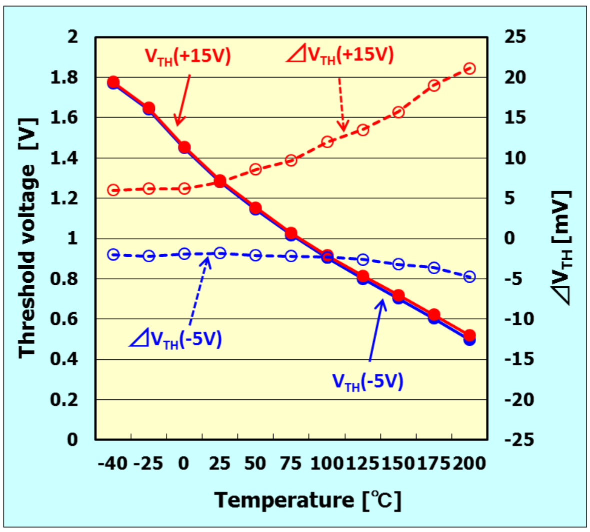

Fig. 5 Temperature dependences of V_{TH} and ΔV_{TH} under the stress V_G of +15 and -5 V.

with an increase in the temperature, and their behaviors are almost the same. Difference of V_{TH} between -40ºC and 200ºC is about 1.3 V. Also, it is shown that ΔV_{TH} becomes large with temperature. At the temperature between -40ºC and 200ºC, the ΔV_{TH}(+15V) and ΔV_{TH}(-5V) increase by 350% and 230%, respectively. At 200ºC, V_{TH} values after positive and negative stress V_G periods of 2000 s are 0.52 and 0.50 V, respectively, which indicate the normally-off operation of MOSFET even at high temperature. Besides, the channel mobility of MOSFET also monotonically decreases from 91.7 cm^2/Vs at -40ºC to 52.5 cm^2/Vs at 200ºC, but maintains at each temperature during the V_{TH} instability test. These results indicate that the MOS structure formed by N_2O POA after dilute-DRY oxidation on the 4H-SiC $(11\bar{2}0)$ face has an excellent V_{TH} stability as well as high channel mobility and high oxide reliability.

Summary

In this study, we have investigated electrical properties of MOS structures on 4H-SiC $(11\bar{2}0)$ face using various gate oxidation procedures. The μ_{FE} values of n-channel MOSFETs with gate oxides by pyrogenic and dilute-DRY/N_2O processes are 88.6 and 57.2 cm^2/Vs, respectively. On the contrary, the Q_{BD} for the dilute-DRY/N_2O sample is about 10 times higher than the pyrogenic one. H_2 POA after the oxidation has an effect on improvement of channel mobility, and higher μ_{FE} than 100 cm^2/Vs was achieved in both pyrogenic and dilute-DRY/N_2O samples. However, the H_2 POA has an insignificant impact on the oxide reliability, and makes V_{TH} instability worse in both the samples. Repeat I_D-V_G sweep measurement indicates the V_{TH} shift of MOSFET with the dilute-DRY/N_2O oxide is smallest among the all samples. According to estimate the V_{TH} instability at the temperature from -40ºC to 200ºC, V_{TH} decreases with an increase in temperature, but is about 0.5 V at 200ºC, indicating the normally-off operation of MOSFET even at high temperature. Also, the ΔV_{TH} values after positive and negative V_G stress cycles of 2000 s are 21 and 5 mV at 200ºC, respectively. These results represent that the MOS structure grown by dilute-DRY followed by N_2O POA has an excellent ability for a practical use of SiC MOS power devices.

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References

[1] S. Onda, R. Kumar, and K. Hara, Phys. Stat. Sol. (a), 162 (1997) 369-388.

[2] S. Harada, S. Ito, M. Kato, A. Takatsuka, K. Kojima, K. Fukuda, and H. Okumura, Mater. Sci. Forum, 645-648 (2010) 999-1004.

[3] Y. Nakano, R. Nakamura, H. Sakairi, S. Mitani, and T. Nakamura, Mater. Sci. Forum, 717-720 (2012) 1069-1072.

[4] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, K. Asano, and Y. Sugawara, IEEE Electron Device Lett., 20 (1999) 611-613.

[5] J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Suzuki, T. Suzuki, and K. Fukuda, IEEE Electron Device Lett., 23 (2002) 13-15.

[6] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami., Jpn, J. Appl. Phys., 44 (2005) 1213-1218.

[7] T. Endo, E. Okuno, T. Sakakibara, and S. Onda, Mater. Sci. Forum, 600-6003 (2009) 691-694.

[8] E. Okuno, T. Endo, J. Kawai, T. Sakakibara, and S. Onda, Mater. Sci. Forum, 600-603 (2009) 1119-1122.