Testability Analysis and Multi-frequency ATPG for Analog Circuits and Systems

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Abstract

Fast and efficient test generation techniques are key to reducing the current high cost of testing analog circuits. A new multi-frequency test generation technique for detecting catastrophic failures in this class of circuits is presented. Testability transfer factors are introduced and we use them to construct an efficient test set for analog circuits. Fault detectability and fault coverage are also defined. Two circuits from the suite [4] of analog and mixed-signal benchmark circuits are used to validate our approach.

1: Introduction

Analog testing has been traditionally approached as verifying a subset of the specifications - the selection of the specific subset dictated by the application on hand. Although functional tests are effective in detecting faults, they are expensive in terms of test resources and typically involve collection of a large number of samples. Alternative test excitations which are designed to exploit the specific structural differences between the defective and non-defective circuits bear promise in reducing the cost of testing.

1.1: Previous work in analog testing

Fault based approaches to analog testing have focused on the construction of fault-dictionaries before manufacture through simulation. In [8] the authors presented an algorithm to construct the signatures and evaluate the detectability of a set of DC measurements. A search technique in the frequency domain similar to the digital ATPG approach to select the best test frequency for linear circuits was presented in [7]. Most of the prevailing methods are fault analysis methods, where the effect of faults are analyzed under a known excitation. In [6], the authors used sensitivity analysis as the basis for selecting test frequencies but no automated procedure was described. A min-max framework was presented in [1] and [2] however this approach requires building a surface response of the circuit under test (CUT). The authors described building the surface response through simulations and for small circuits, simulation times can be tolerable but not so for large analog and mixed-signal systems. In [5], a method was described to shorten simulation times through behavioral modeling of macro blocks. The authors in [3] described a hierarchical specification driven technique to capture faults using simulation based methods. For larger circuits, simulation times can be intolerable.

1.2: Our contribution

This paper describes the development of two measures to characterize the controllability and observability properties of the internal nodes of analog circuits. These measures are used to generate an efficient test set for the circuit under analysis. The intent is to provide a quantitative measure of the difficulty of controlling and observing the signal values of internal nodes.

> Controllability Measure: The relative difficulty of setting a node to a specific value. This measure is normalized to range between 0.0 to 1.0 with 1.0 being totally controllable and 0.0 being totally uncontrollable. Primary Inputs (PIs) are by definition totally controllable.
>
> Observability Measure: The relative difficulty of propagating an error from an internal node to a primary output. This measure is normalized to range between 0.0 to 1.0 with 1.0 being totally observable and 0.0 being totally unobservable. Primary Outputs (POs) are by definition totally observable.

Section 2 describes the derivations for the testability transfer factors and section 3 presents the controllability and observability measures. Section 4 describes our multi-frequency test generation technique. Our technique is used to detect catastrophic faults such as opens and bridging shorts. Section 5 discusses the results of our approach and section 6 concludes the paper.

2: Testability transfer factors

The concept of Testability Transfer Factor (TTF) of a component was first devised by Stephenson and Grason [9] for digital circuits. The underlying idea is that test information must be propagated through components to other components or to primary outputs, a means must be employed to determine how controllabil-

ity and observability is affected in route. The TTF of a component represents:

1. The ease of achieving an arbitrary signal on its outputs by exercising its inputs.
2. The ease of determining whether a specific signal occurred on its inputs by examining the values on its outputs.

We used a similar approach in deriving the testability transfer factors (TTF) for components. The following derivations are for components and a component is defined as a building block in which the designer can use but does not have access to the internals of the component. Examples include resistors, diodes, operational amplifiers and others. Higher level component examples include such macro blocks as analog-to-digital converters (ADCs), phase lock loops (PLLs), etc.

2.1: TTF for passive components

Consider two subcircuits in a circuit coupled through a resistor with resistance *R* at nodes *a* and *b* (refer to figure 1). *PIs* indicate primary inputs and *POs* indicate primary outputs. Node *b* is controllable by node *a* only if a current of magnitude *I* can flow from node *a* to node *b* as according to Ohm's Law. Then we can conclude that node *b* is perfectly controllable by node *a* if *R* = 0 (short circuit). That is any voltage appearing in node *a* will also appear on node *b*. Furthermore, if *R* equals to infinity (open circuit), then node *b* is perfectly uncontrollable by node *a* since no current can flow into an open circuit. Similarly, node *a* is perfectly observable by node *b* if *R* = 0 because any voltage appearing on node *a* will appear on node *b* as well. Also, node *a* is unobservable by node *b* if *R* is equal to infinity because with zero current, voltage at node *a* can not be inferred even if the voltage at node *b* is known.

Therefore, the TTF for a resistor with resistance *R* is:

$$T_f(R) = 1 - \frac{R}{OC} \qquad (2.1.1)$$

Where *OC* is the open circuit condition and is commonly modeled by a resistor with a high resistance [10]. In this work, the open circuit condition is modeled by a 10 MΩ resistor. A 10 MΩ resistor is sufficient for our work because most of the resistance values are well below 1 MΩ. Furthermore, the OP27 op-amp (a high performance op-amp) has an input impedance of well over 6 MΩ (at DC) and that is considered an open circuit for most analog applications. The *OC* value is user defined and it depends on the application and technology.

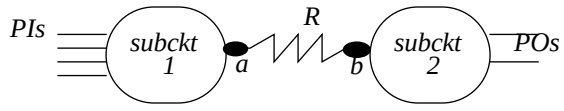

Figure 1: Two subcircuits coupled through resistor R

Capacitors and inductors can be viewed as frequency dependent resistors. Therefore, the resistance *R* in equation (2.1.1) can be replaced by *R(ω)* or in general *Z(ω)* where *Z* represents the component's impedance and ω is the radian frequency. Figure 2 shows the signal flow graph (SFG) for an impedance device. The bi-directional nature of these components are modeled as two uni-directional links with identical weights but opposite directions. The weight of each link is the TTF value of equation (2.1.1).

2.2: TTF for operational amplifiers

An ideal op-amp with input terminals V^+ and V^- and output terminal V_o is characterized by its input null port and zero output resistance. The input terminals are a virtual short for voltages and a virtual open for currents, respectively. This implies that the op-amp's differential gain is infinite. The two input terminals track each other as long as the differential gain is sufficiently large. For an ideal op-amp with infinite bandwidth and infinite differential gain, the input terminal are controllable and observable with respect to each other. As a result, the TTF must approach 1. Furthermore, as the differential gain approaches zero, the input terminals will not track each other and therefore, the TTF must approach zero as well. Since the differential gain can have a wide range of values, the logarithm function is chosen for computation of the TTF between the input terminals (as shown in equation (2.2.1)). The underlying idea is similar to expressing the differential gain in decibels except decibels can take on negative values while TTFs are restricted to a value between 0 and 1 as explained in subsection 1.2.

$$T_f(A_{dm}) = 1 - \frac{1}{\log(A_{dm} + 10)} \qquad (2.2.1)$$

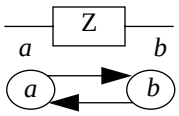

Figure 2: Signal flow graph for an impedance

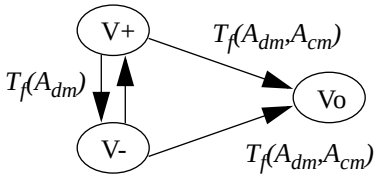

Figure 3: Signal flow graph for an op-amp

Where A_{dm} is a three pole gain function typical used for practical op-amps [11] and has the following form:

$$A_{dm}(f) = \frac{A_{dc}}{\sqrt{\left(1+\left(\frac{f}{f_1}\right)^2\right)\left(1+\left(\frac{f}{f_2}\right)^2\right)\left(1+\left(\frac{f}{f_3}\right)^2\right)}} \qquad (2.2.2)$$

And

A_{dc}	=	Differential gain at DC
f_1	=	First (dominant) pole
f_2	=	Second pole
f_3	=	Third pole

The op-amps output terminal can be "tickled" by stimulating the input terminals with a small differential signal. The output of an op-amp is equal to the differential gain times the voltage difference between the input terminals. An ideal op-amp will only respond to differential signals and common mode signals are rejected. Thus, it is more appropriate to consider both the common mode gain and differential gain when calculating the TTF from the input terminals to the output terminal. The derivation for equation (2.2.3) is similar to the derivation for equation (2.2.2) except in this case we are using the op-amp's common mode rejection ratio (CMRR). With a high CMRR, it is easier to control the output and observe the inputs. With a low CMRR, it is more difficult to control the output and observe the inputs.

$$T_f(A_{dm}, A_{cm}) = 1 - \frac{1}{\log\left(\frac{A_{dm}}{A_{cm}} + 10\right)} \qquad (2.2.3)$$

Where A_{dm} is the differential mode gain of equation (2.2.2) and A_{cm} is the common mode gain. Figure 3 shows the SFG for the op-amp.

Non-ideal effects of the op-amp can be modelled by circuit elements and once we have the effects modelled by circuit elements, we can calculate the TTF by using the corresponding TTF equation. For example, the op-amp's input impedance can be modelled by a parallel RC network connecting the positive and negative terminals. Once we determine the R and C (which are part of the specifications on the op-amp's data sheets) values, we can use equation (2.1.1) to calculate the TTFs.

The above derivations are for op-amps used in closed loop configurations. In open loop configurations, op-amps will essentially function as comparators and within the scope of our work, comparators are viewed as single bit ADCs. We are currently working on the development of an ADC model.

2.3: Circuit building blocks

TTFs for other circuit building blocks can be derived using a similar analysis. For example, operational transconductance amplifiers (OTAs) are very similar to op-amps and by following the same lines of derivations, we can develop TTFs for the OTA. Currently we have developed models for MOSFETs, BJTs, diodes and other circuit elements. However, their complete derivation is omitted here for brevity.

3: Controllability, Observability and Testability Measures

3.1: Controllability measure

The input controllability of a component represents the ease of achieving an arbitrary signal value at the component's input and it depends on the controllability of the input connections and the components it is connected with. The output controllability of a component represents the ease of producing an arbitrary signal value on the outputs of the component. It depends on the input controllability and the TTF of a component or:

$$C_{out} = TTF \bullet C_{in} \qquad (3.1.1)$$

To calculate the controllability of a node, transform the circuit schematic into a SFG with each vertex representing the nodes in the circuit and each edge representing the components in the circuit. The direction of the edges represent the direction of signal flow through the component and the weight of each edge is the corresponding component's TTF. The controllability for any node (or any vertex in the SFG) *i* is:

$$C_i = \frac{1}{F_{in}} \sum_{m=1}^{F_{in}} C_m \bullet TTF_m \qquad (3.1.2)$$

Where:

C_i = Controllability of node *i*

F_{in} = Fan in of node *i*

C_m = Controllability at source node of fan in *m*

TTF_m = TTF of fan in *m*

3.2: Observability measures

The output observability of a component represents the ease of determining whether or not the expected signal value occurs there by observing the signal values at the primary outputs of the circuit. The input observability of a component represents the ease of determining whether or not the expected signal value occurs there by observing the signal values at the primary outputs of the circuit. Since the TTF represents the ease of propagating a signal through the component, we have:

$$O_{in} = TTF \bullet O_{out} \qquad (3.2.1)$$

The observability of any node (or any vertex in the signal flow graph) *i* is:

$$O_i = \frac{1}{F_{out}} \sum_{m=1}^{F_{out}} O_m \bullet TTF_m \qquad (3.2.2)$$

Where:

O_i = Observability of node *i*

F_{out} = Fan out of node *i*

O_m = Observability at destination node of fan out *m*

TTF_m=TTF of fan out *m*

A system of controllability and observability nodal equations is then formed. This system of linear equations can be solved for the controllability and observability measures at each node.

3.3: Testability measures

Since test generation will be difficult if either controllability or observability is low, the function chosen for the testability measure in this work is the geometric mean as shown in equation (3.3.1). However, the testability measure can be user defined for various different applications.

$$T_i = \sqrt{C_i \bullet O_i} \qquad (3.3.1)$$

Where T_i is the testability of node *i*, C_i is the controllability of node *i*, and O_i is the observability of node *i*.

3.4: Testability analysis procedure

The flow chart for the testability analysis procedure is shown in figure 4. A netlist describing the circuit is used as input. Step one is to calculate the TTFs for each component. Then, a SFG is formed from the netlist. Controllability and observability equations are formulated at each vertex according to equations (3.1.2) and (3.2.2). The equations constitute a matrix of nodal equations which are then solved via a matrix solver. Testability for each node is then calculated by using equation (3.3.1). A check is made to see if the range of frequencies under analysis is completed. If the range of frequencies is not completed, then the frequency is incremented and all the variables are recalculated for the new frequency point. The result is a profile of the circuit's testability as a function of frequency (frequency response of testability). This profile shows how testability changes as frequency changes.

4: Multi-frequency test generation

4.1: Automatic test pattern generation

Analog test generation in its simplest form can be viewed as finding an input which maximizes the error between the good and the faulty circuit. For ease of notation, we denote,

$$E = S_g - S_f \qquad (4.1)$$

Where:

E = magnitude of the error

S_g = the signature for the good circuit

S_f = the signature for the faulty circuit

We can apply this principle to the testability profiles dis-

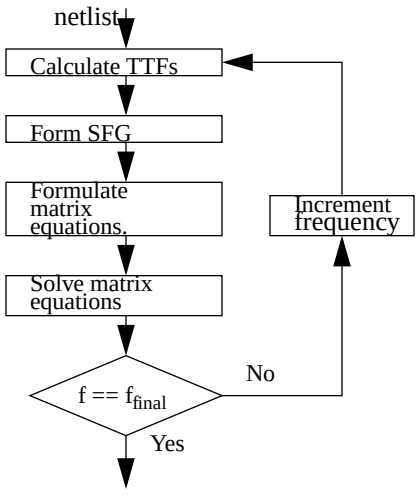

Figure 4: Testability analysis chart

cussed in the previous sections. Let

$$E(F) = \left| T_g(F) - T_{fi}(F) \right| \qquad (4.2)$$

Where:

- E = magnitude of the error response
- F = frequency variable
- T_g = testability profile of the good circuit
- T_{fi} = testability profile of the faulty circuit with fault f_i

Hence, we can define the detectability of fault *fi*, D_{fi}, as the integral of the error response over a frequency range. Equivalently,

$$D_{fi} = \int_{F_{init}}^{F_{final}} E(F)dF = \int_{F_{init}}^{F_{final}} \left| T_g(F) - T_{fi}(F) \right| dF \qquad (4.3)$$

The larger the D_{fi} , the easier it is to detect the fault *fi*. The smaller the D_{fi}, the harder it is to detect the fault *fi*. If $D_{fi} < D_{thrs}$, then our method can not generate a test vector to detect fault *fi*. For any $D_{fi} > D_{thrs}$, we can generate a test vector to detect fault *fi*. D_{thrs} is a user defined threshold which depends on the amount of tolerable process (or component) variations.

Automatic test pattern generation procedure

Step 1: Calculate $T_g(F)$.
Step 2: Calculate $T_{fi}(F)$ for fault *fi*. Catastrophic faults especially opens and bridging shorts are studied in this work. Opens are modelled by a 10 MΩ resistor while bridging shorts are modelled by 1 Ω resistors.
Step 3: Calculate D_{fi} according to equation (4.3).
Step 4: If $D_{fi} < D_{thrs}$, then we can not generate test to detect fault f_i, skip to step 9. Otherwise continue to step 5.
Step 5: Transform *E(F)* into a filter frequency response $|E(e^{j\omega})|$. *E(F)* contains the frequencies or range of frequencies in which $T_g(F)$ differs from $T_{fi}(F)$. This implies that at these frequencies or range of frequencies, the response of the good circuit differs from that of the faulty circuit. Therefore, we want to generate a signal with these frequency components. To generate $|E(e^{j\omega})|$ from *E(F)*, we place a zero in $|E(e^{j\omega})|$ for all the frequencies or range of frequencies in which *E(F)* is zero and place a one in $|E(e^{j\omega})|$ for all the frequencies or range of frequencies in which *E(F)* is non-zero. The phase of $E(e^{j\omega})$ is made linear to eliminate any phase distortion.
Step 6: Calculate inverse transform of $E(e^{j\omega})$ to get *e(t)*.
Step 7: Convolve *e(t)* with δ to produce $v_{fi}(t)$. *e(t)* is the system response of the filter derived from *E(F)*, therefore, by convolving the system response with the δ function, we produce a signal with the frequency components from step 5. This signal can then be use as a test pattern to detect fault *fi*. $v_{fi}(t)$ can be produce by an arbitrary waveform generator (AWG) in the time domain by using piece wise linear segments.
Step 8: Add $v_{fi}(t)$ to test set **V**.
Step 9: Remove fault *fi* from fault list.
Step 10: Select another fault from fault list and go back to step 2.
Step 11: Repeat till fault list is empty.

Let n_f be the total number of faults in the fault list and n_i be the number of faults detected by the test set **V**, then the fault coverage is defined as the ratio of n_i over n_f or:

$$C = \frac{n_i}{n_f} \qquad (4.4)$$

4.2: Signature analysis

In the dynamic case, due to noise and tolerance the exact comparison of time-domain waveforms is an experimental impossibility. Hence, any detection scheme must use some measure of the waveforms as a basis for comparison. Such measures on the waveform are also referred to as signatures of the waveform. One popular signature is the frequency response of the circuit or system under consideration. The signatures are obtain by taking time domain measurements at the primary outputs of the circuit and then performing the fourier transform on the measured data via software.

Figure 5 shows the signature analysis methodology used. The test set **V**, generated by the procedure described in subsection 4.1, is used as input for both the good circuit and the faulty circuits. The outputs of both circuit are then passed into the fast fourier transform box which computes the fourier transforms. The outputs are then passed into a subtracter which takes the difference of the two signatures. If there is a difference, absolute value of ΔS equal to or greater then S_{thres}, then the fault *fi* is detected by the test set **V**. Otherwise, the fault *fi* is not detected (absolute value of ΔS less then S_{thres}). S_{thres} is a user defined threshold which depends on the accuracy of the equipments used.

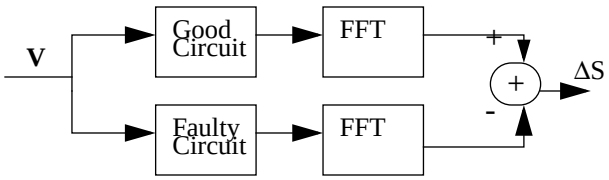

Figure 5: Signature analysis methodology

5: Results

We have implemented the procedure described in section 4 with various C code, shell scripts and MATLAB code and applied the test generation procedure and signature analysis methodology on two circuits from the suite of analog and mixed-signal benchmark circuits - first release [4], a continuous-time state variable filter and a leapfrog filter.

5.1: Continuous-time state variable filter

The continuous-time state-variable filter under consideration is shown in figure 6 where HPO is high-pass output, BPO is band-pass output, and LPO is low-pass output. The current benchmark circuit has the following values: R1 = R2 = R3 = R4 = R5 = 10K, C1 = C2 = 20nF, R6 = 3K, and R7 = 7K. Table 1 shows the fault list and the associating detectabilities.

Table 1: Fault list state variable filter

f_i	Faults	D_{fi}
f_1	Nodes 2 &3 short	0.0112
f_2	Nodes 5 &0 short	0.5641
f_3	Nodes 7 &0 short	0.5862
f_4	Nodes 2 &4 short	0.0156
f_5	Nodes 5&6 short	0.4494
f_6	Nodes 7&8 short	0.4288
f_7	R1 open	13.7937
f_8	R2 open	0.6090
f_9	R3 open	0.3805
f_{10}	R4 open	0.4370
f_{11}	R5 open	0.2490
f_{12}	R6 open	13.2188
f_{13}	R7 open	13.2188

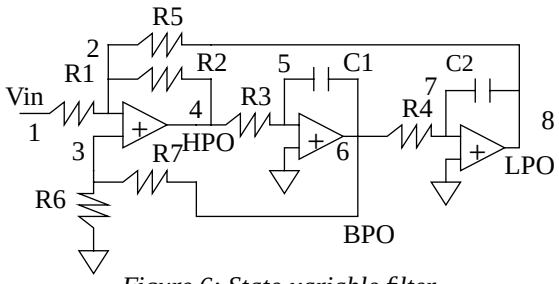

Figure 6: State-variable filter

Table 1: Fault list state variable filter

f_i	Faults	D_{fi}
f_{14}	C1 open	0.0595
f_{15}	C2 open	0.1350

Figures 8 and 9 shows the test patterns generated and the signatures of the HPO, BPO and LPO outputs of the state variable filter for faults f_1 and f_7. Fault f_1 has the lowest detectability and we see that is reflected in its signature. The signatures at the BPO and LPO of the good and faulty circuits are very similar in that they both have similar profiles and magnitudes. On other hand, the signatures for f_7 are significantly different at all three outputs. Although the BPO and LPO have similar profiles, the magnitudes between the good and faulty circuits are significantly different.

5.2: Leapfrog filter

The leapfrog filter under consideration is shown in figure 7. All resistors are 10K, C1 = C4 = 0.01μF, and C2 = C3 = 0.02 μF. Primary input is node 1 and primary output is node 13. Table 2 shows the fault list and the associating detectabilities.

Table 2: Fault list for leapfrog filter

f_i	Faults	D_{fi}
f_1	Nodes 2&0 short	4.7417
f_2	Nodes 4&0 short	4.9848
f_3	Nodes 6&0 short	5.3087
f_4	Nodes 8&0 short	6.3962
f_5	Nodes 10&0 short	6.3994
f_6	Nodes 12&0 short	0.5111
f_7	Nodes 2&3 short	0.0642

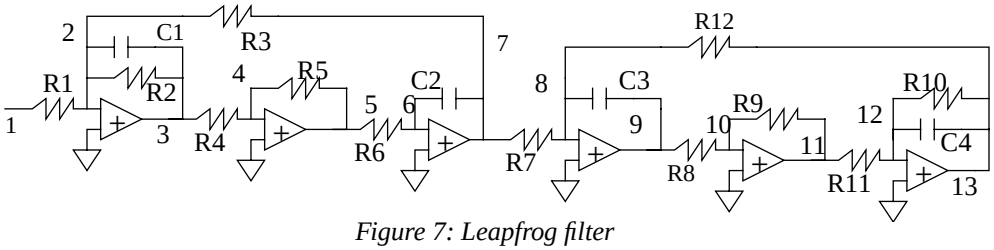

Figure 7: Leapfrog filter

Table 2: Fault list for leapfrog filter

f_i	Faults	D_{fi}
f_8	Nodes 4&5 short	0.0642
f_9	Nodes 6&7 short	0.7534
f_{10}	Nodes 8&9 short	0.6448
f_{11}	Nodes 10&11 short	0.0593
f_{12}	Nodes 12&13 short	0.3507
f_{13}	Nodes 2&7 short	0.0545
f_{14}	Nodes 8&13 short	0.0497
f_{15}	R1 open	47.9371
f_{16}	R2 open	1.0739
f_{17}	R3 open	3.0456
f_{18}	R4 open	0.2346
f_{19}	R5 open	0.2234
f_{20}	R6 open	0.4977
f_{21}	R7 open	47.9371
f_{22}	R8 open	0.1917
f_{23}	R9 open	0.2347
f_{24}	R10 open	0.6946
f_{25}	R11 open	0.2575
f_{26}	R12 open	3.3006
f_{27}	C1 open	0.9008
f_{28}	C2 open	0.1734
f_{29}	C3 open	0.3759
f_{30}	C4 open	0.4977

Figure 10 shows the test patterns generated for faults f_{14} and f_{21} and the signatures at the primary output node 13. Faults f_{14} and f_{21} produced the similar error response *E(F)* profiles however, their magnitude differ. This implies that f_{14} and f_{21} produced an error response with similar frequency components but different magnitudes (the detectabilities are different). Therefore the same test pattern is generated to detect both faults. From table 2 we see that fault f_{14} has the lowest detectability and faults f_{15} and f_{21} have the highest detectability, therefore indicating that faults f_{15} and f_{21} is more detectable then fault f_{14}. This is reflected in their respective signatures. The signature difference between the good circuit and the circuit with fault f_{21} is larger then the signature difference between the good circuit and the circuit with fault f_{14} as shown in figure 10.

We used the presented test generation procedure to generate test sets for all the faults in tables 1 and 2. The signature analysis methodology described above is used to analysis the test sets and the fault coverage (according to equation 4.4) is 100% for both circuits studied. The 100% fault coverage is only applicable to the given fault sets and that the $\Delta S > S_{thrs}$. We have more results which can be shown at the conference. We are currently applying this procedure to other analog circuits and extending this work to include parametric faults. We are also working on extending this procedure to the mixed-signal domain.

6: Conclusions

In this paper, we presented a new approach to test generation for analog circuits and systems. We were able to generate tests to detect catastrophic faults in analog circuits. We have demonstrated the utility of our approach by applying the procedure on several circuits from the analog and mixed-signal benchmark circuits.

Acknowledgments

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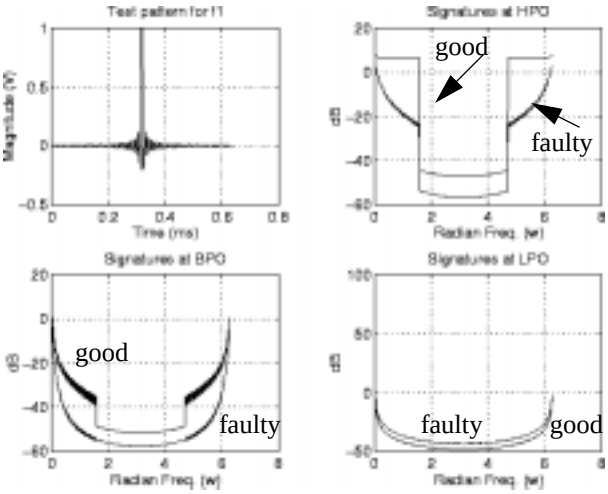

Figure 8: Test pattern and signatures for f_1

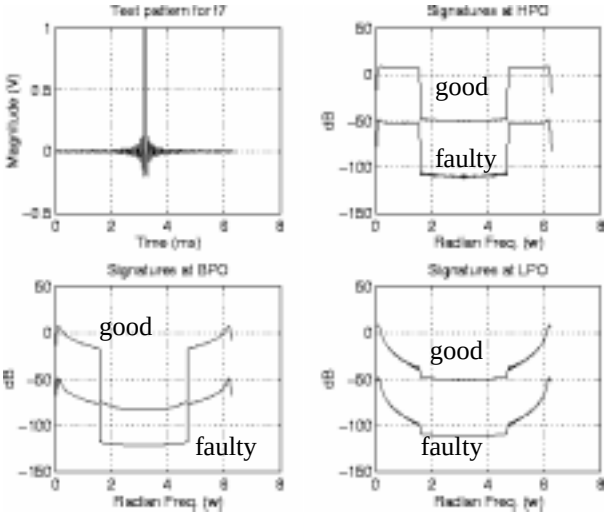

Figure 9: Test pattern and signatures for f_7

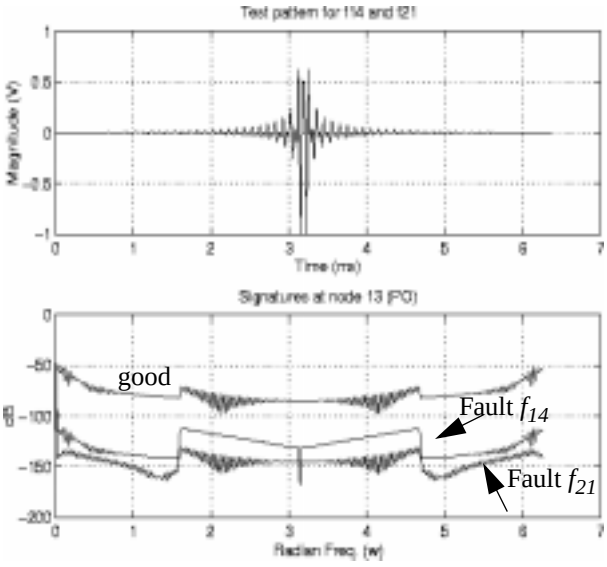

Figure 10: Test pattern and signatures for f_{14} and f_{21}