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AD630 Lock-in Amplifier Circuit for Weak Signal

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Abstract. Lock-in amplifying (LIA) is one of important techniques of picking up weak signals buried in the noise, and is the core component of Tunable Diode Laser Absorption Spectroscopy (TDLAS) technology. Then we design a small size, dual phase lock-in amplifier (LIA). This paper is based on the phase-sensitive detector AD630, together with the phase-locked loop (PLL) circuit (74HC4046) and the active filter (MAX275) the value of Q and the center frequency of which could be adjusted. The output signals were collected by A/D converter and dedicated high-resolution data acquisition card. The range of frequency is 500Hz-100 kHz, the dynamic range of acquisition signal is greater than 100dB, the signal-to-noise ratio is up to 60dB, and the overall area of circuit is only 14cm × 14.8cm. Experiments show that the design meets the requirements of integration into the system.

Introduction

Tunable Diode Laser Absorption Spectroscopy (TDLAS) technology is a new kind of gas detection techniques developed in these years [1, 2], provided with high sensitivity, high precision, and so on.

Among techniques used in TDLAS, the direct absorption method is used to measure small changes in large signal, so that the weak absorption signal is easily hidden in the background noise. In order to improve detection sensitivity and limits, they developed the wavelength modulation spectroscopy (WMS) [3, 4, 5]. Since WMS uses the high-frequency modulation of wavelength and harmonic detection technology, it is effective to suppress noise. To detect the concentration of substance rapidly, we need to use the principle of LIA to detect the harmonic of spectrum absorption. Even the noise component is several times greater than the signal itself, the noise can also be filtered out.

LIA has higher detection accuracy and is one of the most widely used instruments among many weak signal detection techniques, and it has a function of phase-sensitive detection and noise suppression [6, 7, 8]. LIA for sale in today's market is generally finished product, which is expensive, bulky, heavy and therefore not conducive to be embedded into systems. For commercial special test equipment, the input signal frequency range is relatively fixed, does not require frequent adjustment its parameters. This paper designs a small size and low-cost LIA to meet the needs of the laboratory and the system integration of some test measure instrument. Dual phase LIA is not sensitive to the phase reference signal [9, 10]; the phase is not fixed to avoid causing the test inaccurate. In order to ensure that the phase differences of two channels are 90 degrees, we chose a high-precision Phase Locked Loop (PLL) circuit.

The Principle

Lock-in amplifier is actually a simulation of the Fourier transformer. There are two kinds of LIA according to the structure, which are signal phase LIA and dual phase LIA. A basic single phase LIA consists of a reference signal channel, a signal channel, a phase sensitive detector (PSD), and a low-pass filter. This paper we choose the dual phase LIA. Dual phase LIA incorporate a pair of phase sensitive detectors (PSD) and this arrangement enables both the in-phase and quadrature components X and Y of a coherent signal to be measured simultaneously. The output of the reference channel is divided into two channels: one channel is θ, the other channel is θ+90°, and they are inputs as the driving signal of PSD respectively.

It can also produce an amplitude component R, which is independent of the detecting phase. During the operation, the amplitude of a coherent signal can be measured continuously without the need for phase adjustment, producing more precise and quicker result. Its block diagram is shown in Fig.1.

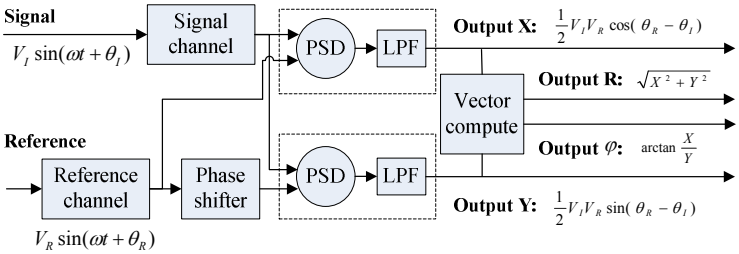


Fig.1 Dual Phase Lock-in Amplifier

The Implementation Scheme of Circuit System

This section includes 3 parts: the reference channel, the signal channel, and the AD data acquisition.

The Reference Channel. The reference signal circuit converts the input reference signal into the driving signal of PSD. Two PSD driving signals, having the duty of 50% and phase difference of 90°, must be accurate square wave and be free to change the phase to the input reference signal, so we need the phase-shift circuit. In this design, we use a PLL circuit, 74HC4046, achieving in phase with the reference signal input, producing four square-PSD driving signals having the same frequency and phase differences of 90 degrees respectively.

The standard application circuit, provided in 74HC4046, has non-linear frequency characteristics, limiting the range of lock-in. According to the datasheet, we design an improved circuit, as shown in Fig.2.

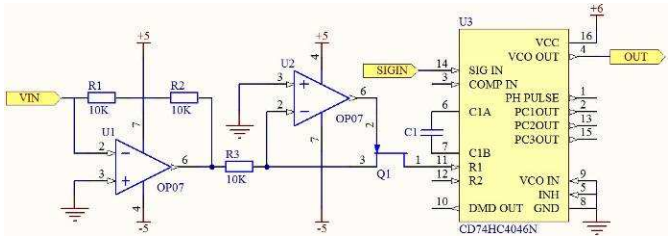


Fig.2 The improved circuit

The Fig.3 is obtained through simulation and experiments which achieves 0 ~ 4V linear voltage - frequency transformation, whose linear range and frequency band range are broadened obviously, and has excellent frequency characteristics. This design uses improved PLL circuit, which has good linear conversion, high transmission precision, wide output range, and simple circuit.

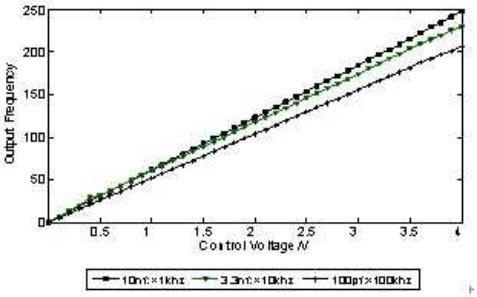


Fig.3 Test results: the oscillation frequency-control voltage characteristic curve of linear optimized circuit

Reference Trigger Circuit. From the Fig.4, we can see that the input of reference signal is a Sine wave and differential input, and the use of RL circuit prevents common mode noise; DC part is cut off, by high-pass circuit. U1 is an operational amplifier. U2 is a comparator which converts sinusoidal signal into logic electron square wave. U3B is an inverter. This circuit converts the reference sine wave into the square wave with the same frequency and phase.

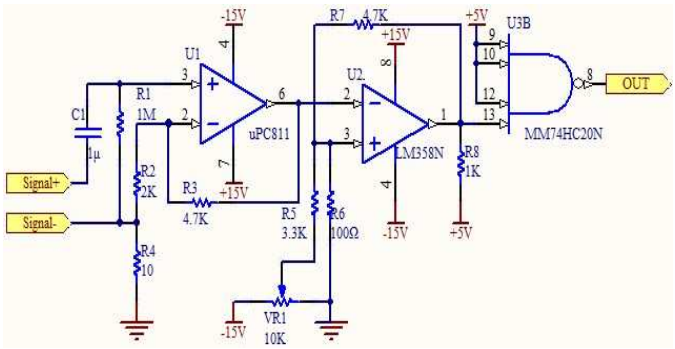


Fig.4 The trigger circuit of reference

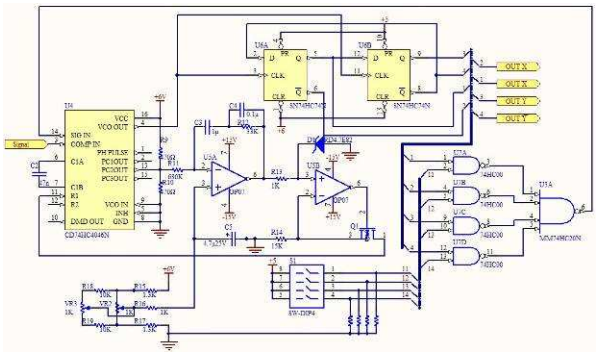


Fig.5 The PLL and Phase-shift circuit

Phase-locked Loop and Phase-shift Circuit [11]. The schematic diagram of PLL and Phase-shift circuit is shown in the Fig.5. The PLL circuit compares the frequency and phase of the input waveform with the voltage-controlled oscillator (VCO), and Synchronize the frequency of input signal and the VCO oscillation. PLL circuit contains a linear VCO and three different phase comparators (PC1, PC2 and PC3), and in this design we choose PC2 output, which is a positive edge-triggered phase and frequency detector. The square wave of the reference trigger circuit inputs to the PLL, COMP IN compared with the SIG IN to keep them equal both in frequency and phase. The phase adjusting circuit using Offset summarization with a minimum number of components puts DC bias on the LPF circuit which is behind PC2, so PLL circuit is locked to this bias voltage, which is equal to the phase. We can adjust the phase adjusting circuit potentiometer VR2 (coarse adjustment) and VR3 (coarse adjustment) to make the in-phase and inverting input voltage of U5A consistent, then the phase lock is set completely. Fig.6 shows the principles of Phase Locked Loop.

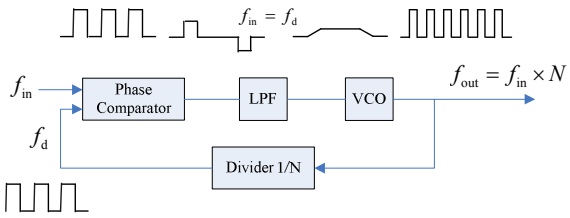


Fig.6 The principles of Phase Locked Loop

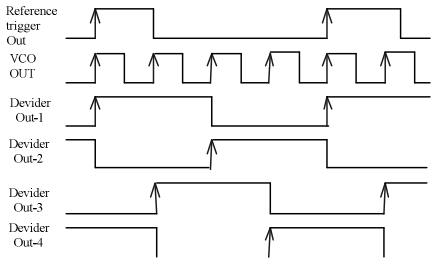


Fig.7 The waveforms of Phase-shift circuit

PLL Operating Principle. To drive two phase PSD, we need accurate 90° phase shift signal, so this design uses 1/4 frequency divider of 74HC74, which is often used as a logic clock circuit to produce 90° phase-shift signal. If the VCO output frequency is constant, then, the difference between four outputs is accurate 90°, as shown in Fig.7. By making one of the four signals in phase with the input signal, we can get two square drive signals of PSD.

The Signal Channel.

The Pre-amplifier Module. To amplify a signal that is below 1μV, we need preamplifier with a very low noise. The pre-stage uses BNC connector to amplify the small signal output from the differential detector and also considers the RFI problem, so the anti-RFI circuit is added in the first level, followed by the height-pass filter , to remove the DC offset of differential detector. The design uses AD620 instrumentation amplifier, which is used widely, has low noise, a simple interface, and requires just one resistor to adjust the gain, a high common mode rejection ratio, appearance indicator reaching 120dB. According to experience by experiment, we use a hybrid design, a simple filtering before the amplifier and a filtering after signal amplifier, to achieve a higher performance, so when the bandwidth of op-amp is constant, the higher the gain is, the smaller the cut-off frequency will be. The design results as shown in Fig.8.

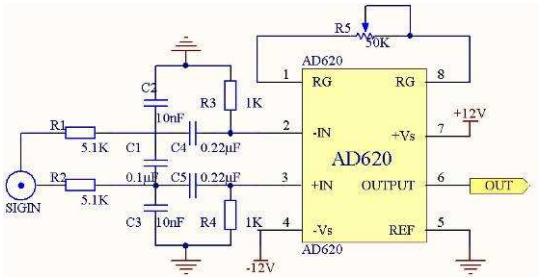


Fig.8 Pre-amplifier module

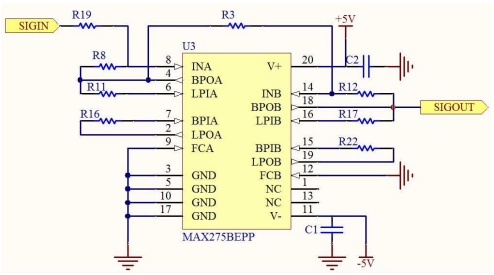


Fig.9 The schematic diagram of band-pass filter

The Band-pass Filter and Low-pass Filter (MAX275). When designing a circuit, the filter will have a direct impact on overall system performance. Common hardware active filter which consists of operational amplifiers and R, C components, is easy to implement, but the parameter modulation is difficult. When the working frequency is high, the surrounding stray capacitance will seriously affect the filter characteristics, which will deviate from the pre-working state. The MAX275 are continuous-time active filters consisting of two independent cascadable 2nd-order sections. Each section can implement any all-pole band-pass or low-pass filter response, such as Butterworth, Bessel, Chebyshev, and Elliptic, and is programmed by four external resistors. Its center frequencies range up to 300 kHz, and since it does not require a clock, aliased and clock noise are eliminated. MAXIM offers free design software, which is used to calculate the exponent number of filter, the zero-pole, the Q factor and the resistance value hence reducing manual calculation.

Take the band pass filter for example, we just need to choose the filter type and set the parameters in the main menu: Amax (the maximum attenuation in pass-band), Amin (the minimum attenuate in stop-band), Fc (the center pass-band frequency), Fbw (pass-band band-width), Fsw (band-pass width). The schematic of band-pass filter is shown in Fig.9.

The Phase-sensitive Detection Modules (AD630) [12].

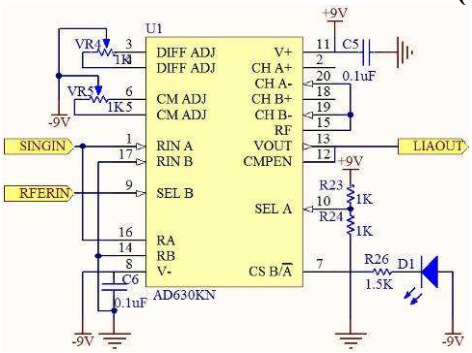


Fig.10 The AD630 module

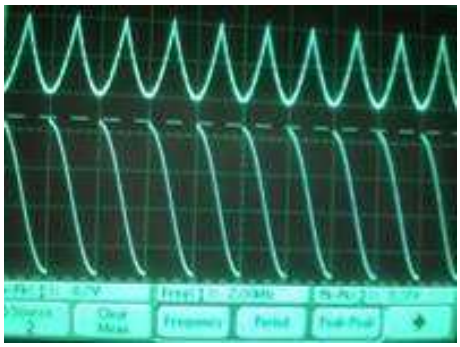


Fig.11 The PSD's output waveforms

This module in the Fig.10 is designed with the AD630 balanced modulator/demodulator, and my schematic is improved on the ADI laboratory circuit and chipset datasheet. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase-sensitive detection, lock-in amplification, and square wave multiplication. It is a high precision balanced modulator that combines a flexible commutating architecture with the accuracy and temperature stability, very low channel crosstalk, high common mode rejection ratio and adjustable gain and so on, afforded by laser wafer trimmed thin film resistors. Its characteristics include: wide unity gain bandwidth of 2MHz, high slew rate 45V/μs, extremely low crosstalk of -120dB/kHz, high-precision closed-loop gain error of 0.05%, low offset voltage of 100μV, a wide full power bandwidth of 350kHz, programmable closed-loop gain of ± 1 and ± 2, recovering signal from the 100dB noise.

The gain of AD630 is flexible and adjustable, and a gain of 2 is used here. According to the Fourier series decomposition relationship, the DC component is the average of output signal in time domain. When the phase difference of reference signal and measured signal is 0, the DC component output is:

$$V_{(PSD)} = \frac{1}{T}\int_0^T \frac{V_{PP}}{2} 2\sin(\frac{\pi}{T}t)dt = \frac{2}{\pi}V_{PP} \text{ (Gain of 2)} \quad (1)$$

The output load of LIA should be not too small; otherwise the chip may be over-heated. The rated power of chip is 600mW, and the actual power will change follow the load. It is a good choice to produce analog lock-in amplifier by AD630, reducing a lot about the design of the phase detector and the considerations for noise. From Fig.11, we can see that the output signal is very nice and the noise is relatively low (the upper signal is in-phase PSD output, and the below signal is quadrature output).

The AD Data Acquisition. This AD7190 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC), which can be configured to have two differential inputs. The output data rate from the part varies from 4.7 Hz to 4.8 kHz, which is enough for library use. It also has programmable gain array (PGA) (gain: 1~128), and it means that signals of small amplitude can be gained within it while still maintaining excellent noise performance. In this paper, the signal is single-ended input and the interface is SPI, as shown in Fig.12.

The SPI interface communicates using 51 or MSP430 microcontroller. The design described in this article is that the communication interface is a Single-ended connection that eases communication between different MCU. Applying the MSP430f159 chip to communicate with it, and then send the data collected to the upper computer by USB to Serial or wireless serial port, which uses Lab View for communication and programming to achieve secondary filtering and data processing.

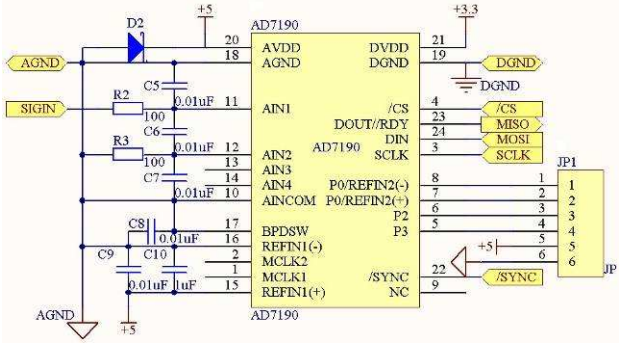


Fig.12 The AD data acquisition

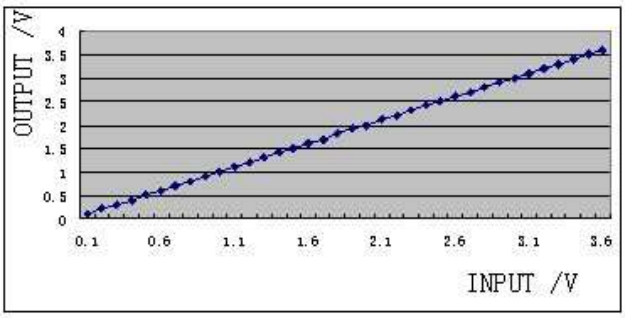


Fig.13 Linearity performance

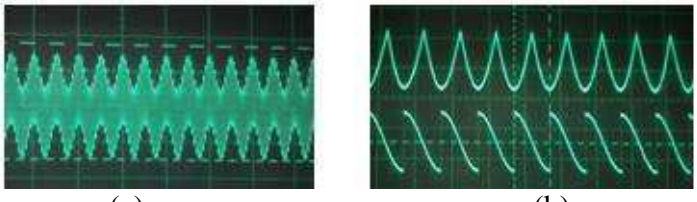
The Performance Test

The Linearity Correspondence Test of Lock-in Amplifier Circuit. Linearity is the linear correspondence of output and input signal magnitude, an important indicator of LIA, and it characterizes the performance of phase sensitive detector.

When the input signal is 0, by adjusting the VR4 and VR5 shown in Fig.10 to compensate the static output of AD630 and be sure that its output voltage is 0. We produce a sine wave of 1 kHz as input signal of both reference channel and signal channel. Change the input signal amplitude, and measure the output signal amplitude of in-phase PSD, and then we can obtain a curve between the input voltage and output voltage, as shown in Fig.13.

We can draw the following conclusion: the linearity did not change much with repeated experiments under the same conditions, and when it is above 0.9, this performance is perfect.

Weak Signal Detection under Strong Background Noise. A sine wave of 1 kHz, as the input signal, is coupled with a sine wave of 100 Hz, 250 mV, producing the curve shown in the Fig.14a. The in-phase PSD output is shown as upper curve, and the quadrature PSD output as shown in Fig.14b.



(a) (b)

Fig.14 (a): Coupled signal output; (b):AD630 signal output

Change the amplitude of x (t) from μV to mV, then compare the standard value and the measured result, we can get a performance of weak signal detection under noise as shown in TABLE I and TABLE II.

TABLE I The measurement result

Standard(μV)	Measured(μV)
1	1.1
10	9.6
50	52.6
100	102.3
200	198.5
500	497.5

TABLE II The measurement result

Standard(mV)	Measured(mV)
1	0.9
10	9.8
100	99.6
500	500.3
1000	999.2
2000	2090

Conclusions

This article describes a small sized dual phase LIA based on instrumentation amplifier, active filter, PLL, PSD and 24bitADC, and it has the following features: simple structure, highly integrated, stable and repeatable. The frequency range can be adjusted between 500Hz~100 kHz, Signal to Noise Ratio can reach 60dB, linearity is as high as 0.9, and the cost is relatively low. In summary, this LIA based on AD630 can work well in the laboratory TDLAS system for weak signal diction.

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