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SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter

CICC Gives Chip Designers a Jump Start

In today's fast-moving world, maintaining leading-edge technical skills is more important than ever. Now is the time to invest in your technical future and stay competitive. Attending the 2002 IEEE Custom Integrated Circuits Conference will provide educational and networking opportunities crucial to design engineers in the current economic environment.

The 24th IEEE Custom Integrated Circuits Conference (CICC) will be held 12–15 May 2002 in Orlando, Florida. CICC is dedicated to IC development, showcasing original first-published technical work and innovative circuit techniques tackling practical problems. Long known as a premier conference for information on leading-edge analog and digital circuits, CICC has evolved with the industry to cover a broad spectrum of technical topics. CICC offers attendees a total educational experience including paper presentations, exhibits, panels, tutorials, and interesting networking events.

This year the program consists of three in-depth educational sessions, twenty-one advanced technical sessions, and three panel discussions, enhanced by a technical/commercial exhibit, exhibitor preview sessions, and networking opportunities.

Educational Sessions—Sunday, 12 May

The conference starts with three full-day educational sessions on Sunday, 12 May. These sessions are taught by practicing experts who work at the

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2002 Symposium on VLSI Circuits

The Symposium on VLSI Circuits will meet 13–15 June 2002 in the Hilton Hawaiian Village, Honolulu, Hawaii. This year the technical program committee reviewed 225 submissions to the conference and chose 84 papers for inclusion in the technical program. The unusually high number of submitted top-quality technical papers has resulted in a technical conference that promises to be bigger and better than ever. With these featured papers, it can be truly said that anyone not in Hawaii during the second week of June will miss an unprecedented unveiling of technical knowledge. Papers describing new and innovative demonstrations of leading-edge concepts dominate every session. The three days of technical presentations and the informal evening rump sessions are a companion conference to the Symposium on VLSI Technology, which precedes it at the same hotel. The one-day overlap in the schedules for the Technology and Circuits meetings features a Short Course as well as a joint rump session on the major technical questions being discussed at leading semiconductor companies around the globe.

The scope of the Circuits Symposium covers all aspects of VLSI circuits, such as:

- Circuits for digital, analog, memory, communications, and signal-processing applications, including A/D and D/A
- Processing applications, including A/D and D/A converters, mixed analog/digital functions, and interface circuits

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leading edge of their field. The topics for these sessions are:

Educational Session 1: Advanced RF: From Devices to Systems

RF Performance and Modeling of CMOS Devices—Dirk Klaassen, Philips Research Labs

RFIC Receiver Circuits—John Long, Delft University of Technology

Key Issues in Transmitter Blocks—Earl McCune, Tropian Inc.

From RF System to Silicon—Asad Abidi, University of California

Educational Session 2: Advanced Data Converter Design and Test Techniques

Introduction to Delta-Sigma Data Converters—Bob Adams, Analog Devices

Multi-Bit Mismatch-Shaping DACs for High-Performance Delta-Sigma Data Conversion—Ian Galton, University of California, San Diego

Practical Aspects of Nyquist-Rate Switched-Capacitor ADCs—David Nairn, Analog Devices

State of the Art Lab Characterization Methods for High-Speed ADCs and DACs—Steve Reine, Analog Devices

Educational Session 3: High-Performance and Low-Voltage Design Challenges and Techniques

Low-Power Circuits and Xscale—Larry Clark, Intel Corporation

Leakage Control and Leakage-Tolerant Circuits—Kaushik Roy, Purdue University

SOI Design Challenges—Andrew Marshall, Texas Instruments

Low-Power Memory Design—Betty Prince, Memory Strategies International Inc.

Technical Program—Monday, 13 May–Thursday, 16 May

Keynote speaker Christine King, CEO of AMI Semiconductor, opens the technical program with "Smart Management of ASIC Requirements and Technology (SMART)," a candid description of the semiconductor industry's battle to balance cost, performance, power, productivity, and time to market.

Technical sessions following the keynote showcase exceptional, in-depth technical papers describing the latest advancements in IC technology and design methods. As always, the technical sessions are highlighted by invited and tutorial papers presented by leading experts from industry and academia. This year there are many excellent papers, especially in the areas related to the communication revolution:

- Reconfigurable Hot SOCs
- Multi-Gigabit Systems and Circuits
- Modeling and Optimization Techniques
- Copper-Wired Communications
- Innovations in Programmable Logic: Architectures and Applications
- Design Approaches for Testability and Reliability
- Advances in Embedded Memory
- Low-Power Circuits and I/O
- Application-Specific Signal Processing
- Oversampled Data Converters
- Modeling for RF Design
- Receiver Architectures
- Sensors and Imaging

Enhancement Techniques for Integrated Passives
SOC Design Methodologies
Analog Techniques
DSP for Communications
Wireless Networking
Nyquist Converters and Techniques
Directions in Process Technology and Integration
Modeling for Signal Integrity

There also is a special in-session educational tutorial presented during Session 10 entitled "Delta-sigma converters for wireless transceivers" taught by Dr. Ian Galton of the University of California.

Panel Discussions—Tuesday, 14 May

Three spirited panel discussions feature experts sure to offer strong opinions on the following topics:

Design Challenges in Wireless LANs

Experts summarize the current state and next generation of the WLAN standards and debate whether 802.11 and Bluetooth are complementary or competitive technologies. Engineers designing these systems discuss issues involved in designing custom ICs for low-cost wireless LAN applications.

Will the Next Great Killer Technology Application Please Stand Up!

Who will lead the charge in the new millennium? Will it be the industry leaders with their R&D or will it be a few of the masses of high-tech startups that will rise to the top? Is the economy affecting innovation? The panelists share their views of where technology is taking us and what engineers will be working on in the future. This certainly will not be a single-minded perspective!

Can Scaling Continue at the Same Rate Below 0.10 µm? What Is the End of CMOS…and What Is Next?

Where does it end—or does it? Experts share their vision of the future process technology roadmap. Their opinions, based on their experiences, will help all involved in IC development to better prepare for the next technology advances.

Exhibits—13–14 May

Monday afternoon the exhibitor preview sessions kick off the opening of the Exhibits Hall. Here, many exhibitors present overviews of new products and services. As always, exhibits include displays and demonstrations by semiconductor manufacturers, software tool suppliers, design service houses, and leading electronics industry publications providing the latest technical information on new integrated circuit design products. The Exhibit Hall is also the site for Monday's Exhibitors' Reception and Tuesday evening's Happy Hour, opportunities for attendees to network with their colleagues and the exhibitors.

Luncheon Presentation—Wednesday, 15 May

The luncheon guest speaker is Eugene Trinh, director of the Physical Sciences Research Division in the Biological and Physical Research Enterprise at NASA. Dr. Trinh was a member of the Space Shuttle Columbia's crew in 1992. In his talk "Accomplishments and promises of research in low gravity," Dr. Trinh shares the results from his orbit research and gives the audience insight into future program directions. This promises to be a fascinating and educational experience.

Caribe Resort Suites, Orlando, Florida

The conference takes place at the Caribe Royale Resort Suites, Orlando, Florida. The Caribe Royale is an "all suites" hotel. Every room has a bedroom and a living/dining room. Parking at the hotel is free. The hotel features five restaurants, offers a complimentary full American breakfast buffet daily, and has an outdoor swimming pool with a water slide and a hot tub.

Orlando is "world famous" for its theme parks and family entertainment. The Caribe Royale is only 1.5 miles from the Walt Disney World Parks® and is close to Seaworld, Universal Studios, and MGM Studios.

Additional Information

Registration forms can be downloaded from the web at *http://www.ieee-cicc.org*. For additional information and general inquiries about the CICC, please contact the Conference Manager, Melissa Widerkehr, CICC: Tel: 301-527-0900, ext. 207 or email: cicc@his.com.

- Systems and architectures related to VLSI circuits
- Fundamentals related to the above subjects, including innovative circuits and device structures
- New System-On-A-Chip circuit applications such as MEMS

The emphasis is on circuit design. Papers are chosen on the basis of originality and quality. Although the circuits need not be implemented in a semiconductor chip, measured results, particularly for analog submissions, are key selection criteria. There will be four invited papers on emerging VLSI circuit technologies: on-chip interconnect, ultra-low-power LSI for mobile communications, biomedical implantable technology, and digital still camera technology.

Technical Highlights

This year we have assembled an array of interesting papers in areas that are at the forefront of integrated circuit design. Among the highlights of this conference are a 1-Megabit MRAM, which is the largest MRAM demonstrated to date, and a 3-GHz Pentium® 4 processor, which will feature the unprecedented scaling of a design from 1 GHz to 3 GHz.

Also featured in this conference are two different papers discussing, for the first time, their implementations of DDR II. Data rates as high as 1 Gb/s/pin are detailed in these flagship DRAM memory papers. In the area of ultra low power, one paper describes SOI circuit technology for batteryless mobile systems. A 0.5-V CPU is fabricated using a fully depleted SOI process. Another key innovation explores the novel concept of logic in memory by a ferroelectric functional pass gate. Active device counts are reduced significantly using ferroelectric technology to merge storage and switching functions. In the analog area a 17-mW transmitter and frequency synthesizer for 900-MHz GSM is reported. This work comprehends the importance of the transmitter in a cellular handset since it is often the overlooked component in considering the power dissipation of the overall system.

Invited Speakers

Invited papers are always a high point of the Symposium and focus on both technical information and business implications of technology change by leaders in their fields. At this year's plenary presentations Jim Meindl from Georgia Tech describes his work involving on-chip interconnects. Takakuni Douseki of NTT gives his vision of ultra-low-power LSI design for future mobile communication. Next, Professor Ken Wise of the University of Michigan reports on the progress in the field of biomedical implantable devices. Finally, Hiroshi Tamayama of Fuji Photo Film discusses digital still camera technology.

Rump Sessions

Evening rump sessions are organized around a controversial topic, and experts are recruited to present their divergent views. All aspects of the issue are explored, and a spirited discussion ensues; active audience participation is encouraged! This year the rump session topics for the Circuit Symposium are:

"Scaling limit in a power-limited environment—architecture versus circuit design," "Will high-performance analog survive in deep submicron CMOS?" and "Revolution or evolution for memory technology?"

A closer look at the rump session on "Scaling limit in a power-limited environment" gives a good idea of the opportunity provided for candid discussion in topics of interest to experts in this area. Today, power dissipation, both in the active and standby modes is becoming a key issue for desktop computers and mobile communication devices. This panel, organized by Ken Yang of UCLA and Tadahiro Kuroda of Keio University, features an array of panelists who are recognized experts in their particular field.

Scaling Limit in a Power Limited Environment

Panelists:

- Kerry Bernstein, IBM
- Uming Ko, TI
- Alireza Kaviani, Xilinx
- Chenming Hu, TSMC
- Kiyoo Ito, Hitachi
- Masayuki Mizuno, NEC

Overlap Day

Another special feature of these Symposia is the one-day overlap in the schedules for the Technology and Circuits meetings. This is an excellent opportunity to meet with members of the opposite discipline to share experiences, frustrations, and ideas for future improvements.

Background

Since 1987, the two Symposia on VLSI Technology and Circuits have provided opportunities for technology experts and circuit and system designers to interact with each other. From the beginning this has provided an intense but limited-size meeting place for international researchers and engineers to openly discuss and exchange new ideas and directions. The meeting locations alternate each year between sites in the US and in Japan. The VLSI Circuits Symposium sponsors continue to be the IEEE Solid-State Circuits Society and the Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information, and Communications Engineers of Japan.

About the Venue

The Hilton Hawaiian Village in Honolulu is a lush 22-acre resort on Waikiki's premier beach, conveniently located near Iolani Palace, Pearl Harbor, Waikiki Aquarium, Honolulu Zoo, and Bishop Museum. Guests can enjoy snorkeling, sailing, surfing, windsurfing, scuba diving, and more. Atlantis Submarines offers dives daily. Other amenities include exceptional dining at Bali-by-the-Sea, Golden Dragon and 13 other restaurants and lounges, plus a business center. The Rainbow Express Children's Program provides supervised activities for young people.

In addition to these chance meetings, there is also a joint rump session organized by members of both the Circuits and Technology committees. This year's topic is "SOC (System On A Chip) versus SIP (System In A Package)."

VLSI Circuits Short Course

Stephen Kosonocky of IBM and Koichiro Ishibashi of STARC have organized an excellent one-day Short Course on Wednesday, 12 June 2002. The topic is "Circuit and technology options for controlling leakage." The agenda includes talks by noted experts representing the entire spectrum of the industry:

- Introduction—Stephen Kosonocky, IBM T.J. Watson Research
- Device scaling, leakage components, joint technology and system optimization—David Frank, IBM T.J. Watson Research Center
- Overview of gate leakage and prospects of a technology solution—Toriumi, Tokyo University
- Optimization and control of VDD and Vth—Tadahiro Kuroda, Keio University
- Multi-Vt fully-depleted CMOS/SOI circuits for low-voltage design—J. Kouji, NTT
- Leakage-sensitive logic and circuits— Kaushik Roy, Purdue University
- Low standby power SRAM—Jae-Hoon Jang, Samsung
- Conclusion—Koichiro Ishibashi, STARC

This Short Course is an intense one-day course intended to give attendees an excellent overview of the topic as well as to provide the latest developments in the area. This represents a rare opportunity to hear presentations describing work in a timely technical area by recognized leading researchers teaching others to do what they do best.

Further Information

For registration and other information, visit the VLSI Symposia home page at: *www.vlsisymposium. org*. Or contact the Secretariats: USA Secretariat, vlsi2002@aol. com, Japan Secretariat, vlsisymp@ bacasj.or.jp

David B. Scott
Conference Chair
2002 Symposium on VLSI Circuits

david.scott@ti.com

Call for Nominees for SSCS Administrative Committee Election

In accordance with its Constitution, the IEEE Solid-State Circuits Society invites members of our Society to nominate candidates for the Society's Administrative Committee (AdCom). The election is held in the September-October time frame.

Nominees by Petition

Nominees will be placed automatically on the ballot provided:

- The nominee is presently a member of the IEEE Solid-State Circuits Society.
- The petition is supported by at least ten identifiable signatures of present members of the Society other than the nominee.
- The nominee is both aware of and agrees to the petition.
- The petition is received by the Chair of the Nominations Committee by 1 May 2002.

Terms of Office

- The term of office is three years beginning 1 January 2003.
- AdCom members may be reelected to a second consecutive term.
- The five nominees receiving the highest number of votes from the Society membership will be elected.

Scope and Responsibilities

Elected AdCom members are expected to attend the two yearly meetings of the AdCom. In addition, much of the Committee work is carried on by email, telephone, and fax throughout the year. The Solid-State Circuits Society currently sponsors *The Journal of Solid-State Circuits*, the International Solid-State Circuits Conference, the Custom Integrated Circuits Conference, the VLSI Circuits Symposium, and the Solid-State Circuits and Technology Committee's workshops. In addition, the Society cosponsors or technically cosponsors a number of other conferences and meetings.

The AdCom has responsibility for overseeing these and other potential future technical activities within the Society's field of interest, as well as the overall operation of the Society.

Mailing Petitions

All petitions should be accompanied by a personal photograph and a short biography (200 words or less), including the nominee's technical areas of interest. Petitions must be received by 1 May 2002. Petitions are to be mailed to:

IEEE SSCS Executive Office
445 Hoes Lane, Piscataway, NJ
08854-1331

Bruce Wooley
Nominating Committee Chair
IEEE Solid-State Circuits Society

wooley@ee. stanford.edu

Dynamic Chapters Chart New Programs

Ten SSCS chapters reported their activities at the annual SSCS Chapters' Luncheon on Wednesday, 6 February, the closing day of the ISSCC. Space prevents listing all the activities reported at the luncheon, but three themes are emerging in chapter management.

- Chapters are becoming more astute and better organized at tapping their own talent for their talks and programs, in addition to using the SSCS Distinguished Lecturers program.
- Chapter leaders are making efficient use of their time and meeting the needs of their members for technical information by cooperating with related IEEE chapters and other organizations in their region.
- New chapters continue to grow their own programs and serve an expanding membership.

Expanding Rosters of Feature Speakers

More chapters are organizing events that bring home the ISSCC by featuring ISSCC presenters from their own section. Japan has a long tradition of this, gearing its presentations for an audience of students and young engineers. Quitang Huang reported that in March the Zurich Chapter meeting featured an agenda of Swiss contributors to the ISSCC. The Zurich Chapter also scheduled a workshop last fall that drew 50 attendees from all over Europe. Other events for 2002 are listed in the table of Distinguished Lectures on page 7.

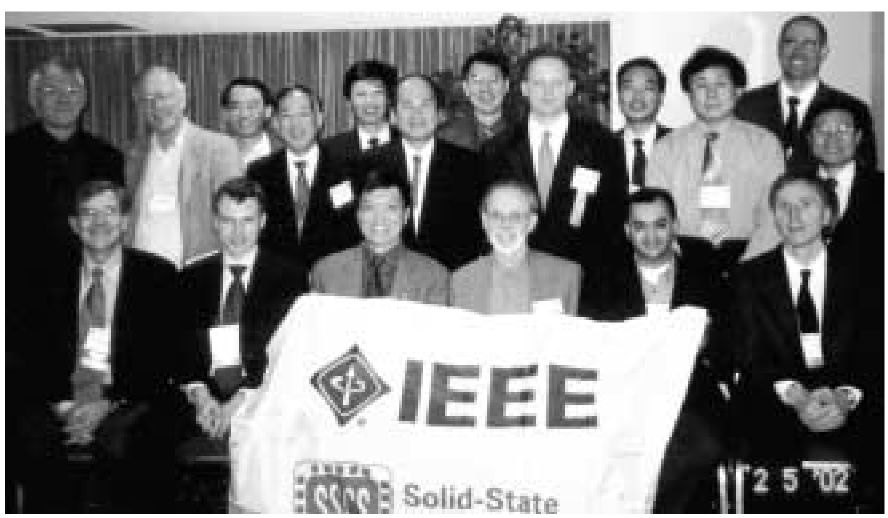
Jieh-Tsorng Wu, Chair of the Taipei Chapter, reported that the Taipei Chapter is creating its own speaker list to promote information exchange and research cooperation within the Taiwan IC design community and to augment their two annual presentations by Society Distinguished Lecturers. This ensures their full recognition and use of the world-class talent in their midst. The lecture at their first meeting was given by Chin-Chieih Chao of Century Semiconductor, who spoke about floating-point multiplier design for a 64-b microprocessor and delayed-reset logic family.

Last year the Taipei Chapter organized four Short Courses. The two in April and May were held at the National Chiao-Tung University in Hsin-Chu and drew 250 attendees each: "Network processing ICs" by C. Bernard Shung of Broadcom Corp. U.S.A. and "Design and simulation of RF and analog ICs" by Georges G.E. Gielen of Katholieke Universiteit Leuven, Belgium. Two in August were held alongside the VLSI Design/CAD Symposium and were co-sponsored by the Chapter with the National Chiao-Tung University, drawing 120 attendees each: "VLSI DSP for broadband communications" by Meng-Lin Yu of Agere and "RFIC design for wireless communications" by Jen-Shan Lin of Agere.

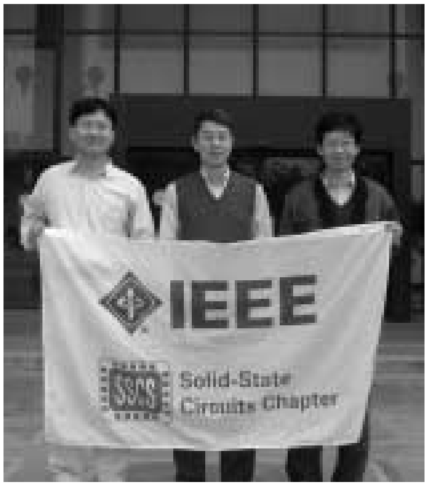
The Taipei Chapter currently is preparing to host the 2002 Asian-Pacific ASIC Conference, 6–8 August at the Grand Hotel, Taipei, Taiwan. Paper selection gets underway this April.

Zhihua Wang of Tsinghue University, Chair of the Beijing Chapter, reported on a June 2001 seminar conducted by Nobel Laureate Jack Kilby on the history of the integrated circuit. About 100 students from the Bejing area attended. In September the Chapter hosted a People-to-People Delegation of 40 experts organized by the IEEE Electron Device Society. During the 11-day visit Albert Wang of the Illinois Institute of Technology and an SSCS Distinguished Lecturer conducted the seminar "On-chip ESD protection design for integrated circuits." In November Kaushik Roy of Purdue University conducted the seminar "Deep submicron leakage: Future trends and possible solutions."

The Chapter is also working with the Bejing Municipality and the Bejing Semiconductor Industry Asso-



Attendees at the 2002 SSCS Chapters lunch with the new SSCS chapter banner (l-r): rear row; Voijin G. Oklobdzija (Oakland/ East Bay Chapter), Lee Colby (Santa Clara Valley Chapter), Jerry Lin (Dallas Chapter), Toshiaki Masuhara (Chapters Committee), Shyh-Jye Jou (Taipei Chapter), Masao Nakaya (Kansai Japan Chapter), Jieh-Tsorng Wu (Taipei Chapter), Anas Mahoui (Toronto Canada Chapter), Akira Matsuzawa (Kansai Japan Chapter), Zhihua Wang, (Beijing Chapter), Christian Enz, (West Switzerland Chapter), Kwang Yoon (Seoul Chapter).
Seated: Jan Van der Spiegel (Chair, SSSC Chapters Committee), David Robertson (Boston Chapter), Quiting Huang (Zurich Chapter), Christer Svensson (Chair, Distinguished Lectures Program), S. Reedhar Natarajan (Dallas Chapter), David Johns (Chapters Committee). Absent for the photo: Cary Yang (Director, IEEE BoD Division 1), Moon Key Lee, (Seoul Chapter), Jonathan David (SSCS Membership Chair), Anne O'Neill (SSCS Executive Director), and Raf Roovers (Benelux Chapter).



Taipei Chapter with new banner. From left to right: Professor Wei-Zen Chen (Treasurer), Professor Jieh-Tsorng Wu (Chair), and Professor Shyh-Jye Jou (Secretary). SSCS chapters who have not received their banner are urged to contact the SSCS Executive Office: l.barankovich@ieee.org.

ciation (BSIA) on an Integrated Circuit Design Training Center for industries in the area. It will open 12 April 2002. The IEEE/SSCS Bejing Chapter will be in charge of inviting international experts to train local engineers at the center in the coming few years.

The Bejing Chapter is preparing to sponsor the Asia-Pacific ASIC Conference in 2004 and has begun seeking cooperation with five other local and national associations in addition to the IEEE regional chapters, the Bejing section and Tsinghue University.

Look for details of these upcoming SSCS Lectures at www.sscs.org/chapters

Month	Distinguished Lecturer	Chapter
April	Rinaldo Castello	Zurich, Switzerland
May	Jan Van der Spiegel	Nis, Yugoslavia
July	Jan Van der Spiegel	Porto Allegre, Brazil
September	Asad Abidi	Zurich, Switzerland

Working with Other Chapters

More Chapters are taking advantage of the efficiencies of cooperating with related chapters in their own section, other SSCS chapters in neighboring sections, and similar national professional associations. This maximizes the exposure of a speaker and the efficiencies of local volunteer leaders organizing meetings that attract local engineers. The Dallas SSCS Chapter, which has featured many SSCS Distinguished Lectures in its first three years of operation, is now cooperating with the Circuits and Systems Chapter in arranging for speakers and in planning the CAS fourth annual spring workshop and poster session. Ana Hamoui reported that the Toronto Chapter has featured local industry experts but is also interested in expanding its use of the Distinguished Lecturers program. They cite the advantages of combining with related societies to stretch both funds and volunteers' time.

Christian Enz reported that the West Switzerland Chapter is looking forward to working with the French Chapter in Grenoble. Last fall West Switzerland organized a workshop in wireless networks and plans another this coming June after ADAC.

David Robertson, reporting for Boston's Chair Bruce Hecht, mentioned that all of Boston's four programs were conducted jointly with another chapter, including MTT, EDS, LEOS, Control Systems, and ACM. They were: "Overview of DARPA microelectronic and photonics initiatives" by Bob Leheny of Microsystems Technology Office of DARPA, "Wireless system considerations in RFIC design" by Steve Lurggiel of Maxim, "Advances in semiconductor device modeling" by Steve Broadbent of Silvaco International, and "Applications, design, and development of biochips" by Manish Deshpande of Coventor. A 2002 goal for the Boston Chapter is organizing a Short Course.

Lee Colby reported that the original SSCS Chapter in the Santa Clara Valley now has 1,400 members and holds nine meetings a year. They are looking forward to a section-sponsored training workshop on chapter management in February 2002. Classes will feature tips and traps for chairs, treasurers, running Web sites, setting up email aliases, and officer training.

Growth in New Chapters

Masao Nakaya reported that the year-old Kansai Chapter has shown an almost 12% increase in SSCS membership, from 138 when it was formed last January to 156 this year. The Chapter covers the region west of Tokyo encompassing three major urban areas: Kyoto, Osaka, and Kobe. Program activities this year have been held in three cities at four different sites. A meeting at Kyoto Research Park last June drew 120 attendees and featured the following lectures: "Linearity, time-variation, phase modulation and oscillator noise" by T. H. Lee of Stanford University and "Mixed-signal LSI technology" by A. Matsuzawa of Matsushita Electric Industrial. A fall lecture meeting at Campus Plaza Kyoto drew 75 attendees and featured: "Design and other ITRS technologies: Sharing brick walls" by A. B. Kahng of University of California at San Diego and "An introduction to circuit design without SPICE" by T. Wada of the University of the Ryukyus. Other activities this fall were cosponsored with the IEICE /ICD of Japan and included a two-day September study meeting at Kobe University and a three-day workshop at Kitakyusyu.

The new IEEE Bangalore EDS/SSCS Chapter was approved officially by the IEEE in October 2001. Navakanta Bhat of the Indian

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SSCS Members Honored as 2002 IEEE Fellows

An IEEE Fellow is a member of unusual distinction in the profession. It is a recognition conferred only by invitation of the Board of Directors upon a person of outstanding and extraordinary qualifications and experience in IEEE designated fields, who has made important individual contributions to one or more of these fields. A nominee must be a Senior Member of the Institute and must have been a member in any grade for at least five years prior to the year of election.

A nomination for Fellow must be accompanied by references from at least five current IEEE Fellows. No more than one-tenth of one percent of the total Institute membership may be advanced to Fellow grade in any given year. Each nomination is evaluated by the relevant technical society or council and is ranked by the 26-member Fellows Committee. Multiple reviewers produce a composite viewpoint that is used in recommending to the Board of Directors suitable candidates for election to Fellow grade.

The IEEE conferred the distinction of Fellow on 259 of its members of the class of 2002. Here are six of sixteen new Fellows who are members of the Solid-State Circuits Society. These new Fellows were evaluated by the SSCS and recognized at the ISSCC 4 February. The remaining ten members will be introduced in our July issue.

Dr. James W. Haslett
University of Calgary, Calgary, Canada

For contributions to high-temperature instrumentation and noise in solid-state electronics

James W. Haslett received his BSc in electrical engineering from the University of Saskatchewan, Saskatoon, in 1966, and his MSc and PhD from the University of Calgary in 1968 and 1970, respectively.

He then joined the Department of Electrical Engineering, University of Calgary, where he is currently a professor. He was head of the department from 1986 to 1997, and has been president of his own consulting firm since 1981, consulting to oil-field instrumentation firms primarily on high-temperature downhole instrumentation with Dr. Fred Trofimenkoff, also in the Department of Electrical and Computer Engineering at Calgary. He was also a member of several national and international science teams designing satellite instrumentation in the late 1970s and 1980s. Dr. Haslett joined the TRLabs Industrial Research Consortium in 1997, first as an adjunct professor and more recently as an affiliate professor.

His current research interests include analog and digital VLSI design, noise in semiconductor devices, high-temperature electronics for instrumentation applications, solid-state imagers for scientific applications, biomedical microsystems and nanosystms, and RF microelectronics for telecommunications. Dr. Haslett has won twelve teaching awards in the past nine years, including the University of Calgary President's Circle Award for Teaching Excellence in 2001.

Dr. Haslett is a member of the Association of Professional Engineers, Geologists and Geophysicists of Alberta, the Canadian Astronomical Society, the Canadian Society of Exploration Geophysicists, and the American Society for Engineering Education. He is currently a member of the Editorial Board of the IEEE Transactions on Instrumentation and Measurement. He is a Fellow of the Engineering Institute of Canada, and a Fellow of IEEE.

Dr. Qiuting Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

For contributions to integrated circuits for wireless communications

Qiuting Huang's primary and secondary education was severely disrupted by the Cultural Revolution, a period of social and political instability in China between the mid-sixties and the mid-seventies. He spent four years after high school working at various odd jobs, from a shop assistant to a high school physics teacher to a factory mechanic, before winning an opportunity in 1978 to receive the university education that had become available again. He graduated four years later from the Harbin Institute of Technology. Subsequently he won a government scholarship to pursue his doctoral studies in analog integrated-circuit design under Professor W. Sansen at the Katholieke Universiteit, Leuven, Belgium, where he received his PhD in 1987. Between 1987 and 1992 he worked as a lecturer at the University of East Anglia, UK. He joined the Swiss Federal Institute of Technology in Zurich in 1993 and was later elected Professor of Electronics.

Dr. Huang's current research focuses on integrated circuit design for communications. He and his graduate students have developed complete RF receivers and transceivers for applications such as paging, GPS, GSM, and UMTS, with particular emphasis on low-power design. He has collaborated extensively with many leading IC companies on projects ranging from data converters, sensor interface, and medical electronics to high-speed digital and smart-power circuits. He currently serves on the technical program committees of both ISSCC and ESSCIRC. He is the Chair of the Zurich Chapter of the IEEE Solid-State Circuits Society and was a guest editor of the IEEE Journal of Solid-State Circuits.

Dr. Akira Matsuzawa
Matsushita Electric Industrial Co., Ltd., Osaka, Japan

For contributions to high-speed A/D converters and mixed-signal integrated circuits

Akira Matsuzawa received his BS and MS in electronics engineering from Tohoku University, Sendai, Japan, in 1976 and 1978. He received his PhD in 1997 from the same university in high-precision and ultra-high-speed A/D converters. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and mixed signal LSI technology, ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, digital read-channel technology for DVD systems, ultra-high-speed interface technologies for metal and optical fibers, testing, boundary scan technology, and CAD technology. He also is responsible for the development of low-power LSI technology, ASIC libraries, analog CMOS devices, SOI devices and circuits, and the specification of advanced CMOS devices.

Currently Dr. Matsuzawa is a general manager in the advanced LSI technology development center and is a part-time teacher at Osaka University and Tohoku University. He served as guest editor-in-chief twice for special issues on analog LSI technology of the IEICE Transactions on Electronics in 1992 and 1997, vice-program Chair for the International Conference on Solid-State Devices and Materials (SSDM) in 1999 and 2000, and was co-Chair of the Low-Power Electronics Workshop in 1995. Dr. Matsuzawa serves on the program committee for analog technology at ISSCC and as guest editor for special issues of the IEEE Transactions on Electron Devices. He has published 17 technical journal papers and 35 international conference papers, and is co-author of eight books. He holds 34 registered Japan patents and 65 U.S. and EPC patents. He has received the R&D100 award.

Dr. Krishnaswamy Nagaraj
Texas Instruments, Warren, NJ

For contributions to the design of CMOS data converters

Krishnaswamy Nagaraj obtained his BE in electronics from Bangalore University in 1972 and his ME and PhD, both in electrical communication engineering, from the Indian Institute of Science, Bangalore, in 1974 and 1983, respectively. From 1974 to 1984 he was with the R&D laboratories of the Indian Telephone Industries, Bangalore, where he was engaged in the design of telecommunication systems and integrated circuits. During 1985 and 1986 he was with the VLSI group at the University of Waterloo, Canada, engaged in research and teaching in analog and digital circuits. His research at Waterloo focused on techniques for overcoming non-ideal effects in switched-capacitor circuits. From 1986 to 1996 he was with Bell Laboratories in Murray Hill, NJ, and Allentown, PA, where he worked in the design of mixed-signal integrated circuits for telecommunications, mass storage, and digital signal processing. He received the Distinguished Member of Technical Staff Award from Bell Laboratories in 1991. Since 1996 he has been with Texas Instruments in Warren, NJ, where he is presently a Distinguished Member of the Technical Staff. From 1996 to 2000 he led the development of high-speed CMOS data converters for mass storage, video, and broadband communications. He presently is leading the design of mixed-signal circuits for the wireless infrastructure.

Dr. Nagaraj was an associate editor of the IEEE Transactions on Circuits and Systems, Part II, from 1993 to 1995. He is presently an associate editor of the IEEE Journal of Solid-State Circuits and a member of the ISSCC technical program committee. He is also an adjunct associate professor of electrical engineering at the University of Pennsylvania, Philadelphia.

Dr. Carl Matthew Sechen
University of Washington, Seattle, WA

For contributions to automated placement and routing in integrated circuits

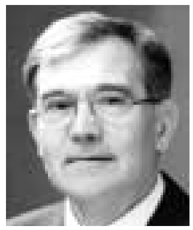
Carl Sechen received his BSEE from the University of Minnesota, an MS from M.I.T., and a PhD from UC Berkeley. Starting in 1986, he was an assistant and then associate professor in the Department of Electrical Engineering at Yale University. In 1992 he moved to the University of Washington, where he is now a professor in the Department of Electrical Engineering. He is a co-director of the National Science Foundation's Center for the Design of Analog and Digital Integrated Circuits (CDADIC).

Dr. Sechen received the Semiconductor Research Corporation's "1994 SRC Technical Excellence Award" and the "1988 SRC Inventor's Award." He received the "SRC Inventor's Recognition Award" in 2001 for his development of output prediction logic. He was a member of the technical program committee for the IEEE International Conference on Computer-Aided Design (ICCAD) from 1989 to 1993. From 1998 to 2001 he was Chair of the placement and floor-planning technical program sub-committee for ICCAD.

Dr. Sechen developed the first version of the TimberWolf placement and routing package in 1983. Versions of TimberWolf that Dr. Sechen developed at UC Berkeley, Yale University, and the University of Washington were used in production at Intel, Digital Equipment, National Semiconductor, Crystal Semiconductor, Advanced Micro Devices, and Motorola from the mid-eighties to the mid-nineties. TimberWolf was used at more than 20 companies and more than 25 universities.

In his 15 years as a professor, Dr. Sechen has graduated 16 PhD students. He has authored one book, and authored or co-authored over 120 research papers. He is a co-founder of InternetCAD.com, Inc., a placement and routing tool vendor. His current research interests are primarily in ultra-high-speed and low-power digital integrated-circuit design.

Dr. Jan Van der Spiegel
University of Pennsylvania, Philadelphia, PA



For contributions in biologically motivated sensors and information processing systems

Jan Van der Spiegel is a professor of electrical engineering and director of the Center for Sensor Technologies at the University of Pennsylvania. He has been Chair of the Department of Electrical Engineering since 1998. Dr. Van der Spiegel received his MS in Electro-Mechanical Engineering and his PhD in Electrical Engineering from the Katholieke Universiteit, Leuven, Belgium, in 1974 and 1979, respectively. His primary research interests are in high-speed, low-power analog and mixed-mode VLSI design, biologically based sensors and sensory information processing systems, micro-sensor technology, and analog-to-digital converters. He has authored over 160 journal and conference papers and is the holds four patents.

Dr. Van der Spiegel is the recipient of the IEEE Third Millennium Medal and has served on several IEEE program committees. He is currently a member of the executive and program committees of the ISSCC. He has been the Chapter Chairs coordinator of the Solid-State Circuits Society since its formation. He is also editor of Sensors and Actuators A for North and South America and is on the editorial board of the Journal of the Brazilian Microelectronics Society.

Dr. Van der Spiegel is the recipient of the UPS Foundation Distinguished Education Chair and has also received the Bicentennial Class of 1940 Term Chair, the Christian and Mary Lindback Foundation Award for Distinguished Teaching, the S. Reid Warren Award for Distinguished Teaching, and the Presidential Young Investigator Award.

Dynamic Chapters Chart New Programs

continued

Institute of Science and joint Chapter Chair sent in the following report.

There are more than 40 engineering colleges in Bangalore and several multinational companies actively involved in VLSI circuit design. Three events were held in December that covered the entire spectrum from systems to materials: "Design technology and architectural adaptation for deep sub-micron VLSI systems" by Rajesh Gupta of the University of California, Irvine; "Failure analysis challenges in deep sub-micron devices" by Dr. Radhakrishnan of Philips Electronics, Singapore; and "Development and characterization of low dielectric constant materials for CMOS and other micro-electronic device applications" by Professor Gautam Sarkar of the University of Alaska. This range of topics addressed the diverse interests of the members of EDS and SSCS.

In August 2002 the Bangalore Chapter will cooperate with the VLSI Society of India to organize the three-day VLSI Design and Test Workshops. Attended by professionals both from industry and academia, the VLSI Society provides fellowships to participating academics. During 2002, the Chapter also plans to organize a one-day workshop for undergraduate and graduate students on future challenges in VLSI technology.

RFIC Symposium, Seattle, Washington, 2–4 June 2002

The RFIC Symposium is a leading international conference dedicated to the advancement of integrated radio frequency circuits and subsystems for RF and communication applications. The RFIC Symposium program starts with tutorials and workshops held on Sunday. The technical program takes place on Monday and Tuesday and includes technical papers, a panel session, and a number of invited and special sessions related to the latest advancements in RFIC.

The technical program starts off on Monday morning with a keynote plenary session. The first keynote talk, "Challenges for the next generation of RF integration," will be presented by Behrooz Abdi of Motorola Inc. Mr. Abdi is the vice president and general manager of the Radio Products Division within the Semiconductor Products Sector responsible for RF & mixed-signal ICs and modules for wireless applications. The second keynote talk, "RF design, a historical perspective," will be given by Dr. Ulrich Rohde. Dr. Rohde is president of Communications Consulting Corporation and executive vice president of Strategic Planning at Ansoft Corporation.

A panel session on "RF-CMOS in cell phones: fact or fiction" is scheduled Monday, 3 June, 12:00–1:15 PM. The panelists, representing various industries and academia will discuss their views on the future of high-performance RF-CMOS for mobile handsets. The panel organizers, Natalino Camilleri and Fazal Ali, comment "RF-CMOS development has come a long way towards being implemented in several systems for multiple applications. One can find RF-CMOS in some cordless devices, WLAN and Bluetooth products. However, in cellular handset systems, RF-CMOS has had a difficult time competing with the SiGe BiCMOS technology in offering the "best in class" RF performance while maintaining the lowest power consumption."

The RFIC social reception will be held on Sunday evening and the *Microwave Journal*/MTT-S reception on Monday evening. The Interactive Forum will meet Tuesday, 4 June,1:20–5:00 PM.

Session Descriptions

Monday, 3 June, 10:10–11:50 AM

Cellular Transceivers

This session focuses on state-of-the-art 2G and 3G transmit and receive IC design techniques. Highly integrated direct-conversion receivers for GSM and WCDMA are discussed in detail. High dynamic range, high-precision, high-efficiency CDMA transmit circuits are also presented.

Efficiency Enhancement Techniques for Handset Applications

This session covers different techniques for improving power amplifier efficiency. Enhancement techniques include variable bias, variable load impedance, envelope tracking/following, and digital predistortion. Detailed design, analysis, and results of high-performance Class E amplifiers are addressed.

Integrated VCO

This session presents the latest advances in integrated voltage-controlled oscillators. Various design techniques for improving VCO performances including phase noise, frequency tuning range, and power consumption are reported. The quadrature generation of VCO for direct-conversion transceivers is discussed in three papers.

Optical System ICs

The session opens with an invited paper from Intel that walks the audience through the ins and outs of circuit design for optical systems. It focuses on 10-Gb/s applications as well as on the challenges that the next generation 40-Gb/s optical systems will face. The next paper highlights the design of one of the indispensable components for high-speed systems: a 37–50-GHz VCO for 40-Gb/s applications. The next two papers discuss the design of other components for 10-Gb/s optical systems: first, a 12-channel amplifier array with low cross-talk is demonstrated; then, a low-cost front-end chipset is described and implemented in Si CMOS technology. The session concludes with a presentation on co-simulation of layout and circuit design in order to shorten the design cycle.

Wireless Data System ICs

This session covers a wide range of applications and highly integrated transceivers. An invited paper on 802.11b WLAN technology contrasts a 0.25-µm full CMOS solution with a 0.5-µm SiGe design. Additional papers demonstrate state-of-the-art tech-

Continued on next page

Sunday Tutorials and Workshops

Tutorials and workshops are scheduled all day Sunday, 2 June, 8:00 AM–5:00 PM

The three tutorial topics are:

- RF Fundamentals
- MEMS Technology for Highly Integrated RF Systems
- EM Simulators–Theory and Practice

Seven workshops are scheduled:

- Developments in Integrated Circuits for Communications at 40 Gb/s and Beyond
- Direct Conversion Transceivers for Cellular and Wireless Applications
- RF and High-speed Flip Chip Technology and Design
- Advances in Bluetooth Technology
- Wireless Systems On a Chip
- RF Solutions for GPS-to-handset Applications
- Intelligent RF Front-ends

niques for Bluetooth, GPS, cordless, and broadband cable modem systems.

Monday, 3 June, 1:20–3:00 PM

LNAs, Mixers and Switches

The papers in this session focus on new developments in key RFIC building blocks for modern cellular systems and span SiGe BiCMOS, BiCMOS, and GaAs technologies. Advances in automatic RF circuit synthesis, high-performance CDMA receiver front-end design, direct conversion WCDMA front-end design, dual-band variable gain mixers, and low-voltage high-power GSM switch design are presented.

High-Frequency Receiver and Converter Technology

This session addresses signal-conversion ICs operating from 2 through 33 GHz using pHEMT and SiGe HBT technologies. The first paper presents a 2–18-GHz high-dynamic range receiver IC utilizing a commercial GaAs pHEMT process. The second paper addresses a 3–33-GHz mixer using distributed topology implemented in pHEMT technology. A Ka-band direct digital receiver IC is reviewed in the third paper. A highly integrated 24-GHz reciever IC utilizing SiGe HBT technology is discussed in the final paper.

PLL and Frequency Synthesizer

This session covers the design techniques for high-speed phase-locked loops in radio frequency synthesizers. Design considerations such as power consumption, jitter, dual band, and high-frequency time delay are reported.

Monday, 3 June, 3:30–5:10 PM

3G Cellular Systems and Chipsets

This session covers both system-level issues and chipsets for 3G CDMA and WCDMA. Multifunction system architectures, digital and RF integration issues, and optimized chipsets are presented. The session concludes with a discussion on 4G technology and architecture challenges.

Low-Noise Amplifiers

Recent advances in fixed- and variable-gain LNAs are discussed in this session. Highlights include a 1-V 8-GHz CMOS variable-gain LNA, 2- and 5-GHz LNAs with gain steps, as well as SiGe BiCMOS and CMOS 5–6 GHz LNAs for WLAN.

Very High Speed Si and SiGe Divider ICs

This session presents divider ICs operating from 14 through 36 GHz implemented in Si and SiGe technology. The first paper reviews a dual-modulus 14.5-GHz divider utilizing Si technology. Next, a 19-GHz static divider in CMOS is presented. A low-power 20-GHz static divider is reviewed, which has been implemented in Si. Finally, a SiGe implementation of a dual-modulus prescaler operating at 36 GHz is discussed.

Power Amplifiers for Handset Applications

This session shows the latest power-amplifier performance for GSM/EDGE and WCDMA applications. Many performances were improved through better bias networks and/or active pre-distortion. Also, an improved CMOS integrated distributed amplifier is addressed.

Tuesday, 4 June, 10:10–11:50 AM

Radio Frequency Integrated Circuits for 3G

This session deals with RFIC and system aspects for third-generation mobile terminals and base stations. Two invited papers demonstrate the first implementations of an integrated even-harmonic-type direct-conversion receiver and of a zero-IF receiver chip for wideband CDMA. Furthermore, a CMOS transceiver chipset and system analysis of base station power amplifiers are presented.

MMIC Technology

The papers in this session address Si, GaAs, and InP MMIC technologies, which enable innovative wireless and microwave applications. New advances in process development of silicon technologies are enabling reduced electromagnetic coupling effects in RFCMOS, the integration of SCR-based ESD protection circuits into RFCMOS, and the novel integration of a short-channel LDMOS technology that is BiCMOS compatible. These developments point to the potential in low-cost RFICs using standard Si processes. In the area of III-V devices, new developments allow the integration of analog and digital functions in an E/D pHEMT process and the demonstration of an InP HEMT-based VCO with heterojunction interband tunnel diode. Finally, a Ka-band MMIC LNA/PA chipset is reported as packaged in a low-cost SMT-compatible technology.

Tuesday, 4 June, 1:20–3:00 PM

Silicon Substrate and Inductor Modeling

Continued advances in developing Si RFIC components require careful consideration of losses in passive components and losses associated with the Si substrate. This session focuses on developments in modeling inductors fabricated on Si substrates. In addition, the influence of conductive substrates on active device behavior is discussed.

SiGe RFIC Process Technologies

RFIC applications now address wireless data as well as mobile communications and broadband tuner applications. The SiGe process is ideal for meeting the needs of these high-frequency applications and is the focus of this session. Several leading companies present their process technologies with respect to RF performance of both passive and active components.

Tuesday, 4 June, 1:20–3:00 PM

Active Device Modeling and Characterization

Development of RFIC components requires precise modeling of active device behavior, including large signal, small signal, and noise effects. This session focuses on developments in the active device modeling occuring in these areas.

RFIC Power Amplifier Technologies

This session focuses on power amplifier technologies and often overlooked RFIC issues such as packaging and passive components. An overview of power amplifier technologies is presented and relevant results in both SiGe and GaAs technologies are discussed.

Program, Keynotes, Exhibitors, and Location Designed to Make the 39th DAC Hotter than Hot!

This year's Design Automation Conference—now celebrating its 39th year—returns to New Orleans, LA, 10–14 June. The combination of a strong technical program with an extensive exhibitor showplace and, this year, a "hotter than hot" location makes it a conference not to be missed.

DAC is the conference that helped launch an industry. Since its inception, it has offered designers the opportunity to discover the best in new technology and new products while meeting with the best people in the industry—all in one place. It is a comprehensive forum for continuing education, networking, and information exchange. It gives designers one place to research new products or identify ones that will help with that new design. Breakthroughs in electronic design automation (EDA) research are presented in the technical program. And, many a successful EDA company have been launched at DAC.

This year's conference is no exception. It boasts more than 250 exhibits hosted by EDA, semiconductor and embedded device vendors, and more than 100 demo suites for private, personalized product demonstrations. DAC pioneered the use of demo suites—a concept now widely imitated throughout the trade show industry.

The technical program exposes attendees to new developments in design methodologies and design tools. This year's program includes 160 technical papers, culled from a record number of submissions, covering a wide range of topics, both practical and theoretical, affecting electronics designers and computer-aided design (CAD) developers. The program, now being finalized, tackles new developments in the design flow, from high-level specification, simulation and verification, to synthesis, place-and-route, and testing. System-On-a-Chip (SOC) design and test, as well as embedded system design are key topics. Low power design, particularly in large embedded system designs, also features prominently in the technical program.

The conference includes eight panels where individuals with differing points of view argue their positions. Attendees will hear discussions ranging from Wall Street's view of EDA moderated by the CEO of Synopsys, to challenges in nanometer design, formal verification, and ASIC signoff. One panel, sure to be controversial, will debate which is the bigger bottleneck: tools or users. Another will try to determine the next growth area in the electronics industry and, hence, the next EDA driver. Attendees interested in analog design can help panelists decide if re-usable analog intellectual property will ever be a reality.

Hands-on tutorials are a new feature of DAC this year. They will give attendees an opportunity to learn new products in an informal and casual setting. Of course, DAC's regular tutorial program, held Friday,

Continued on next page

Congratulations to New Senior Members

Anton Bakker	Meikei Ieong
John O. Borland	Aniruddha Joshi
Bernhard Boser	Norman P. Jouppi
Degang Chen	James Kemerling
Eric Y. Chou	Gary Kaatz
Lawrence T. Clark	Donald Y. C. Lie
Jose Diaz	Youn Long S. Lin
Ertugrul Demircan	Charles F. McConaghy
Rolf Ernst	Clark T.C. Nguyen
Minoru Fujita	Priyavadan R. Patel
Wanda Gass	Betty Prince
Tito Gelsomini	Raminderpal Singh
Douglas Greenway	Bruce M. Thompson
Yuriy M. Greshishchev	Nishath K. Verghese
Masachika Harada	David J. Walkey
James B. Hecht	Chorng-Kuang Wang
Wenkang Huang	Todd R. Weatherford

Program, Keynotes, Exhibitors *continued*

offers up to six full-day tutorials on core EDA topics such as design verification, hardware description languages, low-power design, and deep sub-micron design issues.

The Tuesday keynote address will be given by Dr. Hajime Sasaki, chair of the NEC Corporation, who will discuss new challenges faced by the CAD industry in light of changes that are occurring in the way we design chips. Jerry Fiddler, chair and co-founder of Wind River Systems, will deliver the Thursday keynote. He will explore ways in which we might bring the embedded software design industry and the hardware EDA industry together to more seamlessly design complex systems on a chip.

Chris King, chief executive officer (CEO) of AMI Semiconductor and the first woman to lead a semiconductor company, will deliver the keynote at the Workshop for Women in Design Automation (WWINDA). The yearly workshop is scheduled for Monday, 10 June, from 1:15 p.m.– 4 p.m. Now in its fifth year, the workshop offers individuals who work in the design automation industry the opportunity to hear successful women speak on topics relevant to their careers. The winner of the Marie R. Pistilli Women in EDA Achievement Award, presented annually to the individual who has visibly helped advance women, will also be awarded during the workshop.

There's also a new DAC pavilion on the exhibit floor, offering mini-panel sessions, interviews and video feed from key technical presentations. This year's conference again will feature the Embedded Systems Showcase. In addition, the Student Design Contest award winners will be announced at DAC. This year's entries come from a range of international and U.S. participants. Entry topics range from digital signal processing to wearable computing systems to DNA sequence matching.

Early registration for IEEE or ACM members is $270 and is $335 for non-members. This includes a three-day conference pass for the technical program and exhibits, conference proceedings and refreshments. Pricing for tutorials and workshops is found on the DAC Web site, as is online registration. The DAC Web site is located at www.dac.com.

In this time of uncertainty in our industry, it has never been more important to stay informed and aware of emerging trends. One of the best ways to achieve this is through attendance at technical conferences such as DAC. More than 15,000 CAD developers, researchers, managers, and engineers attend from leading electronics companies, universities, and the EDA industry. New products are introduced, research is described and successful design methods are highlighted. For anyone in electronics design or EDA, it's an event not to be missed. I look forward to seeing you there.

Nanette V. Collins
Publicity Chair
39th DAC
nanette@nvc.com

Free How-To Guide for Course Design Available

Available free from the Educational Activities Board (EAB) is the *Telcordia Technologies' Reference Guide for Instructional Design and Development*. This online-only, how-to guide teaches efficient and effective course and tutorial design. The guide explains how to add educational value to your tutorials and courses, which can qualify them for Continuing Education Units.

Based on the Systematic Design of Instruction by Walter Dick and Lou Chaney, the guide outlines six distinct steps to acquire sound design principles. These clear steps, displayed on colorful, easily navigated Web pages show how to:

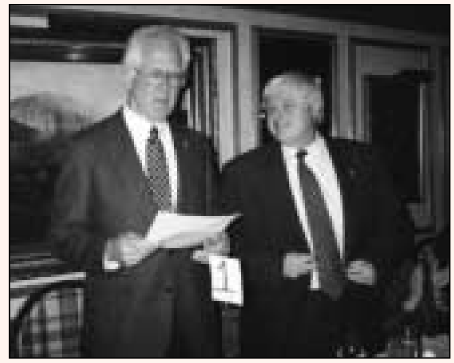
- Assess the needs of the instructional situation
- Analyze the learners
- Write learning objectives
- Select an instructional strategy that fits your assessment
- Develop materials that enhance your strategy
- Evaluate your work

With each step there is a concise concept outline, tools to aid in the application of the steps, and online references that can add to the material in the outline. Access this guide at *www.ieee.org/organizations/eab/tutorials/refguide/mms01.htm.*

Lynn Murison
Outreach Administrator
IEEE Educational Activities
L.murison@ieee.org

SSCS Members Recognized by IEEE Education Activities Board

Two SSCS members have been honored with 2001 IEEE EAB Meritorious Service Citations. Kenneth R. Laker and Jerry R. Yeargan were cited for "for outstanding and sustained service to the aims and objectives of the Educational Activities Board." This citation was established in 1988 by the IEEE EAB to provide an opportunity for colleagues to recognize dedicated, reliable, and consistent service to the various goals of the EAB.



IEEE Educational Activities vice president Lyle Feisel presented the citation to Dr. Laker at the IEEE EAB Planning Meeting held on 25 January in Newark, NJ.

Kenneth R. Laker

"The greatest value that IEEE membership can return to members and their employers is career vitality," said Dr. Laker. "In accepting this award, I do so on behalf of the numerous IEEE volunteers who contribute their time and effort to this vitally important cause."

Dr. Laker, 1999 IEEE president, served as Educational Activities Board vice president 1994–1995. During his tenure he increased the EAB pre-college and continuing education projects. He conducted the first IEEE workshop to address the technical vitality needs of employers and employees. The 1994 Industry 2000 Workshop set the agenda for much of the EAB program for 1994 and 1995. He set the model for partnerships with other Societies and organizations, the use of grants in support of EAB special projects, and the expansion of global outreach activities.

While IEEE president, he established the $10,000 IEEE Presidents' Scholarship for the Intel International Science and Engineering Fair (ISEF) at the 50th anniversary of the Intel ISEF. The scholarship goes to a high school student whose project demonstrates "outstanding achievement in research and presentation of engineering knowledge in electrical engineering, information technology, or other IEEE fields of interest." The scholarship is now funded by the IEEE Foundation.

Dr. Laker is currently Alfred Fitler Moore Professor of Electrical Engineering at the University of Pennsylvania and a member of the Advisory Board of PMC-Sierra Allentown, PA, subsidiary. He serves as Chair of the Trustees for the IEEE History Center and Chair of the IEEE Virtual Museum Oversight Committee. He received his PhD from New York University.

Jerry R. Yeargan

For nearly a decade, Dr. Yeargan has served and chaired a variety of IEEE EAB councils and committees. Whether outreach, nominations, planning, review, pre-college, or awards, or as an IEEE/Accreditation Board for Engineering and Technology (ABET) program evaluator, Dr. Yeargan has been unstinting with his time and attention. While serving as IEEE EAB vice president from 1996–97, he initiated the EAB pre-college program and established its Oversight Committee.

Dr. Yeargan has been a leader in the global expansion of university engineering program accreditation. Accreditation identifies engineering and computing programs that meet established quality criteria to the public, to employers, and to students and their parents. Being accredited is a mark of achievement for a university, helping it attract the best and brightest students. He has authored or co-authored numerous successful proposals that have provided funding for accreditation workshops in South and Central America, Germany, and Slovakia. In addition, he has coordinated a "Memorandum of Cooperation" between the IEEE and the All India Council for Technical Education.

On 3 November, Dr. Yeargan was installed as 2002 ABET president. Dr. Yeargan is currently a professor and Texas Instruments Chair of mixed-signal and mixed-signal microelectronics in the Department of Electrical Engineering at the University of Arkansas. He joined the University of Arkansas faculty in 1963. He received his PhD in electrical engineering from the University of Texas.

SSCS EVENTS CALENDAR

Also posted on *www.sscs.org/meetings*

SSCS Sponsored Meetings

2002 CICC Custom Integrated Circuits Conference
www.his.com/~cicc
12–15 May 2002
Caribe Royale Resort Suites, Orlando, FL
Contact: Ms. Melissa Widerkehr, cicc@his.com

2002 Symposium on VLSI Circuits
www.vlsisymposium.org
13–15 June 2002
Hilton Hawaiian Village, Honolulu, HI
Contact: Phyllis Mahoney, vlsi01@aol.com
or Business Center for Academic Societies Japan
vlsisymp@bcasj.or.jp

2002 SSCTC Workshop
www.ieee.org/ssctc
10–11 October 2002
Key Bridge Marriott, Arlington, VA
Contact: mkramer@courtesyassoc.com

2003 ISSCC International Solid-State Circuits Conference
www.isscc.org
7–9 February 2003
San Francisco Marriott Hotel, San Francisco, CA
Paper deadline: 4 September 2002
Contact: Courtesy Associates, ISSCC@courtesyassoc.com

To maintain all your IEEE and SSCS subscriptions, email address corrections to:
address-change@ieee.org

Technically Co-sponsored Meetings

2002 Radio Frequency Integrated Circuits Symposium
www.rfic2002.org
2–4 June 2002
Seattle, WA

2002 ACM/IEEE Design Automation Conference
www.dac.com
10–14 June 2002
New Orleans, LA

2002 Symposium on VLSI Technology
www.vlsisymposium.org
11–13 June 2002
Hilton Hawaiian Village, Honolulu, HI

2002 European Solid-State Circuits Conference
ele.unipv.it/esscirc2002/index.html
24–26 September 2002
Florence, Italy
Deadline for Electronic Submission: 5 April 2002

2002 Bipoloar/BiCMOS Circuits and Technology Meeting
www.ieee-bctm.org/
29 Sept – 1 October 2002
Minneapolis Marriott City Center

2002 GaAsIC Symposium
www.gaasic.org/
21–23 October 2002
Monterey, CA
Deadline for Abstracts: 18 April 2002

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