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Back-side Thinning of Silicon Carbide Wafer by Plasma Etching using Atmospheric-pressure Plasma

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Abstract. Silicon carbide (SiC) power devices have received much attention in recent years because they enable the fabrication of devices with low power consumption. To reduce the on-resistance in vertical power transistors, back-side thinning is required after device processing. However, it is difficult to thin a SiC wafer with a high removal rate by conventional mechanical machining because its high hardness and brittleness cause cracking and chipping during thinning. In this study, we attempted to thin a SiC wafer by plasma chemical vaporization machining (PCVM), which is plasma etching using atmospheric-pressure plasma. The wafer level thinning of a 2-inch 4H-SiC wafer has been possible without a removal thickness distribution caused by the circular shape of the wafer using the newly developed PCVM apparatus for back-side thinning with a spatial wafer stage.

Introduction

It is very important to develop energy conservation technologies as well as sustainable energy technologies for a sustainable future. In particular, technologies for reducing the use of electrical energy are essential because electric power is the secondary energy produced in the greatest quantity from primary energy sources. The frequency and impedance of electric power are controlled so that it can be used efficiently. Although silicon (Si) power devices are currently used to control them, silicon carbide (SiC) power devices have received much attention in recent years because SiC has better properties than Si such as its large band gap and high breakdown electric field, which result in devices with lower power consumption. SiC power devices such as Schottky barrier diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) are commercially available, although they are not yet widely used. One of the main issues preventing their widespread use is the high wafering and processing cost. SiC is an extremely hard material and is difficult to process by conventional mechanical machining methods. Furthermore, once a damaged layer is generated on the processed surface of a SiC substrate, it is difficult to remove it because of the chemical inertness of SiC. Thus, we are developing novel chemical processing methods for SiC processing. A SiC wafer is generally formed by crystal growth, slicing, lapping, bevelling and polishing. After processing the device on it, it is thinned, diced and packaged. We focus on a thinning process in this study. Back-side thinning is required after device processing to reduce the on-resistance in vertical devices such as power MOSFETs. Although it is easy to thin a Si wafer by conventional mechanical machining processes such as grinding and polishing, it is difficult to thin a SiC wafer at a high removal rate by these processes because its high hardness and brittleness cause cracking and chipping during thinning. Thus, we attempted to thin a SiC wafer by plasma chemical vaporization machining (PCVM), which is plasma etching using atmospheric-pressure plasma [1-5]. No external force that can cause cracking or chipping is applied in PCVM because it is a non-contact machining method. Moreover, it has a high removal rate because of the high radical density in atmospheric-pressure plasma, and no damaged layer is formed on the processed surface because of the low ion energy. We have already reported that a 4H-SiC (0001) C-face strip specimen (20 × 5 mm^2) was successfully thinned to 40 μm by PCVM without any cracking or chipping [6]. We have also reported the thinning of a 2-inch SiC wafer by PCVM using a cylindrical rotary electrode and a scanning table [7]. However, we found that the removal rate was much larger (more than triple) at the outer part of the wafer than in the central area. This is mainly because the length of the plasma was smaller at the edges of the wafer owing to the circular shape of the wafer, which resulted in a higher plasma density (Fig. 1 (a)). Thus in this study, we developed wafer thinning apparatus with a rectangular raised frame that enables us to realize the condition of a constant plasma length while scanning (Fig. 1(b)) and attempted to thin a 2-inch SiC wafer.

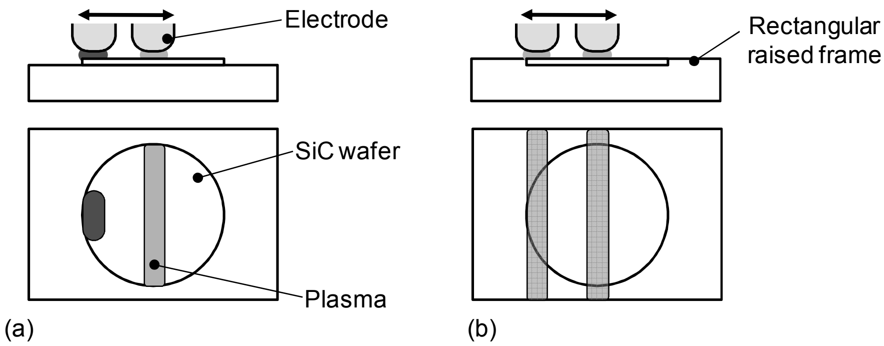

Fig. 1. (a) Schematic of the influence of the circular shape of wafer for line-plasma scanning application, and (b) our proposal on the use of a rectangular raised frame for its improvement

Experiment Apparatus and Procedure

Figure 2 shows a schematic of the sample stage system with the rectangular raised frame. The wafer stage has an elevating axis, while the frame is fixed and electrically grounded. The surface of the wafer is adjusted to be the same level as that of the frame by controlling the elevating axis. The wafer stage also has a rotation axis for averaging, an electrical heater for elevating the wafer temperature and a vacuum chuck system for chucking the wafer. Figure 3 shows a schematic of the PCVM thinning apparatus. An electrode is mechanically fixed to an electrode holder by an insulating ceramic connector and electrically connected to an rf power supply through an impedance matching unit. The electrode holder has an x-axis for plasma scanning and a z-axis for adjusting the gap between the wafer and the electrode.

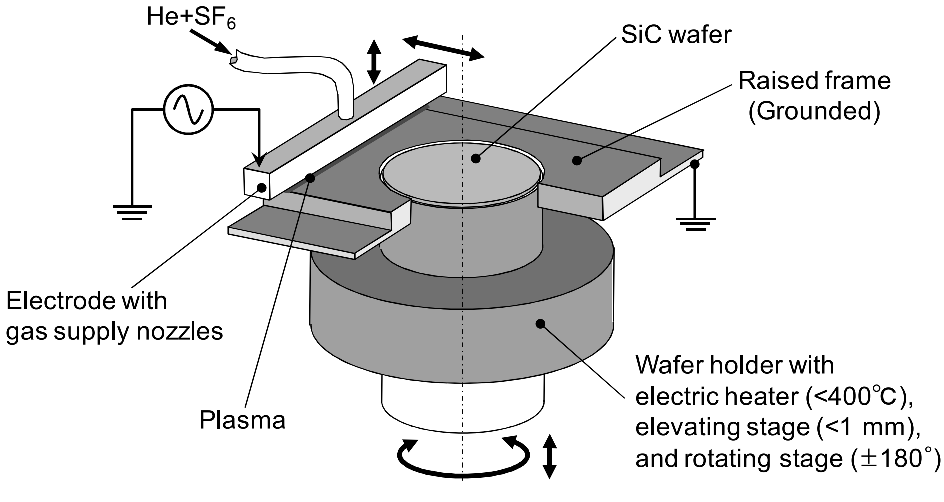

Fig. 2. Schematic of wafer stage system for thinning application with a rectangular raised frame

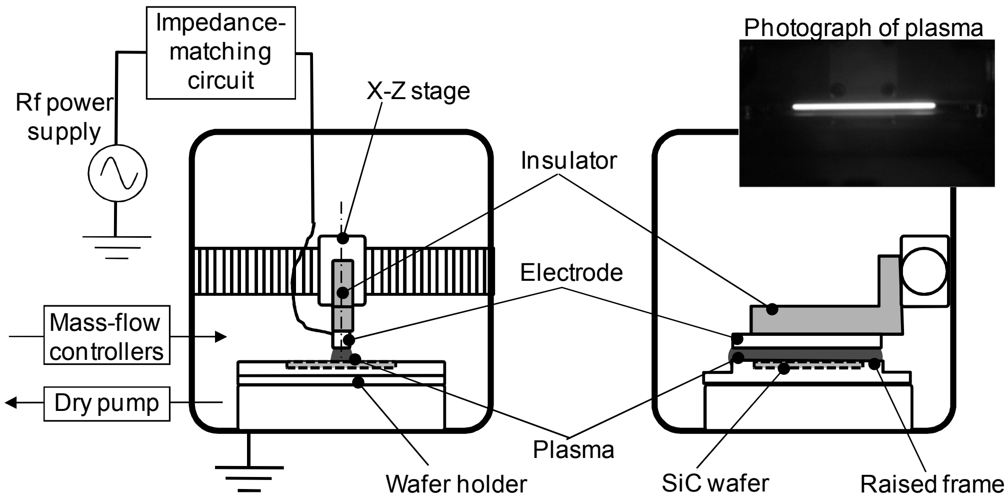

Fig. 3. Schematic of PCVM thinning apparatus

A 2-inch 4H-SiC (0001) (C-face) wafer was set on the wafer stage after sulphuric-peroxide mixture cleaning. The air initially present in the chamber was evacuated, and a reactive gas of SF_6 and He was supplied until the chamber reached atmospheric pressure. Then, 150 MHz rf power was supplied to the electrode to generate band-like plasma. The electrode was scanned in the direction perpendicular to the plasma to process the entire wafer. The sample was removed from the chamber after waste gas evacuation and nitrogen purging. The thickness of the wafer was measured using a spectral-interference wafer thickness meter system (Keyence Corp. SI-F80 and KS-1100). The weight of the wafer was also measured using an electronic balance. The surface roughness of the wafer was measured using a scanning white-light interferometer (Zygo NewView200).

Results and Discussion

Removal Thickness Distribution. Wafer level thinning was performed under the following conditions: He:SF_6=99.7:0.3, machining gap of 350 mm, rf power of 600 W, wafer temperature of 400 °C and scanning speed of 0.1 mm/s. From the visual observation of the plasma, it was confirmed that the length of the plasma corresponded to the length of the rectangular frame and showed no change during scanning. The thickness distributions of the preprocessed and 40-min-processed wafers were measured. Figures 4(a) and 4(b) show these thickness distributions, respectively, and Fig. 4(c) shows the removal thickness distribution calculated by subtracting the processed thickness from the preprocessed thickness. A histogram of the removal thickness data is shown in Fig. 5. The

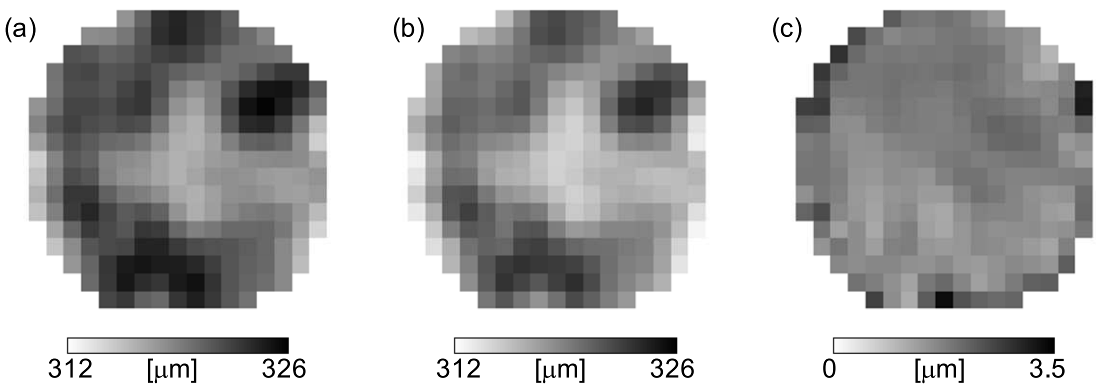

Fig. 4. Thickness distributions of (a) initial wafer and (b) PCVM-processed wafer and (c) removal thickness distribution calculated by subtracting (b) from (a)

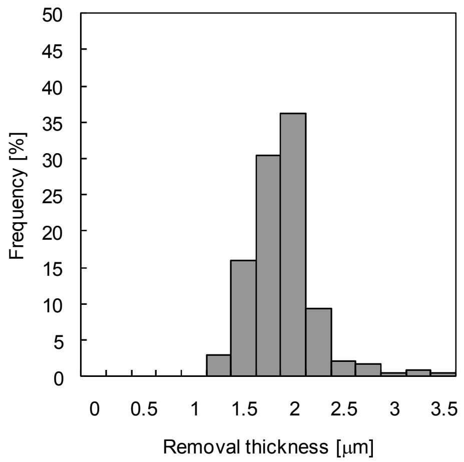

Fig. 5. Histogram of removal thickness data shown in Fig. 4(c)

average is 1.76 μm, which is in good agreement with the weight loss and the standard deviation is 0.33 μm. Although the standard deviation is considerable, there was no significant difference between the removal thickness of the central part of the wafer and that of the outer part of the wafer. Thus, it is proved that a constant plasma length while scanning on a circular wafer can be realized using a rectangular raised frame. We think that one of the reasons for the removal thickness variation is the surface contamination of preprocessed wafers, which can be improved by careful preliminary cleaning of the wafer.

Surface Roughness. The transition of the surface roughness of a SiC wafer in PCVM was investigated. The initial surface of the sample was ground and had no optical transparency (Fig. 6(a)). The wafer was thinned by PCVM for 160 min, an additional 80 min and another additional 80 min, under the following conditions: He:SF_6=99:1, machining gap of 460 mm, rf power of 400 W, wafer temperature of 400 °C and scanning speed of 0.1 mm/s. The removal rate under this condition was approximately 3.75 μm/h. Figures 6(a) and 6(c) show photographs of both the initial wafer surface and the 20-μm-removed wafer surface, respectively, and Figs. 6(b) and 6(d) show images of the scanning white-light interferometer of both wafer surfaces. Figures 6(c) and 6(d) show that the processed surface became smoother and acquired optical transparency. Figure 7 shows the relationship between the rms (root mean square) roughness and removal thickness. It was shown that

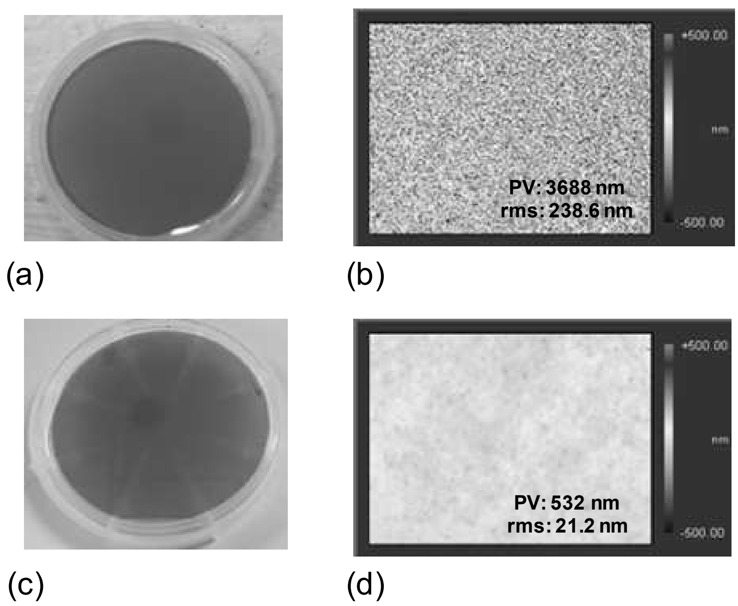

Fig. 6. (a) Photographs of initial wafer and (c) 20-μm-removed wafer. Images obtained using scanning white-light interferometer of (b) initial wafer (320×240 μm^2) and (d) 20-μm-processed wafer.

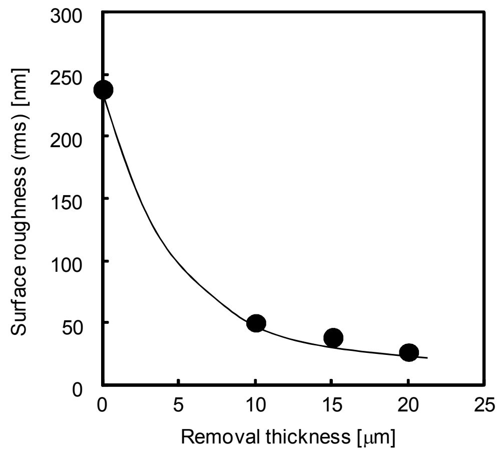

Fig. 7. Relationship between surface roughness (root mean square, rms) and removal thickness

the surface roughness improved with increasing removal thickness. The reason for the improved roughness is qualitatively considered to be the etching reaction proceeding not only in the vertical direction into the substrate but also in the lateral direction. Therefore, micrometer-scale convex regions are considered to become smaller and finally disappear as etching progresses.

Summary

We developed PCVM apparatus for the back-side thinning of a SiC wafer with a rectangular raised frame that enables us to realize the condition of a constant plasma length while scanning. Using the apparatus, we showed that the non-uniform removal thickness observed in the apparatus without a raised frame was markedly improved. Although its removal rate of several micrometres per hour is not high, PCVM's removal rate of more than several tens of micrometres per minute without scanning is still considerable. Thus, the wafer level removal rate with scanning increases with increasing rf power or plasma area.

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