CMOS Standard Cells Characterization for Defect Based Testing

Witold A. Pleskacz, Dominik Kasprowicz, Tomasz Oleszczak[1] and Wieslaw Kuzmicz[2]
Institute of Microelectronics & Optoelectronics
Warsaw University of Technology
ul. Koszykowa 75, 00-662 Warszawa, POLAND
e-mail: pleskacz@imio.pw.edu.pl

Abstract

This paper extends the CMOS standard cells characterization methodology for defect based testing. The proposed methodology allows to find the types of faults which may occur in a real IC, to determine their probabilities, and to find the input test vectors which detect these faults. For shorts at the inputs two types of cell simulation conditions – "Wired-AND" and "Wired-OR" – are used. Examples of industrial standard cells characterization indicate that a single logic fault probability table is not sufficient. Separate tables for "Wired-AND" and "Wired-OR" conditions at the inputs are needed for full characterization and hierarchical test generation.

1. Introduction

It is well known from the literature [e.g. 1-5] that classical test generation methods cannot handle the actual behavior of faulty digital circuits implemented as CMOS ICs. These methods allow to generate test vectors using logic-driven gate-level models to represent the circuit design and abstract fault models (e.g. the stuck-at fault model) to describe manufacturing defects causing IC failure. As a result the circuit layout, physical defects characteristics and the actual circuit behavior are ignored.

To overcome these limitations, in [5, 6] circuit and layout-driven test generation methods were proposed. In these works the whole circuits having hundreds of gates were analyzed as single blocks. Such an approach is computationally expensive and thus highly impractical as a method of generation of tests for real VLSI designs. An alternative approach has been proposed recently [7, 9, 10]. In these works functionality of gates from a standard cell library is analyzed for all possible physical defects using transistor-level simulation. This characterization process may be computationally expensive, but it should be done only once for every standard library cell. This information can be used for defect oriented fault simulation and test generation at higher levels of abstraction [9-11]. It can be shown that classical stuck-at fault based simulation and the test coverage calculation based on counting defects without considering defect probabilities may lead to considerable overestimation of results [8].

In this paper we extend the previous works in the following way:

(a) We define more precisely the simulation conditions of "Wired-AND" and "Wired-OR" shorts at inputs of logic gates.
(b) We use an alternative method of characterization of probabilities of physical defects based on a commercial CAD tool (Dracula).
(c) As a result of (a) and (b), we present examples of new results of estimation of probabilities of logic faults in several digital gates. These results include multiple shorts.

---

[1] Currently with Measurement Microsystems A-Z Inc., Trois-Rivieres, Quebec, CANADA.
[2] Currently with Institute of Electron Technology, Warsaw, POLAND.

The paper is organized as follows. In Section 2 the method of estimation of defect occurrence probabilities is introduced. Identification of faulty functions and test vectors generation procedure is described in Section 3. Section 4 presents examples of characterized standard cells.

2. Estimation of defect occurrence probabilities

In the following we consider one kind of physical defects in CMOS gates - shorts between conducting regions. This is one of the most important sources of faults in CMOS digital circuits. However, the methodology can be extended to other types of physical defects as well (e.g. breaks). A short is a piece of extra conducting material that connects a pair of separate conducting regions in the integrated circuit. This affects the connectivity of the circuit - two separate electrical nodes become shorted. It is intuitively obvious that probabilities of shorts depend on the layout of the circuit. Conducting regions that are adjacent to one another are more susceptible to shorts than regions that are separated by a large distance. We assume that every defect, which results in a short, can be approximated by a circle. To estimate the probabilities of shorts between pairs of nodes we use the concept of critical area for shorts [12, 13]. The critical area for shorts is such a region in the circuit that if the center of a defect of a given radius *r* is located anywhere inside the critical area, a short between two adjacent conducting regions occurs. Fig. 1 illustrates the concept of critical area for shorts.

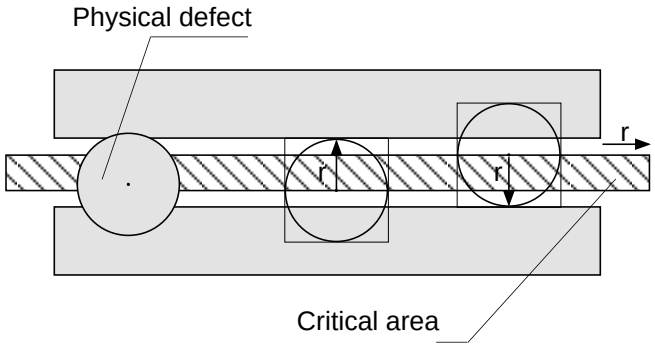

Figure 1. *Concept of the critical area for shorts.*

Probability that two electrical nodes will be shorted by a physical defect is given by the following formula derived from Poisson based yield model:

$$P_{sh} = 1 - \prod_{i=1}^{N} \exp\left[-\int_{0}^{+\infty} Acr_i(r) \cdot D_{oi} \cdot f_{ri}(r)\, dr \right] \tag{1}$$

where: i is the type of conducting layer, N is the number of conducting layers, r is the radius of the defect (a random variable), $Acr_i(r)$ is the critical area function, D_{oi} is the density of physical defects of type "i". $f_{ri}(r)$ is the size distribution function for defects of type "i" given by [14, 15]:

$$f_{ri}(r) = \begin{cases} \dfrac{2(p_i - 1) \cdot r}{(p_i + 1) \cdot X_{0i}^2}, & \text{for: } \quad 0 < r \le X_{0i} \\ \dfrac{2(p_i - 1) \cdot X_{0i}^{p_i - 1}}{(p_i + 1) \cdot r^{p_i}}, & \text{for: } \quad X_{0i} < r. \end{cases} \tag{2}$$

The size distribution function has two parameters: X_{0i} (which is modeled to be very small compared to the minimum feature size of a given manufacturing process) and parameter p_i. In our calculations of the probability of shorts three the most important conducting layers – Polysilicon, Metal1 and Metal2 were taken into account. Parameter X_{0i} was assumed to be 20% of the minimal distance between shapes on a given conducting layer, $p = 3$ and $D_o = 10$ defects/cm^2.

In this work we extracted the critical area using the commercial CAD tool (Dracula) by means of a series of geometrical operations on the cell layout. The operations that are possible in Dracula are normally used for design rule checking, but they can also be used for other geometrical transformations of the layout, and in particular for extraction of the critical area defined as in Fig. 1.

Formula (1) allows to calculate the probability of shorts between more than two electrical nodes as well. In this case critical area Acr_i should be extracted for nonequipotential conducting paths representing given nodes altogether.

3. Faulty functions identification and test vectors generation

The first step in identification of logic faults and their probabilities is to calculate P_{sh} for all pairs of conducting regions representing electrical nodes. If for a given pair $P_{sh} = 0$, this pair of nodes cannot be shorted and is not taken into account. For the pairs that can be shorted the logic faults are determined. In simple cases this can be done by inspection of the circuit, for example it is obvious that a short between an output node and V_{DD} results in "Stuck-at-1" fault at this node. In more complex cases it may be necessary to simulate operation of the faulty circuit at the transistor level.

Analyzed gates and circuits were simulated electrically to find the test set for each short. A testbench circuit (see Fig. 2) was implemented in HSPICE. Level 47 (BSIM3 Version 2.0) MOS transistor model was used in simulations.

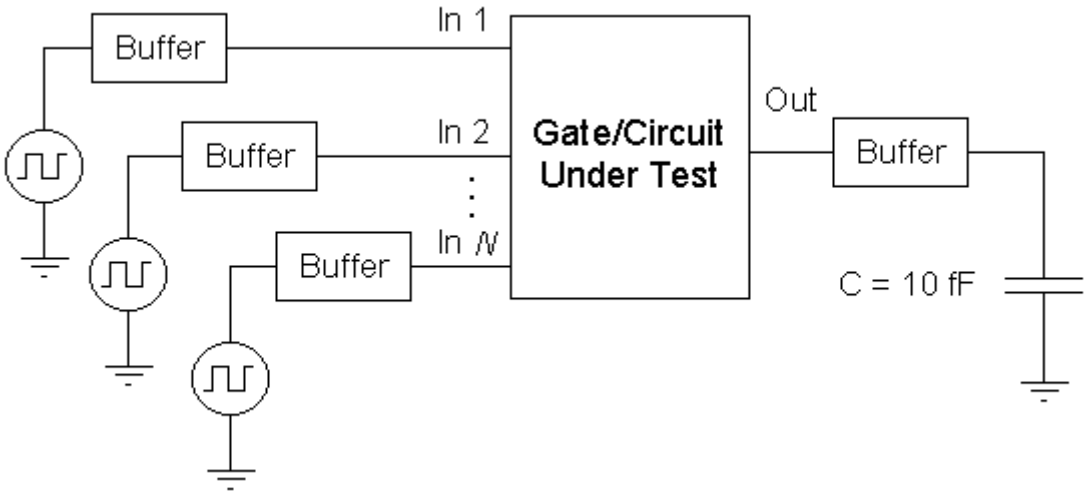

Figure 2. *Testbench circuit schematic diagram.*

For each short the responses to all the input vectors were found. If at least one net of the shorted pair was an input, the simulation was carried out twice using "Wired-AND" and "Wired-OR" models. These two models were implemented by using input buffers with MOS transistors of different channel geometries. The construction of the buffers is shown in Fig. 3. The channel width values of the transistors used in the buffers are given below:

- "Wired-AND" shorts: PMOS W = 10 µm, NMOS W = 10 µm;
- "Wired-OR" shorts: PMOS W = 40 µm, NMOS W = 5 µm.

The channel length was 0.8 µm in all the transistors.

In some cases (e.g. when one of the shorted nets was the output) the output voltage of the tested circuit was significantly different from the expected one, i.e. either 0.0 or 5.0 volts. To avoid ambiguity in classifying such responses as logic one or logic zero, a non-inverting buffer (of the same construction as the input ones) regenerating the voltage level was connected to the output. For each input vector the buffer's output voltage was compared with the correct value of the logic function implemented by the tested circuit. If these two values did not match, the input vector was counted as a test vector.

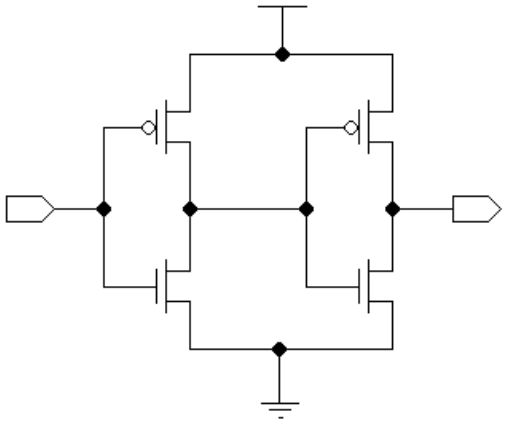

Figure 3. *Buffer schematic diagram.*

A short itself was implemented in the SPICE netlist as a resistor of 100 mΩ, which is the average value of sheet resistance of metals used in the 0.8 µm CMOS process. As the resistances of contacts and vias in this technology are several orders of magnitude higher, the value of the resistor simulating a short is not critical. We tried several resistance values in the range from 0.01Ω to 200Ω. The gate behavior at the logic level did not depend on this resistance. The waveforms obtained from the simulation allow to determine the actual logic function performed by the faulty circuit.

The procedure presented above is the most time consuming part of the characterization. If the number of possible shorts is large and operation of the faulty cell is not obvious for most of them, it is necessary to perform many circuit simulations. This is time consuming and difficult to automate. Hence, the complexity of the characterization process depends mainly on the number of physically possible shorts in the characterized cell and the complexity of the cell function. In practice it may take from several hours to several days to characterize a single cell. However, this process is performed only once for every library cell. In this way the functional faults that result from shorts are identified and their probabilities are determined.

4. Examples of standard cells characterization

The methods described in Section 2 and 3 were used for characterization of gates from an industrial standard cell library in 0.8 µm CMOS technology. Fig. 4 shows the distribution of the probabilities of various types of functional faults for a complex 4 input *AN3* gate performing the *not((A and B) or C or D)* function. Logic and schematic diagrams of *AN3* gate are shown in Fig. 5.

In Table 1, the mapping between functional faults, input vectors of the gate and defects (for "Wired-AND" shorts) is given. For each vector, all the defects detected by this vector are marked by 1.

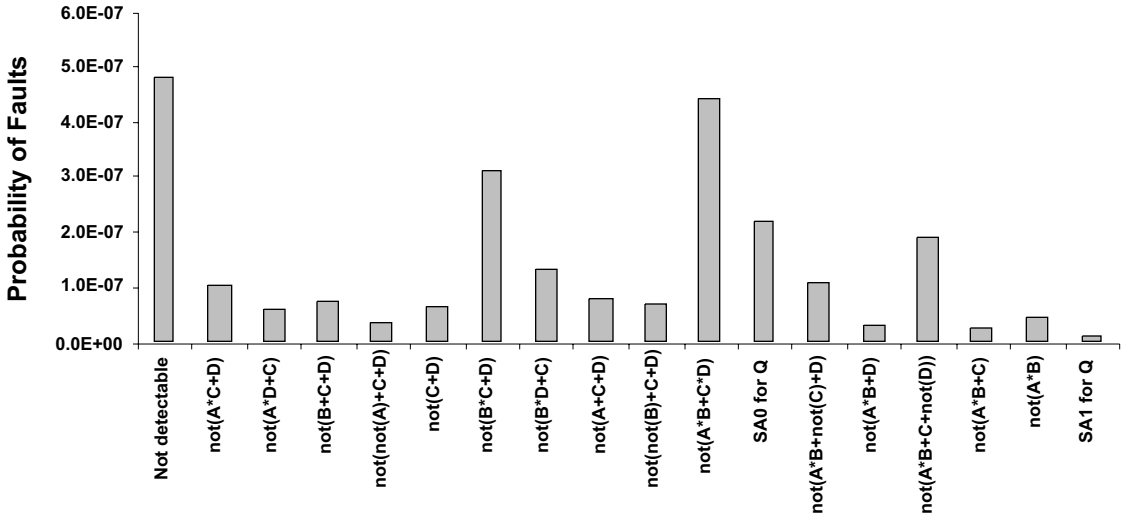

Figure 4. *Distribution of probabilities of faults for AN3 gate.*

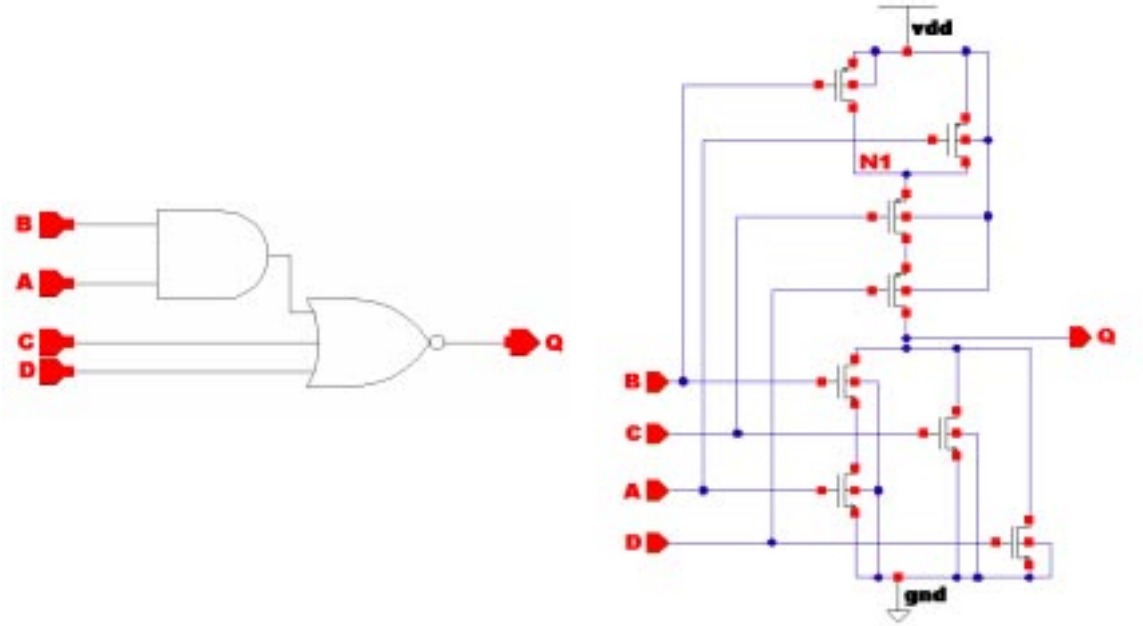

Figure 5. *Logic diagram (left) and schematic diagram (right) of AN3 complex gate.*

Based on data from Table 1 the effectiveness of test vectors was calculated (see Table 2). This effectiveness is defined as the total probability of occurrence of a group of all faults detected by a given test vector [7]. In Table 2 one can see that the vector V(1) = 0010 has the highest effectiveness.

Table 1. *Probabilities of defects ("Wired-AND" shorts) in the complex gate AN3 and the fault table.*

i	Fault d_i	Erroneous function f^{di}	Probability P_i		Input vector t_j <ABCD>															
			absolute	relative	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	A/B	**not detected**	3.2938e-07	0.13550	**none**															
2	A/C	not(A*C+D)	1.0199e-07	0.04196			1				1						1			
3	A/D	not(A*D+C)	5.8123e-08	0.02391		1				1							1			
4	A/n1	not(B+C+D)	5.0892e-08	0.02094					1											
5	A/Q	not(not(A)+C+D)	3.1540e-08	0.01297	1				1								1			
6	A/gnd	not(C+D)	3.4523e-08	0.01420													1			
7	A/vdd	not(B+C+D)	1.8743e-08	0.00771					1											
8	B/C	not(B*C+D)	3.0736e-07	0.12644			1								1		1			
9	B/D	not(B*D+C)	1.2855e-07	0.05288		1								1			1			
10	B/n1	not(A+C+D)	5.5331e-08	0.02276									1							
11	B/Q	not(not(B)+C+D)	6.5150e-08	0.02680	1								1				1			
12	B/gnd	not(C+D)	2.7366e-08	0.01126													1			
13	B/vdd	not(A+C+D)	2.1387e-08	0.00880									1							
14	C/D	not(A*B+C*D)	4.4240e-07	0.18199		1	1			1	1			1	1					
15	C/n1	SA0 for Q	4.0733e-08	0.01676	1				1				1							
16	C/Q	not(A*B+not(C)+D)	1.0515e-07	0.04326	1		1		1		1		1		1					
17	C/gnd	not(A*B+D)	2.5810e-08	0.01062			1				1				1					
18	C/vdd	SA0 for Q	1.4943e-08	0.00615	1				1				1							
19	D/n1	SA0 for Q	2.1978e-08	0.00904	1				1				1							
20	D/Q	not(A*B+C+not(D))	1.8618e-07	0.07659	1	1			1	1			1	1						
21	D/gnd	not(A*B+C)	2.1360e-08	0.00879		1				1				1						
22	D/vdd	SA0 for Q	1.0609e-08	0.00436	1				1				1							
23	n1/Q	not(A*B)	4.2614e-08	0.01753		1	1	1		1	1	1		1	1	1				
24	n1/gnd	SA0 for Q	7.2557e-09	0.00298	1				1				1							
25	n1/vdd	**not detected**	1.4613e-07	0.06011	**none**															
26	Q/gnd	SA0 for Q	1.2459e-07	0.05125	1				1				1							
27	Q/vdd	SA1 for Q	7.0250e-09	0.00289		1	1	1		1	1	1		1	1	1	1	1	1	1
28	gnd/vdd	**not detected**	3.7640e-09	0.00155	**none**															

Table 2. *Effectiveness of test vectors for the gate AN3.*

Test vector <ABCD>	Shorts detected	Effectiveness
V(1)=0010	A/C, B/C, C/D, C/Q, C/gnd, n1/Q, Q/vdd	1.0324e-06
V(2)=1010	B/C, C/D, C/Q, C/gnd, n1/Q, Q/vdd	9.3036e-07
V(3)=0001	A/D, B/D, C/D, D/Q, D/gnd, n1/Q, Q/vdd	8.8626e-07
V(4)=1001	B/D, C/D, D/Q, D/gnd, n1/Q, Q/vdd	8.2813e-07
V(5)=1100	A/C, A/D, A/Q, A/gnd, B/C, B/D, B/Q, B/gnd, Q/vdd	7.6163e-07
V(6)=0101	A/D, C/D, D/Q, D/gnd, n1/Q, Q/vdd	7.5771e-07
V(7)=0110	A/C, C/D, C/Q, C/gnd, n1/Q, Q/vdd	7.2499e-07
V(8)=1000	B/n1, B/Q, B/vdd, C/n1, C/Q, C/vdd, D/n1, D/Q, D/vdd, n1/gnd, Q/gnd	6.5331e-07
V(9)=0100	A/n1, A/Q, A/vdd, C/n1, C/Q, C/vdd, D/n1, D/Q, D/vdd, n1/gnd, Q/gnd	6.1262e-07
V(10)=0000	A/Q, B/Q, C/n1, C/Q, C/vdd, D/n1, D/Q, D/vdd, n1/gnd, Q/gnd	6.0813e-07
V(11)=0011	n1/Q, Q/vdd	4.9639e-08
V(12)=0111	n1/Q, Q/vdd	4.9639e-08
V(13)=1011	n1/Q, Q/vdd	4.9639e-08
V(14)=1101	Q/vdd	7.0250e-09
V(15)=1110	Q/vdd	7.0250e-09
V(16)=1111	Q/vdd	7.0250e-09

Taking into account that in many cases one fault can be detected by several test vectors, the concept of usefulness of test vectors was introduced in [7]. It allows to determine the

optimum sequence of test vectors. Having calculated the effectiveness for every test vector we can determine this sequence in the following way. We select the vector with the highest effectiveness as the first one, and we subtract the probabilities of occurrence of all faults detected by the first vector from the effectiveness of the remaining vectors. In this way we obtain the effectiveness of the remaining vectors for the remaining (i.e. not detected by the first vector) faults. We call it usefulness of the test vectors. Now we select as the second vector the one with the highest usefulness, and again we subtract from the usefulness of the remaining vectors the probabilities of the faults detected by the second vector. We repeat this procedure selecting the third vector and subsequent ones until no more undetected faults remain. The results of the usefulness computation for *AN3* cell are presented in Table 3 and Fig. 6. The fault coverage for 5 test vectors equals 80.28%.

Table 3. *Usefulness of test vectors for the gate AN3 ("Wired-AND" shorts).*

Test vector <ABCD>	Shorts detected	Usefulness	
		absolute	relative
V(1)=0010	A/C, B/C, C/D, C/Q, C/gnd, n1/Q, Q/vdd	1.0324e-06	0.42468
V(2)=1000	B/n1, B/Q, B/vdd, C/n1, C/vdd, D/n1, D/Q, D/vdd, n1/gnd, Q/gnd	5.4816e-07	0.22550
V(3)=1100	A/D, A/Q, A/gnd, B/D, B/gnd	2.8010e-07	0.11523
V(4)=0100	A/n1, A/vdd	6.9635e-08	0.02865
V(5)=0001 (or 0101, or 1001)	D/gnd	2.1360e-08	0.00879

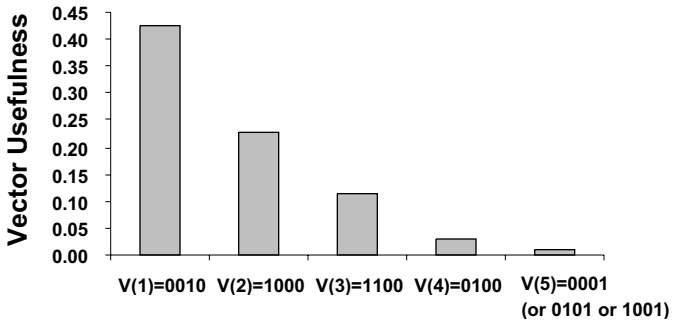

Figure 6. *Usefulness of test vectors for the gate AN3.*

The similar simulations for *AN3* cell but with "Wired-OR" shorts were carried out as well. Obtained fault table, like Table 1, is different. We did not include it because of the lack of space. But the most important results – usefulness of test vectors – are presented in Table 4. As one can note the sequence of test vectors was changed and sets of detected defects are different. In this case the fault coverage equals 75.63%.

Table 4. *Usefulness of test vectors for the gate AN3 ("Wired-OR" shorts).*

Test vector <ABCD>	Shorts detected	Usefulness	
		absolute	relative
V(1)=0100	A/B, A/n1, A/Q, A/vdd, B/C, B/D, C/n1, C/Q, C/vdd, D/n1, D/Q, D/vdd, n1/gnd, Q/gnd	1.3779e-06	0.56683
V(2)=1000	A/C, A/D, B/n1, B/Q, B/vdd	3.0198e-07	0.12423
V(3)=0010	C/gnd, n1/Q, Q/vdd	7.5449e-08	0.03104
V(4)=1100	A/gnd, B/gnd	6.1889e-08	0.02546
V(5)=0001 (or 0101, or 1001)	D/gnd	2.1360e-08	0.00879

In order to check the importance of defects causing shorts between more than two electrical nodes a similar characterization procedure for *NA2 = NAND(A,B)* gate was carried out. The results for "Wired-AND" shorts in *NA2* gate are presented in Table 5.

Table 5. *Probabilities of "Wired-AND" shorts in the gate NA2 and the fault table.*

i	Fault d_i	Erroneous function f^{di}	Probability P_i		Input vector t_j <AB>			
			absolute	relative	0	1	2	3
1	A/B	**not detected**	3.4405e-07	0.27840	**none**			
2	A/Q	A	1.4407e-07	0.11658	1	1		1
3	A/gnd	SA1 for Q	1.7382e-08	0.01407				1
4	A/vdd	not B	4.5933e-08	0.03717		1		
5	B/Q	B	8.1981e-08	0.06634	1		1	1
6	B/gnd	SA1 for Q	4.5555e-08	0.03686				1
7	B/vdd	not A	1.1434e-07	0.09252			1	
8	Q/gnd	SA0 for Q	6.6776e-08	0.05403	1	1	1	
9	Q/vdd	SA1 for Q	1.0407e-07	0.08421				1
10	gnd/vdd	**not detected**	5.5575e-09	0.00450	**none**			
11	A/B/Q	A*B	5.9993e-08	0.04855	1	1	1	1
12	A/B/gnd	SA0 for Q	1.6993e-08	0.01375	1	1	1	
13	A/B/vdd	SA1 for Q	2.7522e-08	0.02227				1
14	A/Q/gnd	SA0 for Q	1.3286e-08	0.01075	1	1	1	
15	A/Q/vdd	SA1 for Q	2.6166e-08	0.02117				1
16	A/gnd/vdd	**not detected**	5.3552e-09	0.00433	**none**			
17	B/Q/gnd	SA0 for Q	1.7587e-08	0.01423	1	1	1	
18	B/Q/vdd	SA1 for Q	3.2060e-08	0.02594				1
19	B/gnd/vdd	**not detected**	5.5220e-09	0.00447	**none**			
20	Q/gnd/vdd	**not detected**	1.7270e-08	0.01397	**none**			
21	A/B/Q/gnd	SA0 for Q	1.2897e-08	0.01044	1	1	1	
22	A/B/Q/vdd	SA1 for Q	1.6905e-08	0.01368				1
23	A/B/gnd/vdd	**not detected**	5.3194e-09	0.00430	**none**			
24	A/Q/gnd/vdd	**not detected**	4.6267e-09	0.00374	**none**			
25	B/Q/gnd/vdd	**not detected**	4.5913e-09	0.00372	**none**			

In Table 5 one can observe that triple and quadruple shorts have much lower importance than double shorts from probability of occurrence point of view. For data completeness results of the usefulness computation for *NA2* cell are presented in Table 6 and Fig. 7.

Table 6. *Usefulness of test vectors for the gate NA2 ("Wired-AND" shorts).*

Test vector <AB>	Shorts detected	Usefulness	
		absolute	relative
V(1)=11	A/Q, A/gnd, B/Q, B/gnd, Q/vdd, A/B/Q, A/B/vdd, A/Q/vdd, B/Q/vdd, A/B/Q/vdd	5.5570e-07	0.44967
V(2)=10	B/vdd, Q/gnd, A/B/gnd, A/Q/gnd, B/Q/gnd, A/B/Q/gnd	2.4188e-07	0.19593
V(3)=01	A/vdd	4.5933e-08	0.03717
V(4)=00	**not used**	0	0

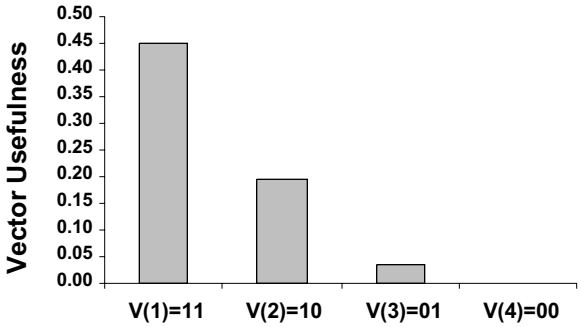

Figure 7. *Usefulness of test vectors for NA2 cell ("Wired-AND" shorts).*

5. Conclusions

In this work we demonstrated that a commercial CAD tool can be used for characterization of probabilities of physical defects in digital cells. Therefore, the methodology proposed in [7, 9, 10] is generally available and does not necessarily require a special purpose software tool. We also analyzed more precisely the cell behavior taking into account by means of appropriate input buffers two possible conditions when shorts at inputs occur: the "Wired-AND" condition and the "Wired-OR" condition. Depending on chosen simulation condition the sequence of test vectors and sets of detected defects are different. This indicates that a cell must be characterized by two logic fault probability tables and in hierarchical testing one or the other must be used depending on the conditions at the inputs.

Acknowledgements

This work was supported in part by the Polish State Committee for Scientific Research under project No. 8 T11B 006 16. The authors are grateful for Dr. M. Blyzniuk and Dr. M. Lobur from Lviv Polytechnic National University, Ukraine for their contribution in an earlier stage of this work.

References

[1] S. Chakravarty, "Defect based testing," invited talk at *the 4th Int. Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems – IEEE DDECS 2001*, Gyor, Hungary, April 2001.

[2] J.M. Soden, C.F. Hawkins, "Quality Testing Requires Quality Thinking," *Proc. of the Int. Test Conference*, pp. 596, Baltimore, USA, October 1993.

[3] W.Maly, J.P.Shen, J.Ferguson, "System. Characterization of Physical Defects for Fault Analysis of MOS IC Cells," *Proc. of the Int. Test Conference*, pp. 390-399, Philadelphia, USA, October 1984.

[4] J.P.Shen, W.Maly, J.Ferguson, "Inductive Fault Analysis of MOS ICs," *IEEE Design&Test*, pp.13-26, 1985.

[5] P.Nigh and W.Maly, "Layout - Driven Test Generation," *Proc. of the IEEE Int. Conference on Computer-Aided Design – ICCAD-89*, pp. 154-157, Santa Clara, USA, November 1989.

[6] M.Jacomet, W.Guggenbuhl, "Layout-Dependent Fault Analysis and Test Synthesis for CMOS Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 12, no. 6, pp. 888-899, 1993.

[7] M. Blyzniuk, W. A. Pleskacz, M. Lobur, W. Kuzmicz: "Estimation of the Usefulness of Test Vector Components for Detecting Faults Resulting from Shorts in Standard Cells," *Proc. Int. Conference: "Mixed Design of Intengrated Circuits and Systems" – MIXDES 2000*, pp. 527-532, Gdynia, Poland, June 2000.

[8] M. Blyzniuk, T. Cibakova, E. Gramatova, W. Kuzmicz, M. Lobur, W. A. Pleskacz, J. Raik, R. Ubar: "Defect Oriented Fault Coverage of 100% Stuck-At Fault Test Sets," *Proc. of the 7th Int. Conference: "Mixed Design of Intengrated Circuits and Systems" – MIXDES 2000*, pp. 511-516, Gdynia, Poland, June 2000.

[9] M. Blyzniuk, T. Cibakova, E. Gramatova, W. Kuzmicz, M. Lobur, W. A. Pleskacz, J. Raik, R. Ubar: "Hierarchical Defect-Oriented Fault Simulation for Digital Circuits," *Proc. of the IEEE European Test Workshop*, pp. 69-74, Cascais, Portugal, May 2000.

[10] W. Kuzmicz, W. Pleskacz, J. Raik, R. Ubar: "Defect-Oriented Fault Simulation and Test Generation in Digital Circuits," *Proc. of the 2001 IEEE 2nd International Symposium on Quality Electronic Design – ISQED 2001*, pp. 365-371, San Jose, USA, March 2001.

[11] T. Cibakova, E. Gramatova, W. Kuzmicz, W. Pleskacz, J. Raik, R. Ubar: "Defect-Oriented Library Builder and Hierarchical Test Generation," *Proc. of the 4th Int. Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems – IEEE DDECS 2001*, pp. 163-168, Gyor, Hungary, April 2001.

[12] W. Maly and J. Deszczka, "Yield estimation model for VLSI artwork evaluation," *Electronics Letters*, vol. 19, no. 6, pp. 226-227, March 1983.

[13] W. Maly, "Modeling of lithography related yield losses for CAD of VLSI circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-4, no. 3, pp. 161-177, July 1985.

[14] C. H. Stapper, "Modeling of defects in integrated circuit photholitographic patterns," *IBM J. Res. Develop.*, vol. 28, no. 4, pp. 461-474, July 1984.

[15] C. H. Stapper, I. M. Armstrong and K. Saji, "Integrated circuit yield statistics," *Proc. of the IEEE*, vol. 71, no. 4, pp. 453-470, April 1983.

[16] G. A. Allan, A. J. Walton, "Hierarchical critical area extraction with the EYE tool," *Proc. of IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 28-36, Lafayette, USA, Nov. 1995.