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Title: New design criterion for high-order delta-sigma DACs

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New design criterion for high-order $\Delta\Sigma$ DACs

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Abstract

Stability analysis of high-order $\Delta\Sigma$ loops is a challenge. In this work,[1] a novel design criterion is presented for error-feedback DACs which are especially suitable for high-speed operation. This criterion allows the design of unconditionally stable, robust, high-order $\Delta\Sigma$ DACs. Both analytical and numerical analysis are performed for verification.

1 High-order $\Delta\Sigma$ modulators

Since a delta-sigma ($\Delta\Sigma$) modulator uses oversampling and quantization error shaping, it trades speed for resolution, and analog-circuit accuracy for digital-circuit complexity. A possible way to obtain a high-resolution and high-speed delta-sigma ADC or DAC is to use a high-order or/and multibit modulator.

Due to the presence of a nonlinear truncator or quantizer[2] in the system, the stability analysis of high-order (i.e., larger than two) loops is a challenge [1]. "Unstable" means that the modulator exhibits large, although not necessarily unbounded, states and a poor signal-to-noise ratio compared to those predicted by linear models [2, Sec. 4.1]. The chain of integrators or accumulators with feedback or feedforward summation are popular topologies for delta-sigma ADCs (Fig. 1.(a)) and DACs (Fig. 1.(b)), respectively. To ensure stability, a conservative empirical rule of Lee [3, 4] or/and the root-locus method [5] along with extensive simulations must be used. Lee's rule applies for single-bit modulators and it requires a gain of the noise transfer function less than 1.5 for any frequencies. Several functional ICs [6, 7] demonstrated that Lee's rule is valid. For multibit high-order designs a more relaxed value, e.g., of 3.5 [8], is sufficient for stability. In any case, while this requirement empirically ensures stability, it drastically limits the achievable performance of high-order modulators; moreover, precaution and lengthy simulations are necessary in their designs.

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[2]"Quantizers" and "truncators" are used in $\Delta\Sigma$ ADCs and DACs, respectively.

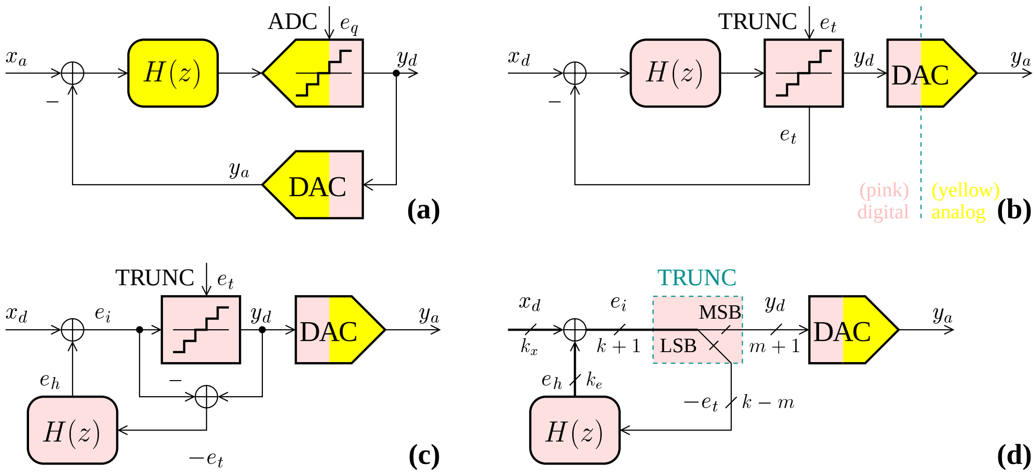

Figure 1: Topologies for delta-sigma modulators: **(a)** ADC: chain of integrators with feedback summation; **(b)** DAC: chain of accumulators with feedback summation; **(c)** error-feedback DAC (block diagram); **(d)** error-feedback DAC (details).

The error-feedback topology (Fig. 1.(c)) is not suitable for delta-sigma ADCs since the imperfections of the analog loop filter $H(z)$ would enter the critical input node and adversely affect the output. However, this drawback does not exist in digital modulator loops. Therefore, it is widely used in delta-sigma DACs [9, 10], [2, Chap. 5] (Fig. 1.(c)) and fractional-N PLLs [11]. For higher-order loop filters internal limiters [10] are often used which protects the overflow of the internal signals; also, the stability of the design needs to be carefully tested by extensive simulations. However, a trivial analysis may lead to a sufficient analytical stability criterion described in the followings.

2 Stability analysis

The block diagram of an error-feedback delta-sigma DAC is shown in Fig. 1.(c). The truncator (TRUNC) provides the most-significant bits (MSBs) for the DAC, and feeds the least-significant bits (LSBs) to $H(z)$. Using the additive white-noise model [2, Sec. 2.3] for the truncator, which replaces a deterministic nonlinearity with a stochastic linear system, we have

$$\begin{aligned} Y_d(z) &= X_d(z) + (1 - H(z))\, E_t(z) \\ &= STF(z)\, X_d(z) + NTF(z)\, E_t(z), \end{aligned} \tag{1}$$

where $STF(z) = 1$ is the signal transfer function and $NTF(z) = 1 - H(z)$ is the truncation error (or truncation noise) transfer function. In order to achieve low truncation error energy in the low-frequency signal band, $NTF(z)$ should have high-pass characteristics. A Butterworth approximation for choosing the pole-zero pattern of $NTF(z)$ leads to a Nth-order differentiator, that is, $(1 - z^{-1})^N$. N also gives the order of the delta-sigma loop.

When $NTF(z)$ is an FIR transfer function, $H(z)$ is also an FIR function. Therefore, there is no accumulation in $H(z)$ as opposed to the case of chain of integrators/accumulators topologies (Figs. 1.(a–b)). The only accumulation occurs during the addition at the input node, but this is directly followed by the truncation operation. Therefore, the bit length of *every* internal signal can be accurately predicted analytically without the need of numerical analysis.

Let us assume that the FIR loop filter $H(z)$ adds m bits to the bit length. The input summation adds one more bit the most. In order to keep all internal signals bounded, whatever enters needs to exit the loop, so y_d should have $m + 1$ bits at least (i.e., 'm' due to $H(z)$, and '1' due to the input summation). By notation the input x_d has k_x bits and the feedback e_h has k_e bits (Fig. 1.(d)). If $k_e \leq k_x$ holds, which is a valid initial condition, and y_d is kept to its minimal value of $m+1$, than e_i will have $k_x + 1$ bits the most, and $k_x - m$ LSBs will be fed back to the loop. This leads to e_h of k_x bits. Therefore, $k_x = k_e = k$ holds for steady state, and all internal signals are bounded indeed, as shown in Fig. 1.(d). Note that $k > m$ for practical reasons, so $k - m$ will not turn into negative.

In conclusion, a **sufficient stability criterion** can be formulated as follows: a stable high-order error-feedback topology requires a truncator of $m + 1$ bits when the FIR loop filter $H(z)$ contributes to an m-bit increase in the dataflow.

3 Practical considerations

Let us consider a Nth-order loop with $NTF(z) = (1 - z^{-1})^N$ and $H(z) = 1 - NTF(z)$. It can be shown[3] that the lowest value for m is N, so y_d has $m + 1 = N + 1$ bits. In case of a 5th-order loop with $NTF(z) = (1 - z^{-1})^5$ and $H(z) = z^{-1}(5 - 10z^{-1} + 10z^{-2} - 5z^{-3} + z^{-4})$, it turns out that $m = 5$ and y_d has 6 bits. Since 1-bit DACs are inherently linear, it is usually desired to obtain a single-bit dataflow at the digital output y_d. However, highly-linear multibit DACs were published recently [12], [2, Chap. 8] which can make the circuit practical and useful. Another possibility is to use such a high-order modulator in a cascade configuration [9].

Both the above described high-order error-feedback structure and the MASH topology [13–15] are unconditionally stable, and generate high-order noise-shaped, multibit output. However, the proposed high-order modulator does not rely on error cancellation, and it is implemented within a single loop, which makes it more robust, and more hardware and power efficient.[4]

In conclusion, the sufficient stability criterion states an analytical trade-off between the bit length of the output data stream and the order of the loop filter. This allows unconditionally stable high-order modulators to dramatically decrease the quantization error's in-band power even for low oversampling ratios, i.e., high-speed designs. Since the high-order loop's stability is guaranteed, neither the maximal gain of the noise transfer function does not need to be reduced according to Lee's rule, nor careful design verified by lengthy numerical analysis is necessary.

[3] A ± 1 alternating sequence applied to $(1 - z^{-1})^N$ leads to 2^N, that is, to N-bit output.
[4] The comparative hardware and power efficiency will be expressed/verified soon.

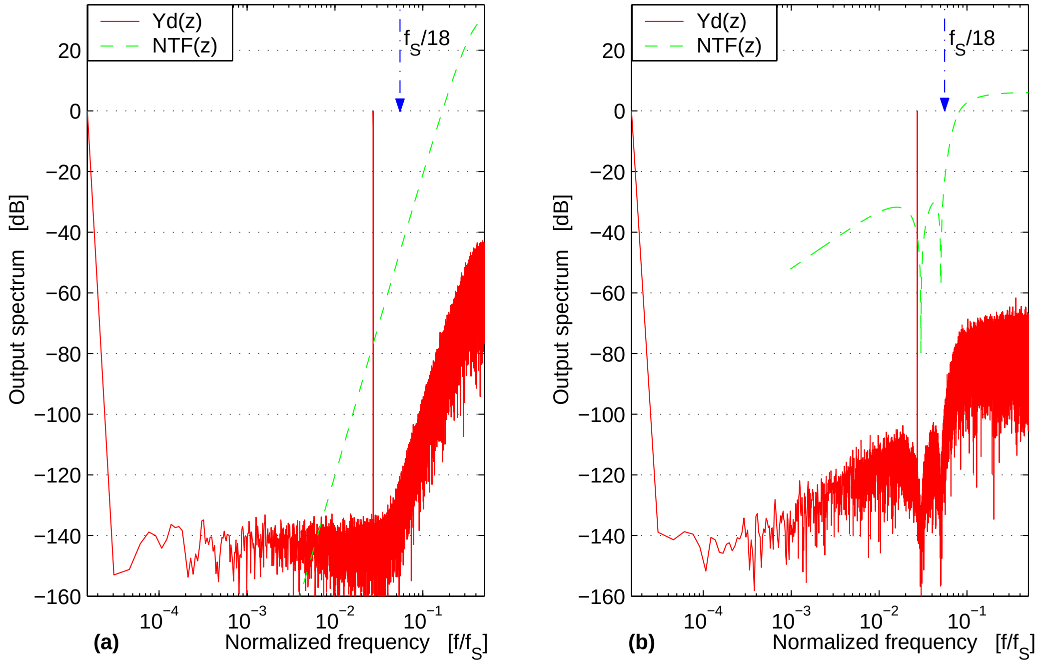

Figure 2: Simulated output spectrum of a 5th-order 6-bit digital $\Delta\Sigma$ modulator [$f_S/18$ marks the signal band's limit for $OSR = 9$]: **(a)** error-feedback topology, $NTF(z) = (1-z^{-1})^5 = \frac{1-5z^{-1}+10z^{-2}-10z^{-3}+5z^{-4}-z^{-5}}{1}$, $SNR = 102.5$ dB; **(b)** chain of accumulators, $NTF(z) = \frac{1-4.9z^{-1}+9.6z^{-2}-9.6z^{-3}+4.9z^{-4}-z^{-5}}{1-3.6z^{-1}+5.2z^{-2}-3.9z^{-3}+1.5z^{-4}-0.2z^{-5}}$, $SNR = 80.7$ dB.

4 Simulation results

To illustrate the behavior of the proposed high-order delta-sigma DAC, a 5th-order structure with $NTF(z) = (1-z^{-1})^5$ was simulated. As expected, it remained stable for several million (2^{24}) samples. A 2^{16}-point FFT of the 6-bit output data stream y_d is shown in Fig. 2.(a). The full-scale input x_d was quantized to $k_x = 16$ bits. Also, a 1-LSB dither was used to prevent idle tones for dc inputs [14, 15]. Since the 6-bit truncation error was aggressively pushed out of band with the 5th-order $NTF(z)$, a signal-to-noise ratio of 102.5 dB was obtained even for a low value of the oversampling ratio of 9.

Fig. 2.(b) shows the output spectrum of a DAC designed under the same conditions, but using a chain of accumulators topology (Fig. 1.(b)). The 5th-order $NTF(z)$ was designed using Schreier's toolbox [16] with optimized zeros and a maximum gain of 2. This modulator achieves 80.7 dB signal-to-noise ratio, 20 dB lower than the proposed architecture. Also note that Lee's rule is not a guarantee of stability, while the proposed modulator is unconditionally stable.

5 Conclusions

In this paper unconditionally stable high-order $\Delta\Sigma$ DACs were designed based on an analytical criterion. This novel criterion states a trade-off between the order of the loop filter and the bit length of the output data stream. Such error-feedback DACs are more robust and power efficient than previous designs. Due to aggressive noise shaping, as simulations showed, they can achieve high resolution and high speed simultaneously.

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References

[1] Bo Zhang, *Delta-Sigma Modulators Employing Continuous-Time Circuits and Mismatch-Shaped DACs*, Ph.D. thesis, Oregon State University, Department of Electrical and Computer Engineering, 1996, chapter The Delta-Sigma Overview, available via anonymous ftp at ftp://next242.ece.orst.edu/pub/ZhangCh6.ps.Z.

[2] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*, New York: IEEE Press, 1996.

[3] Wai Laing Lee, "A novel higher-order interpolative modulator topology for high resolution oversampling A/D converters," M.S. thesis, Massachusetts Institute of Technology, Cambridge, MA,, June 1987.

[4] K. Chao, S. Nadeem, W. L. Lee, and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 3, pp. 309–318, March 1990.

[5] T. Ritoniemi, T. Karema, and H. Tenhunen, "The design of stable high order 1-bit sigma-delta modulators," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 1990, pp. 3267–3270.

[6] D. A. Kerth, D. B. Kasha, T. G. Mellissionos, D. S. Piasecki, and E. J. Swanson, "A 120dB linear switched-capacitor delta-sigma modulator," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 1994, pp. 196–197.

[7] C. D. Thompson and S. R. Bernadas, "A digitally-corrected 20b delta-sigma modulator," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 1994, pp. 194–195.

[8] W. Rhee, A. Ali, and B. Song, "A 1.1GHz CMOS fractional-N frequency synthesizer with a 3b 3rd-order delta-sigma modulator," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2000, pp. 198–199.

[9] H. G. Musmann and W. Korte, "Generalized interpolative method for digital/analog conversion of PCM signals," U.S. Patent 4,467,316, August 21, 1984.

[10] P. J. Naus, E. C. Dijkmans, E. F. Stikvoort, A. J. McKnight, D. J. Holland, and W. Bradinal, “A CMOS stereo 16-bit D/A converter for digital audio,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 390–395, June 1987.

[11] S. Willingham, M. Perrott, B. Setterberg, A. Grzegorek, and B. McFarland, “An integrated 2.5GHz delta-sigma frequency synthesizer with 5μs settling and 2Mb/s closed loop modulation,” in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, February 2000, pp. 200–201.

[12] U. Moon, J. Silva, J. Steensgaard, and G. C. Temes, “A switched-capacitor DAC with analog mismatch correction,” in *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2000, vol. 4, pp. IV.421–IV.424.

[13] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, and T. Yoshitome, “A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 12, pp. 929–934, December 1987.

[14] M. H. Perrott, T. L. Tewksbury, and C. G. Sodini, “A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation,” *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2048–2060, December 1997.

[15] N. M. Filiol, T. A. D. Riley, C. Plett, and M. A. Copeland, “An agile ISM band frequency synthesizer with built-in GMSK data modulation,” *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 998–1008, July 1998.

[16] Richard Schreier, “The delta-sigma toolbox 5.1 for Matlab 5.0,” Matlab code and documentation, April 1998, available via anonymous ftp at ftp://next235.ece.orst.edu/pub/delsig.tar.Z.