Performance Characterization of Mixed-Signal Circuits Using a Ternary Signal Representation

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Abstract

Signatures used in low-cost schemes for testing analog and mixed-signal circuits do not directly represent or characterize the behavior of the device-under-test (DUT), since the lossy compression or complicated mathematical relations used can result in the loss of physical performance information. We develop a novel scheme where the signature is generated by built-in circuits based on a Ternary Signal Representation (TSR), which represents the behavior of a signal with three levels, positive, zero, and negative. The signatures can be used directly to characterize DUTs or can be manipulated to obtain widely accepted dynamic performance parameters, such as SNR, THD, etc. Simulation results on a $\Delta\Sigma$ DAC and a $\Delta\Sigma$ ADC using TSR signatures through built-in circuits are presented to show the feasibility of the proposed method.

1 Introduction

The advent of wireless communication systems and the rapid growth of the multi-media market have increased the importance of research into cost-effective tests for mixed-signal devices. Moreover, Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) are common modules on many mixed-signal chips, since they provide the interface between the outside (analog) world and the digital circuit on the chip. Thus, testing ADCs and DACs becomes a crucial part of the overall test strategy.

In order to characterize an on-chip ADC and a DAC (ADC/DAC) in mixed-signal devices, we could use an oscilloscope or a spectrum analyzer or expensive *ad hoc* test schemes. However, these would result in high test cost and are time-consuming. As an approach to overcome these problems, it has been widely accepted that Built-in Self-Test (BIST) circuitry generating on-chip signatures is an efficient solution [1, 2]. The on-chip signatures compress or represent the output responses of the ADC/DAC.

Most signatures do not directly represent or characterize the behavior of a device-under-test (DUT) due to lossy compression or high degree of dependence on mathematical relations, such as correlation and regression. In [3], the oscillation frequency of the DUT was used to detect catastrophic or parametric faults. However, the variation of the oscillation frequency may not accurately represent the amount of variation of the DUT performance. In [4], though signatures generated by pseudo-random stimuli can be used for fault detection through the use of arithmetic operations (such as auto-correlation and cross-correlation), performance characterization is difficult due to their high dependency on mathematical relations that can lose physical performance information. In [5], while it is possible to predict the DUT performance using DUT signatures generated by an optimized test stimulus, it is difficult to measure harmonic distortion or noise effects that are used to characterize the dynamic performance of the DUT.

In this paper, we propose a Built-In Self-Test technique using a Ternary Signal Representation (TSR) in order to realize cost-effective test. With TSR, we obtain signatures that can represent the behavior of a DUT very well. We use ADC and DAC testing as examples to demonstrate our approach. The organization of this paper is as follows. We review the characterization of dynamic performance of ADC/DAC in Section 2. The basic concepts of our method are explained in Section 3. Section 4 shows the application of our proposed method to on-chip converters and simulation results are shown in Section 5. Finally, conclusions are drawn in the last section.

2 Review of dynamic performance characterization of ADC/DAC

The dynamic performance of ADC/DAC includes Signal-to-Noise Ratio (SNR), Signal to Noise and Distortion Ratio (SNDR), Total Harmonic Distortion (THD), Effective Number Of Bits (ENOB), etc. The dynamic performance can be estimated through an FFT in a spectral test with sinusoidal inputs [6]. SNR is the ratio of the signal amplitude to noise level or the ratio of signal power to the non-signal power as given by

$$SNR = 20\log\frac{Vsignal_{RMS}}{Vnoise_{RMS}} = 10\log\frac{Psignal_{avg}}{Pnoise_{avg}} \quad (1)$$

In SNR calculation, the harmonic distortion due to the nonlinearities of ADC/DAC is usually excluded. When harmonic distortion is included in SNR estimation, it is referred to as SNDR or SINAD. THD is the RMS sum of all harmonics and generally given by

$$\begin{aligned} THD &= 20\log\frac{Vh_{RMS}}{Vf_{RMS}} \\ &= 20\log\frac{\sqrt{Vh_{even}^2 + Vh_{odd}^2}}{Vf_{RMS}} \end{aligned} \quad (2)$$

where Vh_{even} is the amplitude of even harmonics, Vh_{odd} is the amplitude of odd harmonics, and Vf is the amplitude of the fundamental signal. ENOB is related to the SNR as given by

$$ENOB = \frac{SNR - 1.76}{6.02} \quad (3)$$

In fact, ENOB can be defined using the SNDR instead of SNR.

3 Signature based on Ternary Signal Representation

Due to the nature of analog signals, it is difficult to obtain a test signature which is exactly the same as that from an ideal expected signal. Furthermore, the analysis of analog signals is more difficult due to the error caused by preprocessing stages, such as the digitization of the analog signal. Thus more accurate analysis requires more complex and expensive digitizers. To overcome this problem we propose an analysis based on a Ternary Signal Representation (TSR).

3.1 Signals with harmonics and noise

The output of an ADC/DAC can be written as the sum of signals and noise. If the ADC/DAC shows nonlinear behavior, it generates harmonic distortion when a pure input signal is applied to the system. The resultant output equation can be expressed in the time domain as follows.

$$\begin{aligned} f(t) &= a_0 - (a) \\ &\quad + \sum_{n=1}^{\infty} a_n sin(n\omega_0 t) + \sum_{n=1}^{\infty} b_n cos(n\omega_0 t) - (b) \\ &\quad + n(t) - (c) \end{aligned} \quad (4)$$

where ω_0 is the frequency of the fundamental signal. This equation has three terms, DC bias ((a)), a fundamental input signal and harmonics ((b)), and additive noise ((c)). The harmonics, which are the integer multiples of the tones present in the input signal, produce the distortion of the fundamental signal that is correlated with the tones. In harmonic distortion, there are two types, that is, even-order harmonic distortion and odd-order harmonic distortion. Even-order distortion is caused by asymmetrical non-linearities, such as faulty circuits, asymmetrical or unbalanced bias signals, etc. The generated even order harmonics can change the duty cycle and result in DC offset or destruction of the input signal. Odd-order distortion is produced by symmetrical non-linearities and is represented by shaping the resultant output to have sharper transitions at zero crossings in the fundamental signal without affecting the duty cycle of the resultant output.

The noise sources in the converters are quantization noise, circuit noise, clock jitter, etc. Circuit noise includes thermal noise, $1/f$ noise, noise due to the resistive polysilicon gate and the distributed substrate resistance, shot noise associated with the leakage current, etc. These noise sources cause errors that are not directly related to the input signal.

3.2 Dynamic Performance Parameter Extraction

3.2.1 Even-order harmonic distortion

Assume that a one-tone sine wave having zero DC bias is applied to an ADC/DAC which has non-linearities causing even-order harmonic distortion. Then Equation 4 can be rewritten by a Taylor expansion as follows [7].

$$f(t) = \alpha_1 Asin(\omega_0 t) + \alpha_2 A^2 sin^2(\omega_0 t) + \alpha_4 A^4 sin^4(\omega_0 t) + \cdots \quad (5)$$

where A is the amplitude of an input signal and α_1, α_3, and α_5 determine the amplitude of the harmonics. This

produces a waveform with a different duty cycle which is not symmetrical, and destroys the fundamental waveform. To illustrate this even-order distortion, we set α_1, which is the amplitude of the fundamental signal to 1 and limit the first two even harmonics having an amplitude 1/8 the fundamental. The resultant waveform is shown in Figure 1. A DC offset (f_{avg}) caused by this distortion is determined by the average value in the time domain that can be calculated using the following Equation 6.

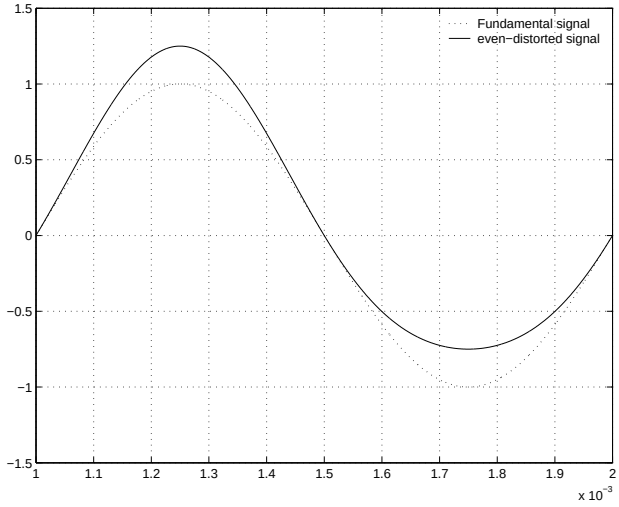

Figure 1. Even order harmonic distortion

$$f_{avg} = \frac{1}{T}\int_0^T f(t)dt \tag{6}$$

where T is the period of the fundamental waveform. Using the calculated DC offset, the degree of the asymmetry in this distortion (f_{asy}) can be estimated by the ratio of the positive portion (PP) to the negative portion (NP) relative to the DC offset in the waveform.

$$f_{asy} = \frac{PP(f(t) - f_{avg})}{NP(f(t) - f_{avg})} \tag{7}$$

3.2.2 Odd-order harmonic distortion

Assume that a one-tone sine wave having zero DC bias is applied to an ADC/DAC which has non-linearities causing odd-order harmonic distortion. Then equation 4 can be rewritten as follows.

$$f(t) = \alpha_1 A sin(\omega_0 t) + \alpha_3 A^3 sin^3(\omega_0 t) + \alpha_5 A^5 sin^5(\omega_0 t) + \cdots \tag{8}$$

where A is the amplitude of an input signal, and α_1, α_3 and α_5 determine the amplitude of the harmonics. This produces a waveform that is wider at the top and bottom. The resultant waveform has sharper transitions at zero crossings maintaining the symmetry of the waveform as a square wave. To illustrate this odd-order distortion, we set α_1, which is the amplitude of the fundamental signal, to 1 and limit the first two odd harmonics having an amplitude 1/8 the fundamental. The resultant waveform is shown in Figure 2. For a sine wave the highest slope of the signal occurs at the zero crossings. This slope can represent how odd harmonics distort the fundamental signal. The slope (f_{slp}) is defined as the derivative,

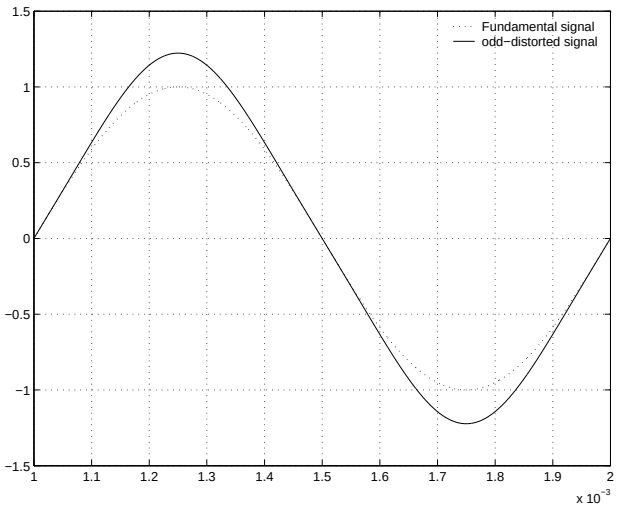

Figure 2. Odd order harmonic distortion

$$\begin{aligned} f_{slp} &= \frac{df(t)}{dt}|_{\omega_0 t = 2\pi n} \\ &\simeq (\alpha_1 A + \alpha_3 A^3 + \cdots)\omega_0 \end{aligned} \tag{9}$$

It should be noted from Equation 8 that higher f_{slp} means more distortion.

3.2.3 Noise effect

Assume that a one-tone sine wave having zero DC bias is applied to an ADC/DAC which has additive noises ($n(t)$). Then equation 4 can be rewritten as follows.

$$f(t) = a_1 sin(\omega_0 t) + n(t) \tag{10}$$

If $n(t)$ are random noise values, the amplitude distributions are Gaussian. These noise values are superimposed on the fundamental signal. The resultant output waveform at a given amplitude also shows a Gaussian distribution. Then the width of the Gaussian distribution corresponds to the RMS noise. The width of the Gaussian distribution can be represented by the standard deviation (σ) that corresponds

to the half width of the peak at about 60% of the full height, as can be calculated from Equation 11.

$$P(x) = \frac{1}{\sigma\sqrt{2\pi}} exp(-\frac{(x-\mu)^2}{2\sigma^2}) \quad (11)$$

where μ and σ are the mean and standard deviation of the distribution. In the case of odd-order harmonic distortion and noise effects, we first estimate the zero crossing time (t_{ZX}) of the fundamental signal. In fact, t_{ZX} is the average value with a variance. The variance can be seen as noise effects if we assume that most noise is random and additive. In addition, the variance will occur in a similar way at any given voltage level of the fundamental signal. Thus $n(t)$ in Equation 10 can expressed as the following equation.

$$n(t) = t_{ZX0} + \Delta t_{ZX} \quad (12)$$

where t_{ZX0} is the average value of the fundamental signal. The RMS noise can be calculated as

$$n_{RMS} = \sqrt{(\frac{1}{2N}\sum_{i=1}^{2N}(t_{ZX}(i) - t_{ZX0})^2)} \quad (13)$$

where N is the number of cycles of the fundamental signal. Figure 3 shows the output of ADC/DAC in the presence of harmonic distortion and noise.

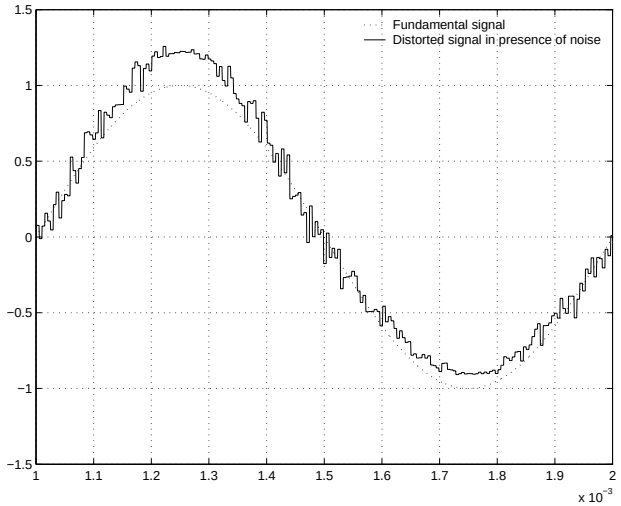

Figure 3. The output of ADC/DAC in presence of harmonic distortion and noise

3.3 Signature Generation

In order to measure the parameters mentioned earlier using BIST, modification of the equations for the parameters is required since the measurement is limited by the BIST. The limitation can produce measurement error. Techniques to minimize the measurement error can lead to complexity in the BIST implementation. However, our proposed on-chip signatures, Ternary-Signal-Representation (TSR), can achieve cost-effective BIST with much less measurement error. In TSR there are three portions, positive, zero, and negative portions. The reference voltage for the positive portion ($Vref_P$) can be any voltage between the maximum voltage and the average voltage of a given input signal, the reference voltage for the zero level ($Vref_Z$) is the average voltage, and the reference voltage for the negative portion ($Vref_N$) can be any voltage between the minimum voltage and the average voltage of a given input signal. In fact, these reference voltages can affect the accuracy of TSR. This will be discussed in Section 5. To illustrate TSR, an example of a one tone sine wave having zero DC bias is shown in Figure 4.

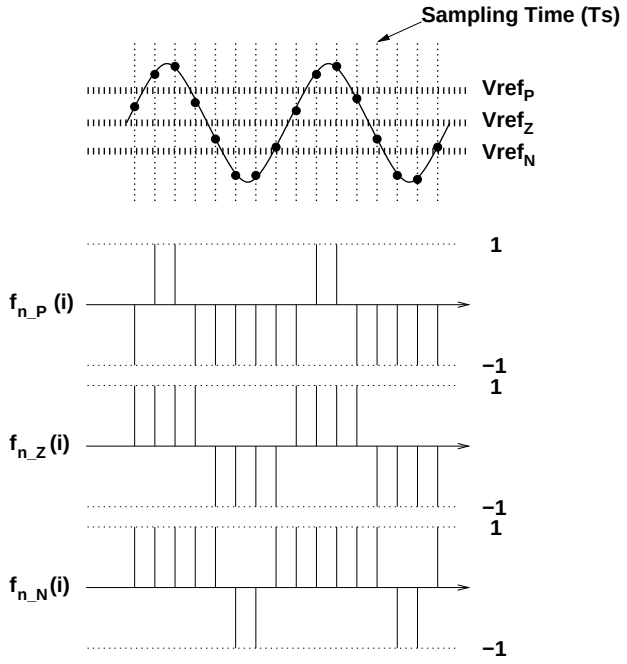

Figure 4. TSR representation of a one tone sine wave having zero DC bias

In the case of the generation of the signatures representing odd-order harmonic distortion and noise effects, we first estimate zero crossing time (t_{ZX}) of the fundamental signal. The zero crossing times (t_{ZX}) can be determined by $PP(f_{n\_Z}(i-1))$ exclusive-ORed with $NP(f_{n\_Z}(i))$ as shown in Figure 5. The t_{ZX0} can be calculated based on the zero crossing times of the fundamental signal and compared with t_{ZX} to calculate RMS noise using Equa-

tion 13. The slope at the zero crossings is estimated using f_{n_P} exclusive-ORed with f_{n_N} as given in Equation 14.

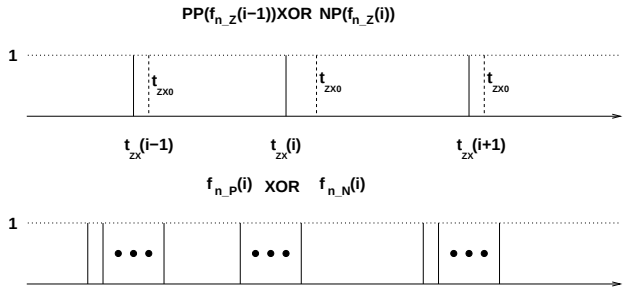

Figure 5. The slope at zero crossing

$$f_{slp} = \frac{Vref_P - Vref_N}{NO(f_{n\_P} XOR f_{n\_N})T_S} \quad (14)$$

where T_S is the sampling rate and NO is the number of ones in the sampling data.

The signatures representing even-order harmonic distortion, f_{avg} and f_{asy}, can be generated as follows.

$$f_{avg} = f_{slp} T_s \frac{\sum_{i=1}^{NS}(f_{n\_P}(i) + f_{n\_Z}(i) + f_{n\_N}(i))}{3} \quad (15)$$

$$\begin{aligned} f_{asy} &= \frac{\sum_{i=1}^{NS} PP(f_{n\_Z}(i))}{\sum_{i=1}^{NS} NP(f_{n\_Z}(i))} + \frac{\sum_{i=1}^{NS} PP(f_{n\_N}(i))}{\sum_{i=1}^{NS} NP(f_{n\_P}(i))} \\ &\quad + \frac{\sum_{i=1}^{NS} PP(f_{n\_P}(i))}{\sum_{i=1}^{NS} NP(f_{n\_N}(i))} \end{aligned} \quad (16)$$

where NS is the number of samplings.

3.4 Characterization of dynamic performance using signatures

The signatures generated by TSR can be used directly to characterize ADC/DAC or to obtain widely accepted dynamic performance parameters, such as SNR, THD, etc. The amplitude of harmonics is estimated with f_{slp} and f_{avg}. Odd harmonic distortion is mostly reflected in f_{slp} and even harmonic distortion can be represented by f_{avg}. To calculate the amplitude of harmonics due to the variation of f_{slp} (Vh_{odd}), f_{slp_ref} is subtracted from the estimated f_{slp} and this difference is divided by fundamental frequency ω_0 (Equation 9) as given by

$$Vh_{odd} = \frac{f_{slp} - f_{slp\_ref}}{\omega_0} \quad (17)$$

The amplitude of even harmonics (Vh_{even}) can be represented by f_{avg}. With Vh_{odd} and Vh_{even}, the RMS amplitude of harmonics can be estimated as follows.

$$Vh_{RMS} = \sqrt{Vh_{even}^2 + Vh_{odd}^2} \quad (18)$$

In order to obtain widely accepted dynamic performance parameters, it is necessary to adjust $Vsignal_{RMS}$ and Vf_{RMS} as follows.

$$Vsignal_{RMS} = Vf_{RMS} = \beta_1 A + \beta_2 Vh_{odd} \quad (19)$$

where A is the amplitude of an input signal and β_1 and β_2 are gain adjust factors for the amplitude of a fundamental frequency in an output signal, $Vsignal_{RMS}$ or Vf_{RMS}. β_1 is determined by a gain error of the DUT, which can be obtained through static tests, and β_2 is estimated by the amount of odd harmonics. In order to simplify the estimation example of β_2, assume that input signal is $Acos(\omega_0 t)$ and distortion effect is limited to third-order harmonics [7].

$$\begin{aligned} f(t) &= \alpha_1 Acos(\omega_0 t) + \alpha_2 A^2 cos^2(\omega_0 t) + \alpha_3 A^3 cos^3(\omega_0 t) \\ &= \alpha_1 Acos(\omega_0 t) + \frac{\alpha_2 A^2}{2}[1 + cos(2\omega_0 t)] \\ &\quad + \frac{\alpha_3 A^3}{4}[3cos(\omega_0 t) + cos(3\omega_0 t)] \end{aligned} \quad (20)$$

Then from Equation 20, we can extract the amplitude of the fundamental frequency as

$$Vsignal_{RMS} = Vf_{RMS} = \alpha_1 A + \frac{3\alpha_3 A^3}{4} = \alpha_1 A + 3Vh_{odd} \quad (21)$$

By comparing Equation 21 and Equation 19, we can obtain β_1 and β_2. The RMS amplitude of noise can be calculated using Equation 13. These calculated RMS amplitudes are plugged into Equations 1, 2, and 3.

4 DSP-based test for on chip converters

Reconfiguration of a mixed-signal chip using built-in circuitry is required to realize the ADC/DAC test with TSR signatures as shown in Figure 6.

The test controller in the figure consists of non-overlapping clock generators and can be provided externally. A Signature Generator (SG) should be simple and implemented with small area overhead in order to achieve cost-effective test. The signature generator consists of multiplexers, comparators, interconnection wires, etc., as shown in Figure 7. The major contribution to the area overhead is the comparator. In [9, 10], low cost comparators are introduced. In fact, the accuracy of our proposed method

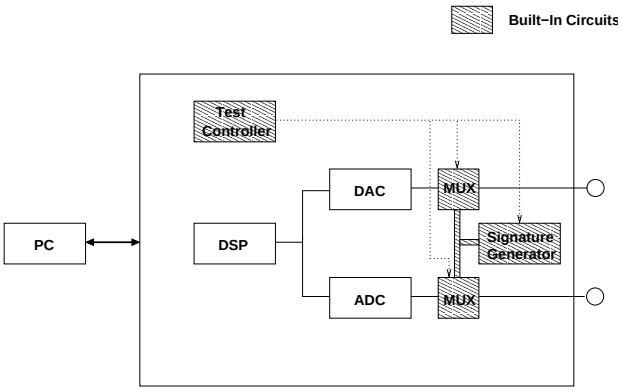

Figure 6. The reconfiguration of a mixed-signal chip for ADC/DAC test

depends on the speed of comparator, that is, the sampling rate of the SG. While a higher speed comparator means more accurate test, it is more expensive to implement BIST. Therefore, we need to decide on the sampling rate based on a trade-off between test accuracy and test cost. The reference voltages $Vref_P$, $Vref_Z$, and $Vref_N$ can be provided externally or be internally generated. For testing the ADC these reference voltages are digital values and signature generation can be performed by a DSP or PC. The collected data from the SG can be post-processed by a DSP [8] or a PC to obtain f_{slp} , f_{avg}, and f_{asy}. The DSP processor first generates a digital input stimulus and feeds the signal out for DAC testing. After DAC testing, the converted analog signal by the tested DAC is loop-backed to the ADC and digitized. The digitized signal is transferred to the DSP processor. The ADC/DAC conversion and the transmission to the DSP are done in real-time so that any communication between the PC and the DSP will not interrupt the real-time operation. In fact, the PC is used for post-processing or debugging the system.

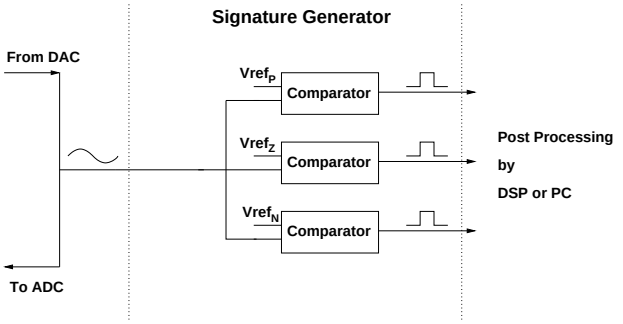

Figure 7. Signature Generator

In ADC testing, input compensation based on DAC testing results is required to implement accurate test. The dynamic performance of an ADC can be expressed as a function of the performance of an ADC, a DAC, and a SG,

$$Perf(ADC(Perf(DAC) + Perf(SG))) \quad (22)$$

where $Perf$ is one the performance parameters. If we assume that there is low performance degradation and low area overhead due to the SG, the last term in Equation 22 can be neglected. Perf(DAC) is reflected to Equation 19. $Vsignal_{RMS}$, Vf_{RMS}, and Vh_{RMS} are compensated as

$$Vsignal_{RMS} = Vf_{RMS} = \beta_1 A + \beta_2 Vh_{odd}(1+\Delta) \quad (23)$$

$$Vh_{RMS} = \frac{\Delta}{\beta_2}\sqrt{Vh_{even}^2 + Vh_{odd}^2} \quad (24)$$

Δ is estimated with SNDR of the tested DAC as follows.

$$\Delta = \pm 10^{\frac{|100 - SNDR_{DAC}|}{20}} \quad (25)$$

The sign of Δ is determined by the sign of $100 - SNDR_{DAC}$. With the compensated $Vsignal_{RMS}$, Vf_{RMS}, and $Vsignal_{RMS}$ the characterization of the ADC is performed.

5 Simulation Results

On-chip converters with 2^{nd} order $\Delta\Sigma$ converters were modeled and simulated using Matlab with SIMULINK. The modeled $\Delta\Sigma$ converters had audio bandwidths (BW=20 – 20kHz) and their oversampling ratio (OSR) was 256. The sampling frequency (f_s) was 11,264 kHz, which can be calculated by $2 \cdot BW \cdot OSR$. A 1kHz single-tone sine wave digitized to 16-bit codes was used as an input stimulus to the digital $\Delta\Sigma$ modulator.

In simulation, the first four even harmonics and the first four odd harmonics were added to the simulation model to emulate harmonic distortion. The combination of harmonics was determined by Monte Carlo simulation. In addition, random noise was added to the simulation model in order to include noise effects. Figure 8 shows how f_{slp}, f_{avg}, and f_{asy} of a DAC are correlated with the expected amount of harmonics. As can be seen in this figure, these signatures are linearly related with the amount of harmonics. While there are estimation errors, the estimated amount of harmonics is linearly related with the expected amount of harmonics as shown in Figure 9.

The estimated RMS noise from Equation 13 is also linearly related with the expected amount of noise as seen in

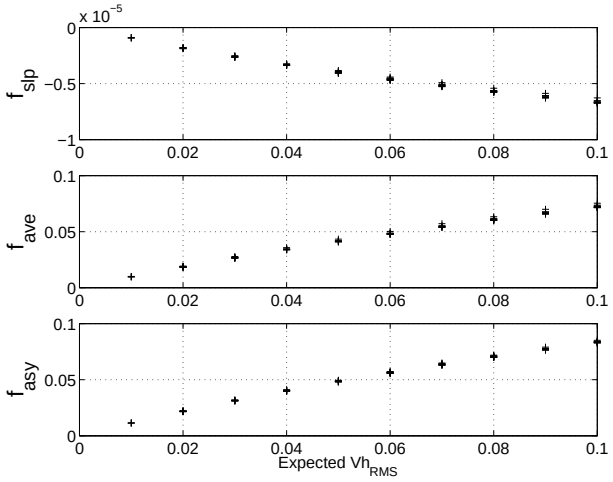

Figure 8. The Extraction of harmonics from signatures based on TSR

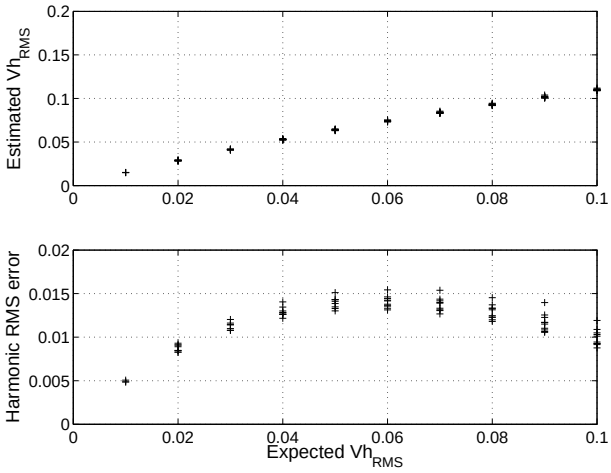

Figure 9. The estimated RMS harmonics vs the expected RMS harmonics

Figure 10. The RMS noise estimation also shows calculation errors. These errors are related to the sampling rate and reference voltages.

The higher $Vref_P$ or the lower $Vref_N$ shows less errors in the calculation of the harmonics. This is caused by the fact that the distortion effect of the top or bottom portion of a signal is larger than the other portions as shown in Figure 11. The higher sampling rate provides more accurate test as shown in Figure 11, but the sampling rate is limited by the speed of the comparator.

In order to estimate widely accepted dynamic performance parameters of the DAC, such as SNR, SNDR, THD, and ENOB, we determined β_1 and β_2 through simulation and estimation. With these values, the comparison between the estimated and the expected dynamic performance was performed. For SNR comparison, the estimation error increases monotonically except with a much lower noise range as shown in Figure 12. In the THD comparison case, the estimated THD is well correlated with the expected THD and the estimation error is randomly distributed. The comparison with the SNDR case shows similar results as the case with the THD, except with less random error as shown in Figure 13.

The standard deviations from the expected dynamic performance parameters of the DAC are shown in Table 1.

Table 1. The estimation error of DAC [dB]

SNR	SNDR	THD
1.81±1.30	1.20 ±1.26	0.59 ± 0.42

To estimate dynamic performance parameters of an ADC, the SNDR result of the DAC is used with Equation 25 and 24. In this paper, we extracted the SNDR of the ADC and the results are shown in Figure 15 and Table 2.

Table 2. The estimation error in SNDR extraction [dB]

	DAC	ADC
SNDR	1.87 ± 1.11	1.63 ± 0.93

6 Conclusions

In this paper, we presented a novel signature for testing analog and mixed-signal circuits. The signature is generated by built-in circuits based on a Ternary Signal Representation (TSR), which represents the behavior of a signal with three levels, positive, zero, and negative. The signatures can be used directly to characterize DUTs or can be manipulated to obtain widely accepted dynamic performance parameters, such as SNR, THD, etc. Simulation results show that the estimation error is less than 3 dB (0.5 bit error in resolution bit for converters). The proposed method does not depend on circuit types and thus can be applied to general mixed-signal circuits.

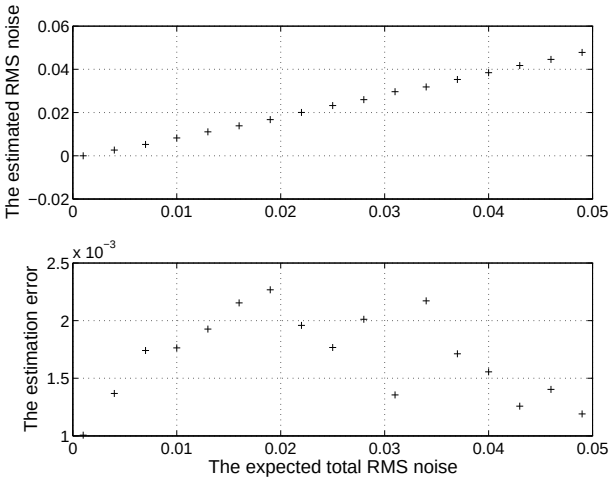

Figure 10. The extraction of RMS noise from signatures based on TSR

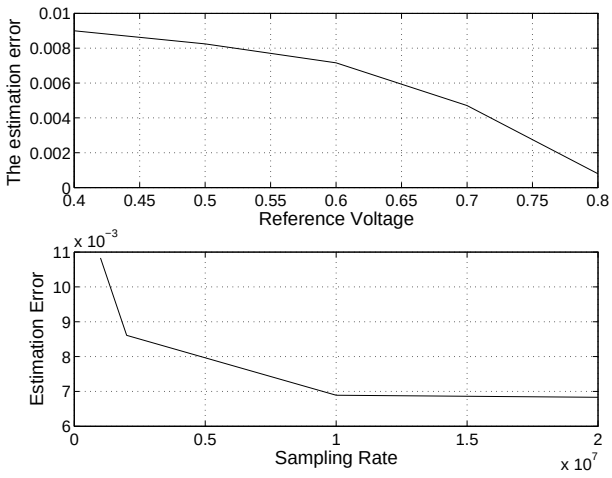

Figure 11. The estimation error with reference voltage and sampling rate

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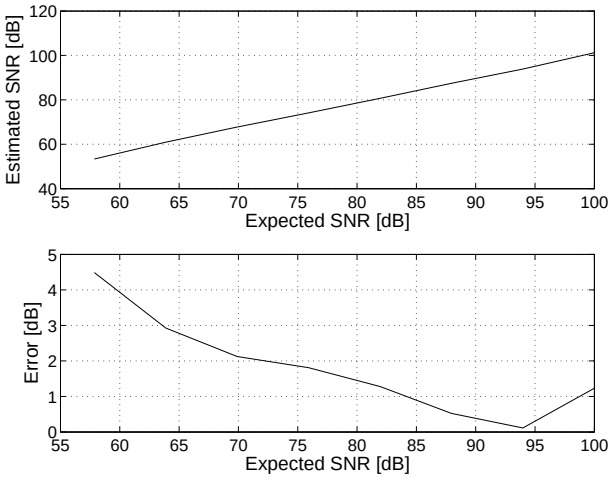

Figure 12. The estimated SNR vs the expected SNR

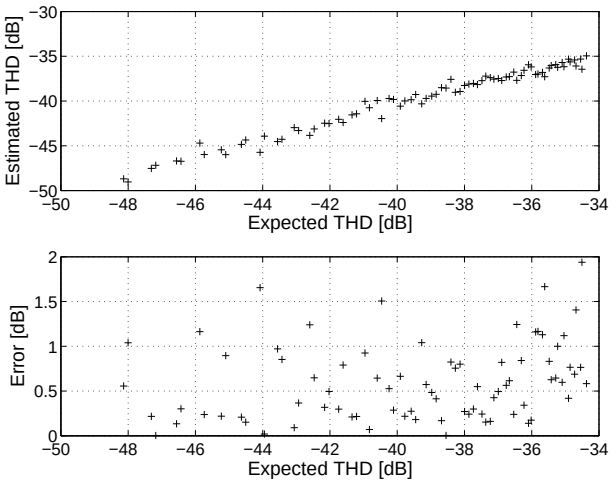

Figure 14. The estimated THD vs the expected THD

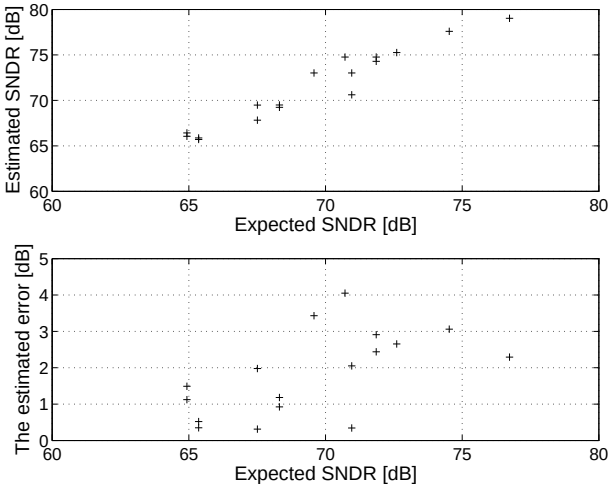

Figure 13. The estimated SNDR vs the expected SNDR

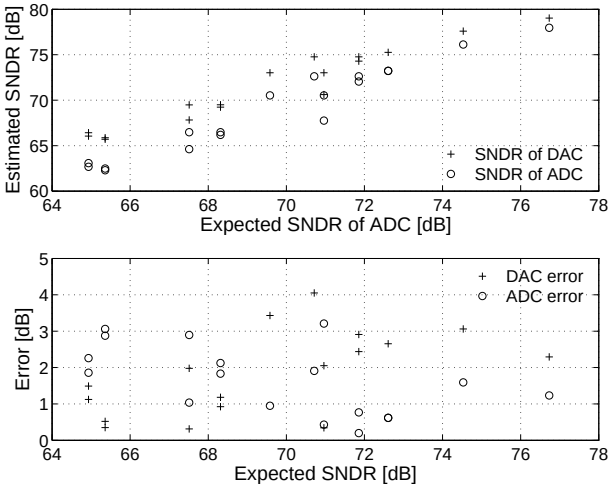

Figure 15. The estimated SNDR of an ADC and a DAC