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640 Gbit/s OTDM Lab-Transmission and 320 Gbit/s Field-Transmission with SOA-based Clock Recovery

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Abstract: We demonstrate low-jitter 40GHz baserate clock recovery from 640Gbit/s OTDM-data after 50km lab-transmission, using a potentially integrable injection-locked loop circuit with SOA-based phase-comparison at low data-powers. A 54.3km field-transmission test at 320Gbit/s is also performed.

OCIS codes: (060.2330) Fiber optics communications; (060.4510) Optical communications.

1. Introduction

Clock recovery (CR) is the essential functionality which allows a receiver to synchronize to a transmitted data signal in an optical communication system. In a network based on optical time-division multiplexed (OTDM) data signals, the CR circuit must extract a clock at the baserate, which is the repetition rate of the individual data channels constituent of the OTDM signal. This requires an optical phase comparison between the received OTDM signal and the locally generated clock signal. Such a phase comparator must have a very high timing-resolution, i.e. lower than the bit-slot duration which in the case of a 640 Gbit/s OTDM signal is ~1.5 ps. Earlier demonstrations of clock recovery from high-speed data signals have exploited a.o. four-wave mixing in a laser-diode amplifier at 400 Gbit/s [1], electroabsorption at 320 Gbit/s [2], and filtered chirp from an SOA at 320 Gbit/s [3]. It has been demonstrated that a semiconductor optical amplifier (SOA) can exhibit a time-response faster than ~1 ps when it is assisted by filtered chirp, which has been used for demultiplexing from 640 Gbit/s [4]. The advantages of an SOA is further that it can be integrated, its stability, and that it requires low optical power for switching.

In this paper, we perform 50 km lab-transmission of a 640 Gbit/s on-off keyed (OOK) OTDM data signal and subsequent clock recovery of the 40 GHz baserate clock by using a potentially integrable clock recovery circuit. It is an injection-locked loop containing an SOA as optical phase comparator, a Gunn oscillator, and a pulse source. Phase-noise measurements on the electrical clock from the Gunn oscillator result in very low timing jitter values, both for short and long PRBS data patterns, and for low data input powers to the SOA (down to -6 dBm). To further test the robustness of the CR circuit against phase perturbations, it is used after transmission over a 54.3 km field-installed SMF fibre link. Due to imperfect dispersion compensation of the link, the bit-rate had to be lowered to 320 Gbit/s. This test also results in a successful recovery of the 40 GHz baserate clock with low jitter-values (<200 fs).

2. Operation principle and experimental set-up

The experimental set-up is shown in Fig. 1, which covers both the 640 Gbit/s lab-trial and the 320 Gbit/s field-trial.

The 640 Gbit/s data signal consists of 16 bit-interleaved 40 Gbit/s OOK-modulated channels, all at the same wavelength

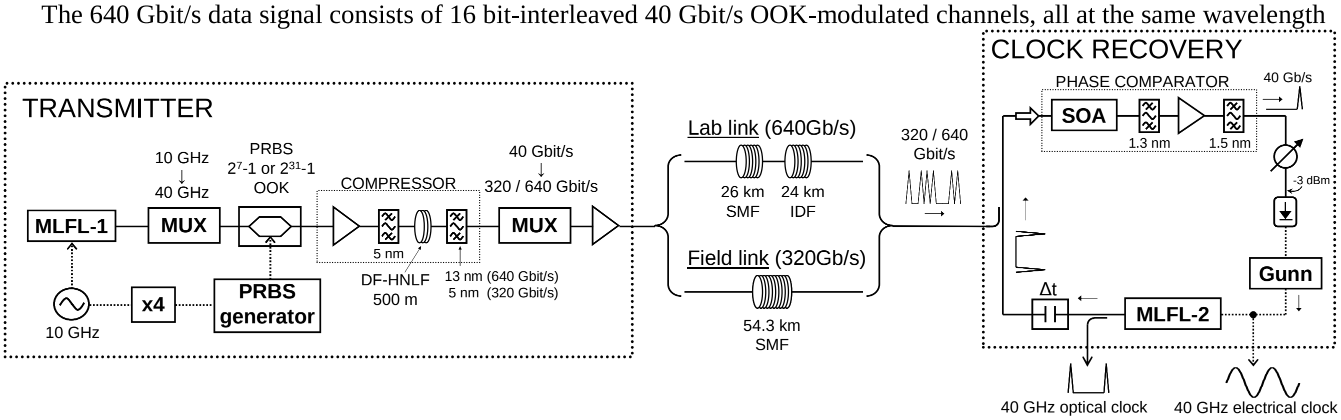


Fig. 1. Experimental set-up for the 640 Gbit/s lab-trial and the 320 Gbit/s field-trial.

and in the same polarization. It is generated as follows. A Mode-Locked Fibre Ring Laser (MLFL-1) at λ_1=1560 nm emits ~2 ps pulses at 10 GHz. These are then multiplexed up to 40 GHz by a passive fibre delay-line multiplexer (MUX). The 40 GHz pulses are OOK-modulated to 40 Gbit/s with a PRBS pattern, and then injected to a pulse compression stage. This is based on self-phase modulation (SPM) induced spectral broadening in a 500 m dispersion-flattened highly non-linear fibre (DF-HNLF) with a dispersion D=-0.36 ps/nm·km and slope 0.004 ps/nm^2·km at 1560 nm. The output of the DF-HNLF is off-carrier filtered with a 13 nm bandpass filter (BPF) centered at 1554 nm [5], as can be seen in Fig. 2 (a). The SPM in the DF-HNLF results in an up-chirping of the pulses, which are then compressed by the positive dispersion in the remainder of the transmitter, where the 40 Gbit/s pulses are multiplexed up to 640 Gbit/s by a 2^7-1 PRBS-maintaining MUX. At the output of the transmitter, the pulses are thus compressed to ~700 fs with low pedestals. The 640 Gbit/s data are then transmitted through a 50 km dispersion-managed laboratory fibre link consisting of 26 km standard single-mode fibre (SMF) and 24 km inverse-dispersion fibre (IDF). The 640 Gbit/s data before and after transmission are shown in Fig. 2 (b) and (c), respectively.

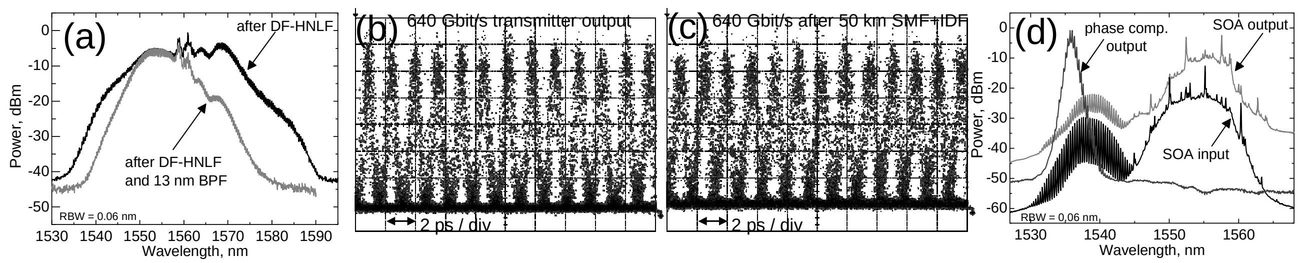
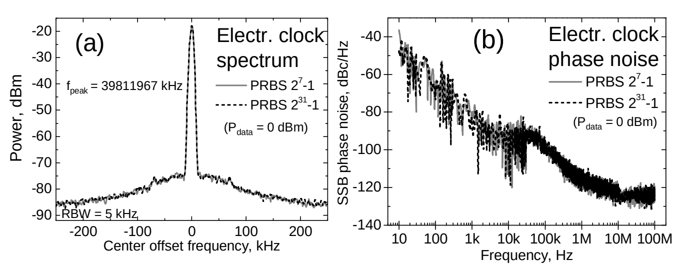


Fig. 2. 640 Gbit/s lab-trial. (a) 40 Gbit/s spectra in the compression stage, (b) 640 Gbit/s data pulses at the transmitter output, measured by a 700 GHz sampling scope, (c) 640 Gbit/s after 26km SMF+24km IDF at the input to the SOA, (d) Spectra of the input/output of the SOA showing the 640 Gbit/s data and 40 GHz probe, and spectrum of the demultiplexed 40 Gbit/s after the BPFs (phase comparator output).

The clock recovery circuit, shown in Fig. 1, is an optical injection-locked loop containing an SOA as phase comparator, a 40 GHz mode-locked fibre ring laser (MLFL-2) emitting <1 ps pulses at λ_2=1538 nm, and a Gunn oscillator in injection-locked mode. The SOA is designed with a high optical confinement for optical signal processing, and has the following characteristics: length 1.9 mm, polarization dependence 2-3 dB, small signal gain 13-14 dB, saturation output power 12 dBm, recovery time ~8 ps, and it is biased to 400 mA. The 640 Gbit/s data is coupled into the loop and injected to the SOA with an average power of only 0 dBm, together with the 40 GHz probe pulses from the MLFL-2 at -14 dBm. The data acts as a pump and modulates the SOA gain, which results in a chirping of the probe pulses. This chirp is extracted by two narrow BPFs, centered at 1536 nm, resulting in a 40 Gbit/s inverted copy of the baserate channel data onto the probe pulse train [4]. This 40 Gbit/s demultiplexed data signal is detected by a 43 GHz photodiode followed by a transimpedance amplifier. The resulting electrical 40 Gbit/s is injected into the Gunn oscillator which is in injection-locked operation. The free-running resonance frequency of the Gunn cavity is mechanically tunable, and a DC supply to the Gunn diode allows for fine-tuning. When injected with a 40 Gbit/s signal, the Gunn oscillator emits a high-quality electrical sine at 40 GHz. This is used to synchronize the MLFL-2 via an internal phase-locked loop. The CR loop length is adjusted by a variable optical time-delay Δt, in order to fulfill the phase-matching condition for the 40 GHz baserate of the incoming OTDM data signal.

3. Results

The 40 GHz clock is successfully recovered with low jitter from the 640 Gbit/s data after the 50 km SMF+IDF span.



(c) Electrical clock: integrated jitter

PRBS / P_{data}→SOA	10Hz-100MHz	100Hz-10MHz
2^7-1 / 0 dBm	149 fs	75 fs
2^7-1 / -3 dBm	139 fs	75 fs
2^7-1 / -6 dBm	132 fs	73 fs
2^{31}-1 / 0 dBm	132 fs	76 fs
2^{31}-1 / -3 dBm	134 fs	75 fs
2^{31}-1 / -6 dBm	147 fs	77 fs

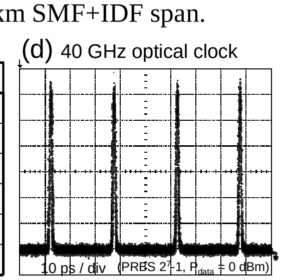


Fig. 3. Recovered 40 GHz clocks in 640 Gbit/s lab-trial. (a) Spectrum of recovered electrical clock, (b) Single side-band phase noise measurements on electrical clock when P_{data}=0 dBm, (c) Timing jitter values obtained by integrating the SSB phase noise over the intervals 10Hz-100MHz and 100Hz-10MHz for short/long PRBS and different data input powers to SOA, (d) Optical clock (MLFL-2 pulses).

Fig. 3 shows the spectrum (a), single side-band (SSB) phase noise measurements (b), and timing jitter (c) of the recovered electrical clock from the Gunn oscillator, as well as the optical clock pulses from the MLFL-2 (d). The SSB phase noise of the electrical clock was measured for PRBS 2^7-1 and 2^{31}-1 data patterns. Furthermore, the dynamic range of the CR circuit was investigated by varying the data input power to the SOA over a 6 dB range, from P_{data} = 0 dBm to -6 dBm (both for long and short PRBS). Fig. 3 (a) and (b) show the spectrum and phase noise, respectively, of the recovered electrical clock in the case of P_{data} = 0 dBm. Integration of the measured SSB phase-noise spectra over the ranges 10Hz-100MHz and 100Hz-10MHz, yields the timing jitter values shown in Fig 3 (c). These reveal the low power requirement of the CR circuit since the electrical clock jitter remains low (<150 fs) for data powers down to -6 dBm, both for long and short PRBS patterns. As another advantage, the optical clock pulses obtained from the circuit (see Fig. 3 (d)), can be used directly for demultiplexing, i.e. in another SOA [4]. The circuit has the potential for integration, since the MLFL-2 can in principle be replaced by i.e. a semi-conductor based pulse source.

A field-trial was also conducted in order to test the performance of the CR circuit in the presence of transmission-induced phase fluctuations of the incoming data signal. The experimental set-up is shown in Fig. 1. The field-installed fibre is located around the city of Eindhoven in the Netherlands, and consists of 54.3 km of standard SMF. The dispersion in the link was post-compensated by using appropriate lengths of dispersion-compensating fibre. Due to insufficient dispersion-slope compensation, it was not possible to transmit the 640 Gbit/s data, since the pulse broadening after the link was too large. The data rate was therefore lowered to 320 Gbit/s, and the data pulses before/after transmission are shown in Fig. 4 (a). Compared to the 640 Gbit/s lab-trial, there are a few minor changes in the set-up. Due to the different dispersion profile of the field-link, the wavelength allocation of MLFL-1 and -2 are changed to λ_1=1542 nm and λ_2=1563 nm. The last filter in the compression stage is a 5 nm BPF, resulting in broader ~1 ps pulses. At last, the data input power to the SOA for sufficient gain modulation is P_{data}~6 dBm, which is attributed to an asymmetry in the SOA spectral gain-profile and the broader data-pulses (lower peak-power). The results of the field-trial are shown in Fig. 4 (b-e). The 40 GHz clock is successfully recovered from the 320 Gbit/s transmitted data, both for PRBS 2^7-1 and 2^{31}-1. The spectrum and SSB phase noise of the recovered electrical clock are shown in Fig. 4 (b) and (c), respectively. Timing jitter values obtained by phase noise integration are shown in Fig. 4 (d), measured for short/long PRBS and P_{data}=6 dBm and 3 dBm. After transmission over the field-installed link, the CR circuit is able to recover the clock with a 10Hz-100MHz timing jitter lower than 200 fs (for P_{data} > 3 dBm).

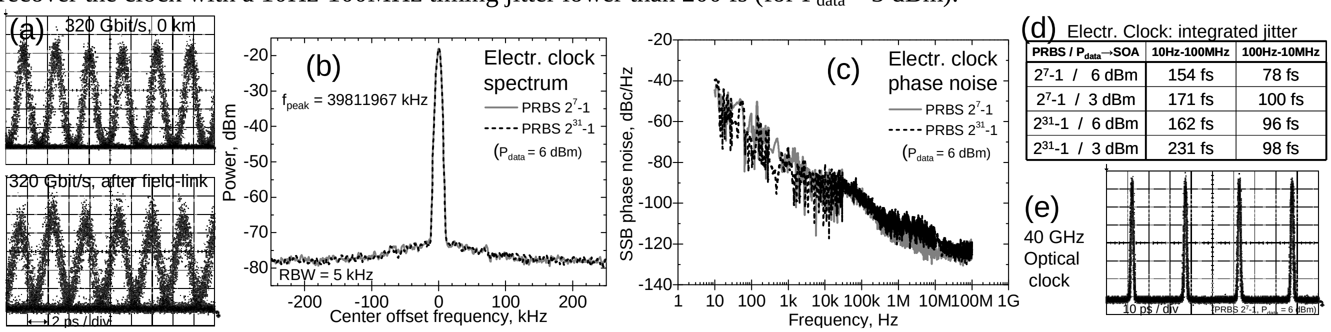


Fig. 4. Field-trial. (a) 320 Gbit/s OTDM data before and after transmission, (b) Spectrum of recovered 40 GHz electrical clock, (c) Single side-band phase noise measurements on the electrical clock, (d) Timing jitter of the electrical clock, (e) Recovered 40 GHz optical clock.

4. Conclusion

We have demonstrated 40 GHz baserate clock recovery in a 640 Gbit/s OTDM lab-transmission over 50 km. We used a potentially integrable clock recovery circuit with a high jitter-performance and low power requirements. The circuit was an injection-locked loop with a SOA as optical phase comparator. The recovered clock maintained a low jitter (<150 fs) at data input powers as low as -6 dBm. Furthermore, a field-transmission over 54.3 km of 320 Git/s data confirmed the capability of the clock recovery circuit to produce a low-jitter clock (<200 fs) in the presence of transmission-induced phase-fluctuations.

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