

Lithography for enabling advances in integrated circuits and devices

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Because the transistor was fabricated in volume, lithography has enabled the increase in density of devices and integrated circuits. With the invention of the integrated circuit, lithography enabled the integration of higher densities of field-effect transistors through evolutionary applications of optical lithography. In 1994, the semiconductor industry determined that continuing the increase in density transistors was increasingly difficult and required coordinated development of lithography and process capabilities. It established the US National Technology Roadmap for Semiconductors and this was expanded in 1999 to the International Technology Roadmap for Semiconductors to align multiple industries to provide the complex capabilities to continue increasing the density of integrated circuits to nanometre scales. Since the 1960s, lithography has become increasingly complex with the evolution from contact printers, to steppers, pattern reduction technology at i-line, 248 nm and 193 nm wavelengths, which required dramatic improvements of mask-making technology, photolithography printing and alignment capabilities and photoresist capabilities. At the same time, pattern transfer has evolved from wet etching of features, to plasma etch and more complex etching capabilities to fabricate features that are currently 32 nm in high-volume production. To continue increasing the density of devices and interconnects, new pattern transfer technologies will be needed with options for the future including extreme ultraviolet lithography, imprint technology and directed self-assembly. While complementary metal oxide semiconductors will continue to be extended for many years, these advanced pattern transfer technologies may enable development of novel memory and logic technologies based on different physical phenomena in the future to enhance and extend information processing.

Keywords: lithography; circuits; devices; processing

1. Introduction

In the 1940s, the information communications and information processing industries sought a more reliable amplifying device and investigated the potential for a solid-state amplifier [1]. The invention of the point contact field-effect transistor (FET) [2,3] provided a proof of concept for the solid-state device, but

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One contribution of 16 to a Discussion Meeting Issue ‘Ultra-precision engineering: from physics to manufacturing’.

manufacturing was very difficult. With the invention of the planar transistor [4] and planar integrated circuit [5], these devices provided the potential for manufacturable devices.

The ability of the semiconductor industry to continue developing higher density, higher performance integrated circuits has been enabled by the evolution of lithography, pattern transfer and process technology. While early integrated circuits were fabricated with 25 μm features, current integrated circuits are currently manufactured with 32 nm features, and this required development of new process technologies and introduction of new materials. As integrated circuit technology advanced, the feature size, separation of structures and layer-to-layer registration were reduced by approximately 30 per cent linearly per generation, which enabled a doubling of the density of transistors with each generation, which was documented by Gordon Moore [6] and has become known as ‘Moore’s Law’. This has resulted in a reduction of cost per transistor, higher transistor density, higher operating frequency and increased functionality.

As feature sizes were reduced and density increased with each new technology, improvements were made in the processes and materials to fabricate the devices with higher density. Although evolutionary changes in processes enabled much of this progression, at times radical new technologies were introduced to enable continuation of device density and performance. As an example, chemical deposition of dopants was replaced with ion implantation in the 1980s to enable fabrication of devices with features sizes less than 2 nm. More recently, the thermally grown 1 nm thick SiO_2 gate dielectric was replaced with a thicker high dielectric constant (κ) [7] material grown by atomic layer deposition [8].

The early improvements of pattern transfer were driven by interactions between the integrated circuit community and the lithography community, which resulted in the development of a lithography community dedicated to developing capabilities for integrated circuit manufacturers. As time progressed in the 1980s, increased interaction was required between the lithography community and the integrated circuits community to enable continued increases in pattern transfer density. In the early 1990s, the US National Technology Roadmap [9] was developed to highlight the need for increased communication between the research community, lithography, process, materials and integrated circuits communities. In 1999, multiple national roadmap efforts were merged into the International Technology Roadmap for Semiconductors (ITRS) [10].

Each new integrated circuit technology manufactured with optical UV lithography requires complex mask-making, and improved photoresist, but further improvements in cost-effective integrated circuit technology are becoming even more challenging. The ITRS has identified a number of technology options to enable continued increases in density to enable the following Moore’s Law; however, novel solutions are identified along with the challenges for their becoming viable solutions in the future. In the 2009 ITRS roadmap, options include double patterning, extreme ultraviolet (EUV); however, options for long-term lithography extension include nanoimprint and directed self-assembly (DSA). Each of these technology options requires development of many capabilities to enable their adoption as viable technologies.

In addition to being able to increase device and interconnect density, the lithography and pattern transfer technology must have low defect density (less than 0.01 cm^{-2}) and this is critical for new technology options. In addition,

metrology is needed to detect and correct defects in the master and in the transferred pattern.

2. Technology adaptation and evolution

With the demonstration of the solid-state FET, industry pursued methods for mass production; however, the early structures were not compatible with high-volume mass production. With the invention of the planar transistor and integrated circuit [5], devices could be fabricated with optical contact printing of photoresist; however, many capabilities needed to be developed to enable this capability. To fabricate an integrated circuit, multiple patterns needed to be generated, aligned to earlier structures and transferred into the materials on the wafer. This required the development of methods to (i) generate master images, (ii) fabricate optical contact masks, (iii) optically transfer the pattern to a photoresist, and then (iv) etch the pattern into the thin films on the semiconductor wafer. While many of the basic capabilities came from the lithographic industry [11–15], several required significant improvement and inventions to enable the development of the first manufacturing process. Because the circuits could be fabricated with large features, they were able to employ existing lithography equipment; however, the photoresist needed to withstand wet chemical etching with hydrofluoric acid, so new photosensitive chemistries were developed to enable this image transfer and etching process [16]. The invention of this new photoresist was driven by semiconductor industry researchers approaching Kodak and describing their problem. With the invention of photo-activated cross-linking chemistries and applications of materials that bonded to SiO₂, this resulted in the development of a photoresist Kodak thin-film resist (KTFR) [17] that could withstand wet chemical etching and enabled effective pattern transfer in the fabrication of planar transistors and integrated circuits. KTFR was the main photoresist for the industry from 1957 to approximately 1972 when features became smaller than could be reliably patterned [18].

The semiconductor industry used these capabilities to fabricate transistors and integrated circuits and continued to reduce their size to increase performance and reduce their cost. As the size of the integrated circuits was reduced, the capabilities of the existing lithographic capabilities started to limit the ability to shrink the devices, so members of the semiconductor industry sought solutions to these issues. As they made their needs known, they discovered new capabilities that were being developed for other applications and were able to apply them to their needs and technology continued to increase in density.

Initial master images were generated by selectively removing a red film from a two-layer film (rubylith) [12]. The contact printing mask was produced by optically shrinking the master image onto a polymer on a glass plate and stepping and repeating this multiple times [12]. Over time, the mask-making became more sophisticated and a pattern-comparing device was developed to generate a master image from a computer-generated image. As the market developed for these masks, more resources were expended to improve the generation of the contact mask through the step-and-repeat process. Eventually, this step-and-repeat operation used to make the mask would be enhanced and used to

pattern the master on the silicon wafer. As the number of transistors continued to increase, computers were increasingly used to design the transistors [19] and circuits and design the mask images [20].

(a) *Mask-making*

Early photomasks were an emulsion coating on a glass plate, but, as features were reduced in size, masks moved to patterned chrome on glass and then quartz as the wavelengths were reduced to the near UV. When projection lithography was employed, pellicles, thin polymer films, were placed above the mask to keep dust and other particles out of the focal plane of the mask. As features were reduced in size to sub-micrometre dimensions, the move to $5\times$ projection lithography reduced demand on mask-making capabilities for a number of years, but, as features approached 250 nm, mask-making was challenged again. As features were reduced in size, projected images on the wafer surfaces were becoming less distinct, so contrast enhancement features [21] were added to enable ‘sharpening’ of features. This has evolved to add characteristics to improve feature size and shape control [22,23].

(b) *Photoresist innovations*

As feature sizes continued to decrease, the early photoresists were unable to continue reducing the size of features and new resists were discovered being used for other applications that were then applied to the semiconductor industry. Companies were then spun off to enable these new resists in higher volume. In the early 1970s, the KTRF was reaching its practical limits, so a new resist was needed. With the need for higher resolution photoresist, the industry adopted a positive-tone novolac [24] resist from the printing plate industry and this was able to be evolved through multiple generations of lithography.

Through the 1960s and 1970s, contact printing and proximity printing continued to be employed and improved, but in the 1980s, with features being reduced below 2 μm , step-and-repeat systems were employed to fabricate the smallest features, and these were aligned to the features generated by proximity contact printing. Initial production steppers used $1\times$ mask technologies to pattern features of 2–1.5 μm , but these were supplemented with $5\times$ steppers for features below this. Over time, it became apparent that the intensity of radiation was decreasing as the wavelength of radiation was decreased, so resists with higher photosensitivity were needed. Researchers invented and developed a chemical amplification process [25], where a photon generated an acid catalyst that diffused and initiated depolymerization of multiple polymer bonds. This chemical amplification process became the basis for multiple generations of resist and enabled cost-effective patterning of photoresist through the 248 nm and 193 nm lithography technologies. As feature sizes continued to shrink, the range of diffusion of the acid needed to be reduced, so species were added to quench this diffusion. So, while chemical amplification has enabled scaling, the competing requirements for high sensitivity, high resolution and low-line edge roughness (LER) had to be balanced and this may limit its long-term application to future lithography.

(c) Etching technology

While pattern transfer from the photoresist was accomplished with wet chemical etching through the 1960s and 1970s, these etchings were isotropic and etched laterally as well as vertically into films. As features were decreased below 2 μm , and the feature size approached the thickness of some of the films to be etched, anisotropic etches were needed. Early plasma etch systems employed capacitively coupled barrel designs that operated at high pressure, which produced isotropic etching. Reactive ion plasma etching [26] was developed to enable improved control of feature size, dimensions and anisotropy of etch for SiO_2 [27] and Al [28]. Through the 1980s, plasma etch and reactive ion etching were developed to enable transfer of sub-micrometre features into the films on the silicon. Critical requirements for plasma etching were anisotropic etch, high etch selectivity (etch rate relative to adjacent materials), low erosion of the photoresist and volatile etch products. As a result of these requirements, different gases were used to etch different materials (e.g. fluorine chemistries to etch SiO_2 and chlorine chemistries to etch aluminium). High etch rate single wafer etchers were developed and employed with improved uniformity and etch rate control [29].

As plasma etch processes were employed, robust processes were needed to remove the photoresist, which had been changed by the plasma etch and other post residues on the etched surfaces. Since the plasma etch processes ‘hardened’ the surface of the resist to wet chemical strips, oxygen plasma cleans (ashing) [29] were developed to strip the hydrocarbon resist and residue from the surface of the wafer. This was followed by chemical cleans to remove non-polymer etch residues.

(d) Dopant processing masking

While several chemical doping techniques [30,31] were used in the early stages of integrated circuit technology, oxide or patterned thin film mask were used as patterns. For many generations, it was possible to continue increasing device density by reducing processing temperatures that reduced diffusion; however, chemical doping needed to be replaced below features of 2 μm . Early in the development of semiconductor technology, ion implantation was identified as a potential method for doping and forming junctions [32,33]; however, it was not until later that ion implantation was used to introduce dopants into lightly doped regions of devices and eventually into the heavily doped regions of devices [34–37]. In many cases, the photoresist was used to block implantation of ions into undesired regions. This greatly simplified the manufacturing process, but meant that the photoresist would need to not outgas in vacuum and be resistant to ‘burning’ and be removable after the implant.

(e) Process and depth of focus

In the 1980s, integrated circuit technologies introduced new materials and structures to enable increased device densities and performance. While many had claimed that it was ‘physically impossible’ to fabricate structures smaller than 1 μm with optical lithography, the industry continued shrinking devices through the use of smaller wavelengths of light (g-line and then i-line) and new photoresist to pattern features on specific layers.

Table 1. Imprint template requirements. This table is based on the 2009 ITRS lithography imprint template requirements. The ITRS imprint template requirements table has much more detail. Reproduced with permission from the Semiconductor Industry Association [39].

requirement	16 nm half-pitch	10 nm half-pitch
nominal image size (nm)	14	9
feature size uniformity (nm 3σ) MPU	1.1	0.8
image placement (nm)	1.6	1.2
mask substrate flatness peak to valley (nm)	36	22
trench width roughness (nm 3σ)	1.1	0.7
defect size causing feature variations (nm)	1.1	0.7

With multiple layers of interconnects being introduced in the 1980s at the same time as optical reduction printing with $5\times$ lithography, the depth of focus became more important in controlling feature size over complex topologies. The introduction of chemical mechanical polishing (CMP) of metals [38] and interlevel dielectrics (ILDs) enabled the use of lithography with higher numerical aperture and smaller depth of focus for many technology generations.

3. Technology roadmap for semiconductors

In the early 1990s, the interactions of the materials, process and lithography were highly coupled and continued increases in density would require coordination of materials, equipment and technology, so the first US National Technology Roadmap for Semiconductors (NTRS) was developed and published in 1994 [9] to identify the lithography and process capabilities needed to continue scaling of integrated circuit technologies. Technology roadmaps were developed in other geographies and these efforts were consolidated in 1999 into the ITRS [10] with collaboration between Asia, Europe and the USA (table 1). The goal of the ITRS is to identify technology needed to keep integrated circuit technology on schedule to support Moore's Law.

One of the biggest concerns of the roadmap was how to cost-effectively achieve continued scaling according to Moore's Law when features were being reduced to less than 250 nm. The 1994 NTRS identified multiple options for pattern transfer (figure 1), and the viability of these was assessed in later roadmaps. The ITRS roadmap identified detailed performance requirements, as a function of time, for each of the photolithography and etch capabilities and operations that are required to enable continuation of scaling following Moore's Law. Requirements include feature resolution, pitch, overlay, defect density, etc. For each of the lithography solutions, the supporting capabilities including mask-making, photoresist and lithography tool capabilities are identified. Where no known solutions are capable, potential solutions were identified along with supporting capabilities required for their successful implementation.

In 1994, the NTRS identified 248 nm, 193 nm, X-ray proximity, EUV proximity lithography, high-throughput e-beam and ion beam lithography as potential lithography solutions, as shown in figure 1. Through subsequent years, 248 and

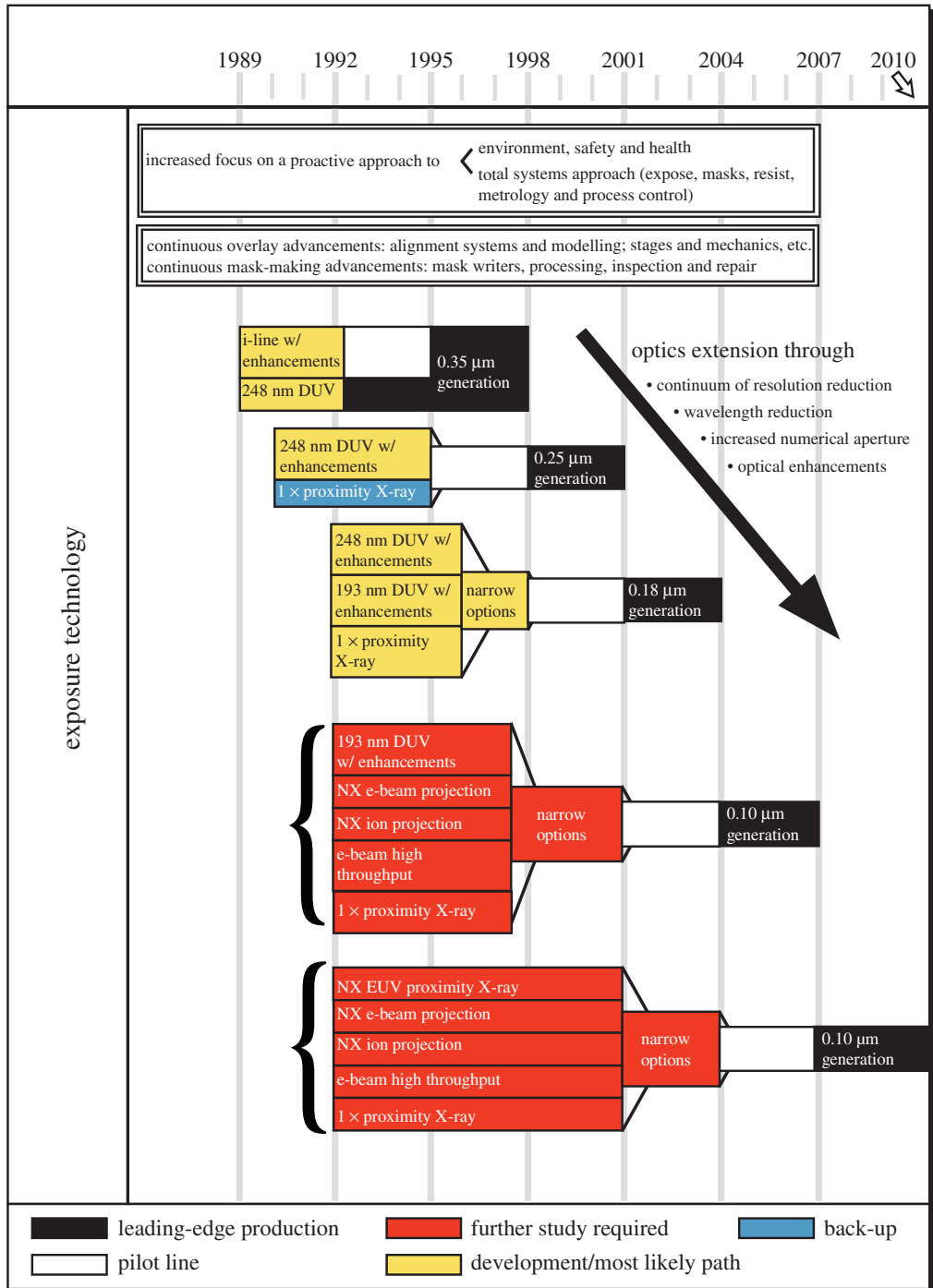


Figure 1. 1994 US National Technology Roadmap for Semiconductors (NTRS) lithography solutions table. Reproduced with permission from the Semiconductor Industry Association [9]. (Online version in colour.)

193 nm lithography and enhancements to these have progressed, while $4\times$ EUV has emerged as a roadmap potential solution and nanoimprint, and DSA has been added as a potential solution for 16 nm and beyond lithography [39], as shown in figure 2. On the other hand, $1\times$ X-ray, $1\times$ EUV, direct write e-beam and ion beam technologies have been dropped as potential solutions. The 248 and 193 nm lithography capabilities have been in production for many years. Both 248 and 193 nm lithography required the development of brighter radiation sources, and lenses that did not degrade with exposure to these wavelengths. Similarly, improved mask and pellicle materials were needed that do not degrade with exposure to the high-energy photons, which required the development of improved quartz for the mask and polymers for the pellicles. In addition, double patterning is a potential solution in addition to being used with 193 nm or EUV lithography [39].

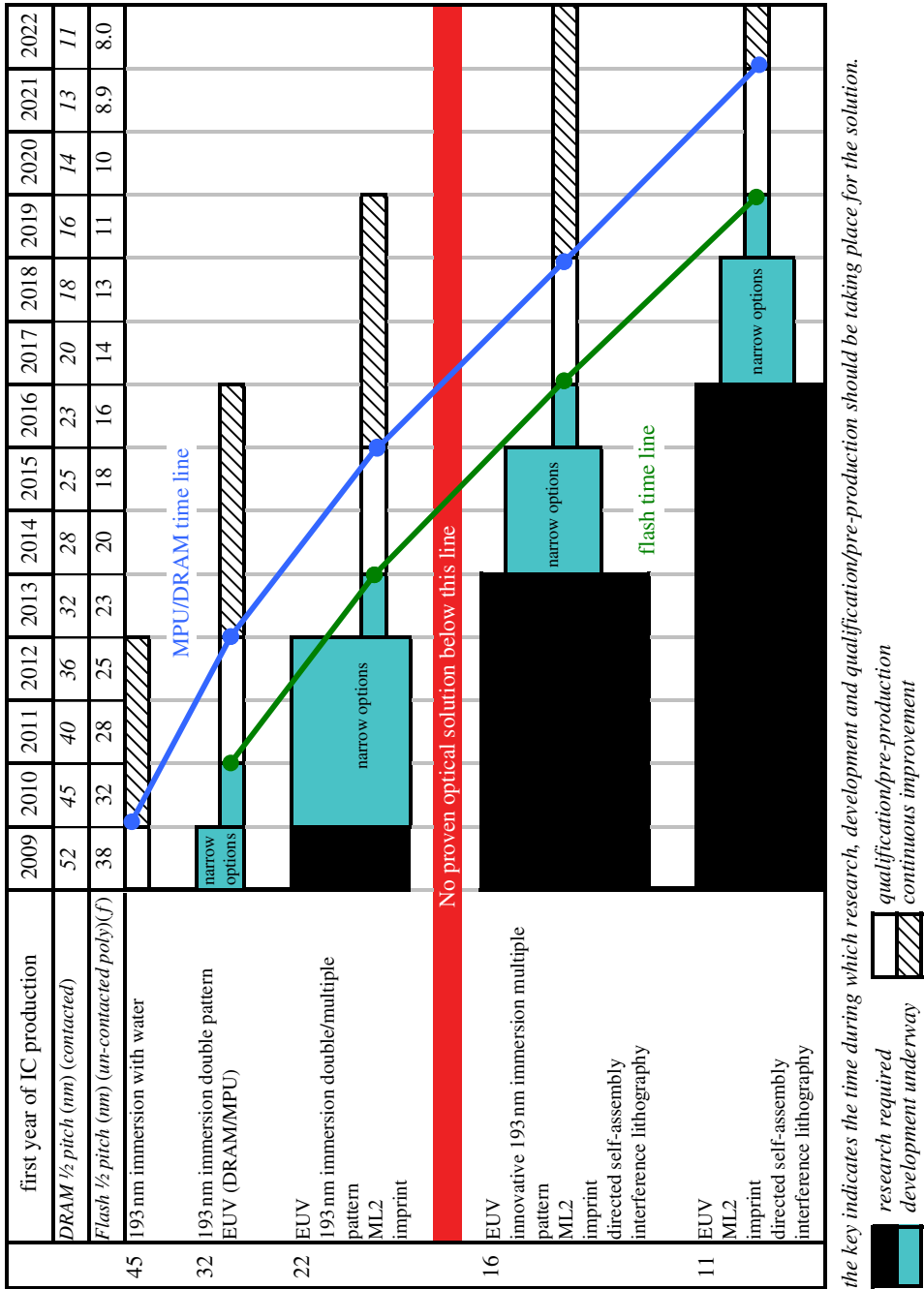
While 193 nm lithography has been in production for over 10 years, significant improvements have been made in the lasers' optics and alignment equipment to enable patterning of smaller features and tighter registration with existing features. This has required significant development of lenses with higher numerical aperture and the introduction of immersion fluids between the lens and the wafer to enable higher effective numerical apertures [14]. Immersion lithography required changes in photoresist to reduce the effects of leaching of chemicals from the resist into the immersion fluid. Thus, the immersion process has placed an additional constraint on the requirements of the photoresist.

(a) *Resist*

Since the chemically amplified resists were introduced, they have continued to evolve with additions of new photoacid generators and additions of quenching agents. These have enabled technologies to reduce half-pitches (one-half of the sum of the minimum line width and space between lines) of patterned structures to 32 nm in production. On the other hand, chemically amplified resists are facing significant challenges. As feature sizes are progressing below 32 nm, the diffusion of the photoacid must be controlled, which means that quenchers must be added to reduce the diffusion length of the acid, but this also reduces the number of polymer links that can be broken, so this reduces sensitivity. In addition to these effects, line edge or line width roughness (LWR) needs to be controlled and this places an additional constraint on the resist. The competition between resolution, sensitivity and LWR [40] has been called the 'triangle of death' for chemically amplified resist; however, the question is what resist mechanism can enable patterning to smaller feature sizes with higher resolution, higher sensitivity and lower LWR.

(b) *Etching technology*

Initially patterns were transferred by exposing and developing photoresist and then chemically etching the films on the wafer. Thus, the resist needed to have good adhesion to the wafer surface and also to be resistant to the chemicals in the etch medium. This required development of more complex resists to meet the adhesion and etch resistance requirements. As features



the key indicates the time during which research, development and qualification/pre-production should be taking place for the solution.

Figure 2. 2009 ITRS lithography potential solutions table. Reproduced with permission from the Semiconductor Industry Association [39]. (Online version in colour.)

were reduced in size below $2\ \mu\text{m}$, the isotropic etchings reduced feature sizes and limited technology scaling. To overcome this limitation, plasma etching and reactive ion etching were developed to anisotropically etch-pattern thin films for devices and interconnects. As these new etch technologies were integrated into the manufacturing process, they needed to have a high selective etch rate to different materials in the process and not erode the photoresist or produce unusual artefacts that would alter the performance of devices and interconnects.

In plasma processing, as the film is etched, by-products are produced in the vapour above the wafer and often deposit on the sidewall of the etched structure; in some cases, this can enhance the anisotropy of the etched film. When the etch is completed, and the photoresist is to be removed, the resist strip needs to also remove the 'polymer' coating of the sidewall. Similarly, depending on the pressure and energy of the plasma or reactive ion etch, damage may be generated in the sidewall of the structure and this could either be removed during cleaning operations or degrade the performance of the fabricated devices.

Many plasma sources have been developed for improving etch performance. The required characteristics include controllable and uniform sidewall angle, tightly controlled feature sizes (critical dimensions (CDs)) and etch rate uniformity, and no electrical damage. Advanced etchers, multi-frequency capacitive coupling plasma, inductive coupling plasma and electron cyclotron resonance are used for these purposes. Pulsed plasma etching is underdeveloped for reducing charge-induced damage and improving photoresist pattern integrity [41]. Microwave surface-wave discharge is also underdeveloped for generating large-area high-density plasma that diffuses towards the wafer region to form quiescent, uniform and low-temperature plasma [42]. Atomic layer control of etch has been established by cycled polymer deposition and etching steps, modulating the bias power [43]. This method is inherently slow but is a potential candidate for low-loading-effect CD shrink or double-pattern double-etch applications.

With new materials being introduced into technologies, different strategies have been needed to pattern and etch them. First of all, copper interconnects were introduced in the 1990s and, because there are no volatile etch species at room temperature, a dual damascene process was developed to etch trenches in the ILD, coat it with a diffusion barrier, electroplate Cu and then use CMP to remove the copper that is not in the trenches, thus defining the interconnects, as illustrated in figure 3. Other materials such as lead zirconium titanate (PZT) for ferroelectric memory devices do not have volatile species and are patterned through sputter etching.

As non-planar transistors become necessary, etch becomes much more challenging. FinFET configurations bring new constraints to selectivity, anisotropy, damage and surface roughness control. The fins are actually the smallest features in the whole process and involve etching using a sidewall-defined mask, a feature as small as $0.7\times$ the gate length [44]. Profile control must be very tight to make very parallel fin surfaces without defects. The gate etch provides many new challenges such as etching thick potentially planarized gate electrodes, and stopping on very thin high- κ material and preserving photoresist. This may require more selective processes, and improved anisotropy without photoresist present.

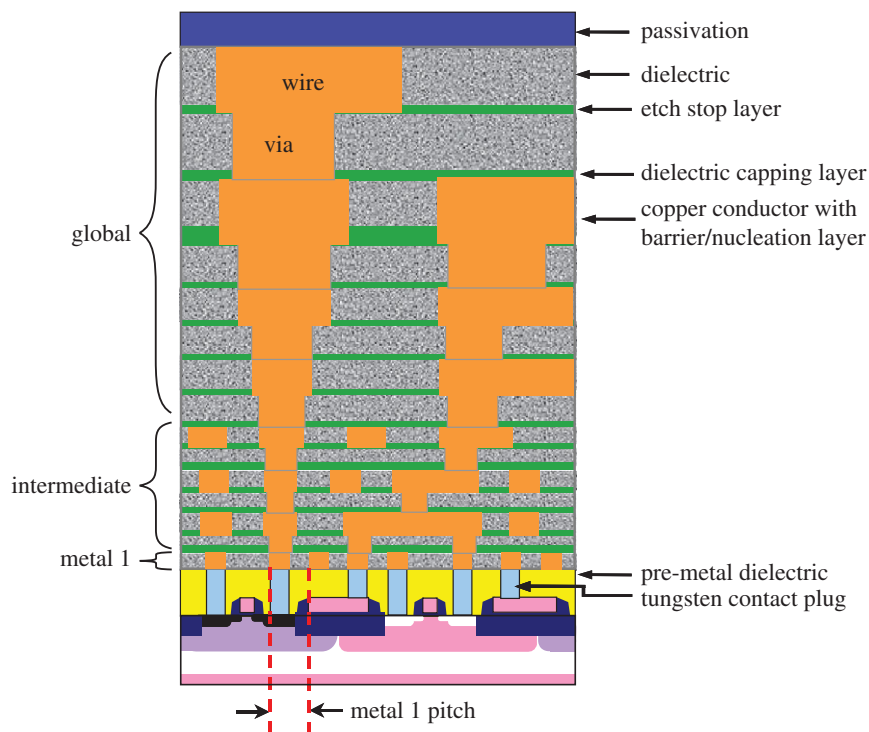


Figure 3. Planarized multi-layer copper interconnects. Reproduced with permission from the Semiconductor Industry Association [39]. (Online version in colour.)

4. Future challenges and options for extending pattern transfer

The 2010 ITRS identifies a number of technology options to replace or be integrated with optical lithography to extend processing below 10 nm half-pitches. At the same time, the ITRS is also evaluating new device and interconnect technologies to extend Moore's Law and these may interact with the lithography and pattern transfer technology options.

(a) Lithography

(i) Options for extending 193 nm lithography

The primary focus of resist development will continue to be the evolutionary design of positive photoresist for use with chemically amplified resist; however, the challenges in simultaneously achieving resolution, sensitivity and LER [40] are daunting. Consequently, older material systems, such as non-chemically amplified resists, negative resists and materials to support pitch division, are also being explored.

193 nm non-chemically amplified materials. Recent advances in ArF excimer laser (193 nm) technology will soon result in lasers with enhanced exposure intensity and throughput. Recent increases in ArF immersion scanner speeds provide excess photons that may enable the re-evaluation of low-sensitivity resist materials, including non-CARs. Also, up to 7× sensitivity improvement

can be realized by reducing poly(methyl methacrylate) (PMMA) film thickness to approximately 20 nm [45]. Polysulfones, which are more sensitive than PMMA, also were investigated for 193 nm immersion lithography applications. A post-exposure bake can accelerate polysulfone depolymerization. The 193 nm irradiation of polynorbornene sulfone [45] results in film thinning, reduced SO₂ content and E_0 of less than 50 mJ cm⁻², when developed in an isopropyl alcohol/cyclohexanone mixture. Successful non-CAR thin film materials must demonstrate enhanced ArF sensitivity, resolution and plasma etch resistance, while maintaining acceptable levels of LER. This consideration may limit the applicability of chain scissioning-type chemistries, or polymer designs, which include significant levels of heteroatoms such as oxygen or sulfur.

193 nm negative-tone resist materials. Several 193 nm negative-tone resist materials were developed to operate by a cross-linking or a polarity change mechanism [46,47]. Negative resists tended to perform better than positive-tone resists with binary masks, but responded less well to phase-shift mask designs, which may limit the use of negative imaging in some types of memory cell layouts.

Recently, top coat-free ArF negative-tone resist was developed and demonstrated, using a 1.07 NA 193 nm immersion scanner, with a performance close to that of a corresponding positive-tone resist [48]. Historically, negative-tone resists tended to exhibit pattern bridging, which must be resolved for use with 193 nm immersion exposure technologies.

(ii) *193 nm pitch division*

Pitch division technology options are being explored for extending 193 nm lithography and there are multiple options under consideration. These options include spacer double patterning, double exposure and double patterning as illustrated in figure 4. Spacer double patterning does not require the development of new resists, but does require deposition of multiple layers of conventional materials, planarization and etches to generate the higher density features and will not be described further. Similarly, dual patterning employs a ‘hard mask’ that is patterned and etched twice with two different photoresist masking operations and can use conventional materials.

Double exposure requires a nonlinear response in the resist and new exposure mechanism. Alternatively, a single-exposure process with dual, positive and negative, tone developer has been demonstrated.

Single-exposure dual tone develop. In this method, the positive developer removes resist with the highest dose, while the negative developer removes the lowest dose resist, leaving an intermediate-dosed resist pattern. Dual tone develop (conventional positive-tone and solvent negative-tone developers) has been demonstrated with 38 nm dense lines/spaces, under 1.35 NA immersion exposure. This represents a proof of concept for enhancing feature size uniformity and achieving low LWR [49], but significant work is needed to optimize dimensional control.

Double-exposure materials for 193 nm lithography. ‘Double-exposure material’ refers to materials that enable pitch-division imaging with two arbitrary sequential exposures, without de-chuck of the wafer between exposures. Such a material would provide benefits in cost, improved overlay and greater design rule flexibility versus other pitch-division approaches. What makes these materials

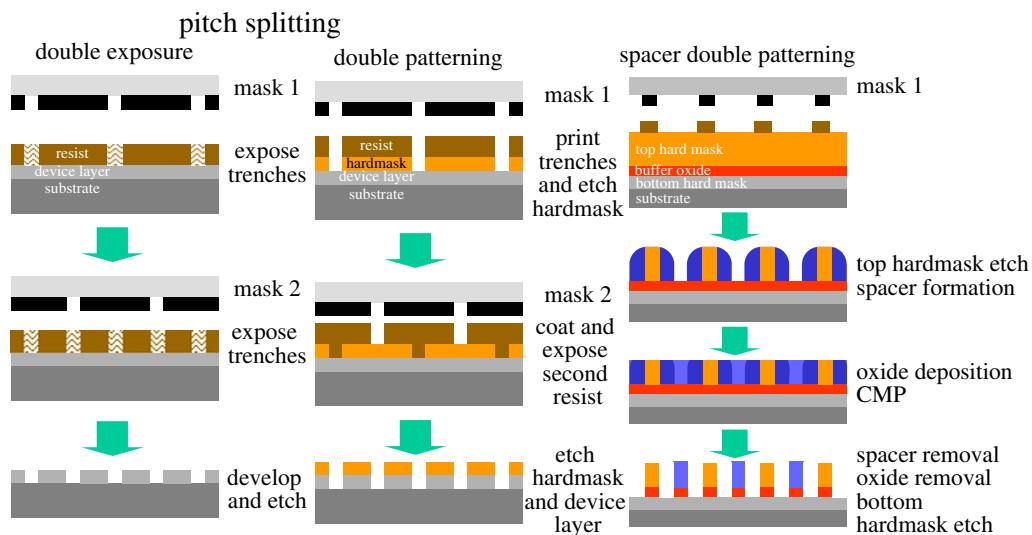


Figure 4. ITRS lithography examples of pitch division or splitting. Reproduced with permission from the Semiconductor Industry Association [39]. (Online version in colour.)

so challenging is that they must have a response dependent not just on the total dose received, but also on the time history in which the photons were received. This property, called non-reciprocity, is needed for the material to distinguish information which would normally be lost in regions of overlap in a double-exposure scheme.

True two-photon absorption produces an intensity squared (I^2) response; however, the required cross sections for relevant lithographic pulse lengths are many orders of magnitude greater than those available [50,51]. The reversible contrast enhancement layer (rCEL) approach has been modelled extensively [50,51], but the resulting contrast is simply too low, owing to diffractive effects and the imperfect bleaching available from even remotely realistic materials.

5. Next generation lithography

Technology options for ‘next generation lithography’ include EUV, NanoImprint and DSA. All of these technologies have significant challenges that must be overcome before they could be viable to replace optical technology (e.g. 193 nm lithography) for patterning features with the smallest size.

(a) Extreme ultraviolet lithography

The basic concept of EUV lithography is to produce a bright source of 13.5 nm radiation and use X-ray optics to reduce the mask image by $4\times$ and transfer the pattern into resist on the wafer surface. Since most materials absorb photons in this wavelength range, reflective optics was developed and the mask must also

be a multi-layer reflective mask. Since this is a new technology with 13.5 nm radiation, multiple challenges must be overcome; these include:

- an intense 13 nm radiation source;
- a reflective optical system;
- a reflective mask technology; and
- EUV resist that has adequate sensitivity, and required resolution.

Owing to the wavelength of the radiation, this must all be accomplished in a vacuum system. Progress has been made in improving the intensity of 13.5 nm radiation sources, but the intensity of radiation reaching the EUV resist is still lower than desired owing to the losses occurring from each reflective mirror in the system. Since most materials absorb 13.5 nm radiation, the optical system must employ reflective optics that has losses of 30–40% for each mirror. With the high-intensity radiation illuminating the first mirrors, degradation of reflectance occurs as a result of contamination being deposited on the surface of the mirrors from the vacuum system and also ion bombardment from the plasma source.

The EUV mask has another set of challenges since it requires a set of layers of silicon and tungsten to constructively reflect the 13.5 nm radiation. A serious metrology challenge is to detect imperfections in the thin-film stack or the patterned mask that would generate defects on the imaging wafer. Significant progress has been made in improving the quality of the mask ‘blanks’ and thus reducing defects, but the ability to repair defects is a serious challenge. In a conventional transmission mask for 193 nm radiation, imperfections can occur in processing, but these can be corrected through focus ion beam processing. A comparable technology needs to be developed to correct imperfections in patterned EUV mask.

Since the intensity of the radiation reaching the surface of the resist is greatly reduced, the resist needs to have a high sensitivity and the ability to produce small high-resolution features while also having low LER and tight control of feature size. The material properties of existing chemically amplified resist are in direct opposition to these requirements and are often called the ‘triangle of death’ in the lithography community. There are concerns that, as the features become smaller, the radiation reaching the resist surface will be lower in intensity and ‘shot noise’ will dominate and cause wide variations in feature sizes and shapes.

(b) *Extreme ultraviolet resist*

While the evolutionary use of positive chemically amplified resist is the primary focus of resist development, the challenges of simultaneously achieving high sensitivity, high resolution, low LER, low outgassing and potential pattern collapse are very challenging, so other alternatives are also being evaluated.

EUV lithography requires revolutionary resist materials to address the resolution–LWR–sensitivity trade-off, with reduced outgassing [52–54]. Resist film thicknesses may continue to shrink with feature size, in part to avoid pattern collapse [55,56], which may introduce new issues. Future semiconductor processes might also require several different post-processing methods [57] to meet the projected patterning requirements. While work on positive chemically amplified resists will continue, research is underway to explore other potential material candidates that satisfy projected requirements for enabling emerging lithographic

technologies. These include: non-chemically amplified resist materials, inorganic, organic–inorganic hybrid resist materials, novel negative resists and 193 nm double-exposure resists.

(i) *Extreme ultraviolet negative-tone cationic resist materials*

EUV lithography is expected to have 7 per cent flare (background illumination), which affects resolution and process window. Negative-tone resist was investigated to reduce the effects of flare intrinsic to the bright-field mask. Negative-tone resist showed the largest process window for 60 nm isolated line [58]. Molecular glass fullerene resist, composed of a fullerene derivative, novolac epoxide and a photoacid generator, was evaluated using a scanning electron microscope and developed using organic solvent [59]. These chemically amplified fullerene-based resists show high sensitivity ($11 \mu\text{C cm}^{-2}$), good resolution (20 nm hp) and low LWR (2.5–4.5 nm). The etch resistances of these resists are comparable to those of a high-durability commercial resist. A negative-tone molecular glass, based on a cationic polymerization mechanism, was developed and evaluated using e-beam and EUV and developed using organic solvent [60]. These molecular glass resists were able to resolve 35–25 nm half-pitch patterns with high sensitivity ($38\text{--}22 \mu\text{C cm}^{-2}$) and showed low LER.

(ii) *Non-chemically amplified negative-tone resist materials*

If the negative-tone resist operates by a mass-conserving cross-linking mechanism, this resist should exhibit low outgassing. Cross-linking chemistries, in general, are being investigated to determine whether they can also achieve resolution, sensitivity, LER and etch resistance. In initial experiments, a number of these individual properties have been independently demonstrated, and the challenge is to combine them into one single resist. One high-resolution resist material resolved 20 nm line/space and 20 nm dot patterns with e-beam lithography [61]. Similarly, a polyphenol molecular glass and azide cross-linker also showed good resolution and reduced LER [62]. Another molecular glass approach showed ultrahigh resolution (10 nm), little side roughness and high durability to halide plasma etching [63,64]. Photoradical cross-linking approaches are mass-conserving and should be low outgassing. One example of this approach is a resist containing a photoradical initiator resolved 60 nm isolated lines at a dose of $5\text{--}6 \text{ mJ cm}^{-2}$ with EUV [65]. These new resists had a lower number of molecules per cm^2 outgassing than standard resists. One of the particularly attractive aspects of negative-toned resists, which are non-CA, is that there is likely to be fewer molecular structural design trade-offs between plasma etch resistance and photospeed than positively toned non-CA resists.

(iii) *Inorganic and organic–inorganic hybrid resist*

In addition to the challenges of improving resolution, sensitivity, LER and low outgassing, pattern collapse needed to be addressed as features scaled to smaller dimensions. Electron beam inorganic resists can exhibit higher contrast than organic resists and improved mechanical properties that could prevent pattern collapse of dense high-aspect-ratio features, but they show poor resist sensitivity. Hydrogen silsesquioxane (HSQ) is a high-resolution negative-tone

inorganic resist that shows resolution below 10 nm when coupled with e-beam lithography [66], resolves patterns with half-pitches as small as 20 nm with EUV interference lithography [67], and has low LER (less than 2 nm) [68,69]. New inorganic electron-beam resists with Zr and Hf [70] have demonstrated, with a 30 keV electron-beam, sensitivities as low as $8 \mu\text{C cm}^{-2}$, achieved 15 nm lines and 36 nm dense features at higher doses with an LWR of approximately 2 nm. These resists also exhibit high etch resistance (greater than $7\times$ that of thermal SiO_2) in reactive-plasma etching. Incorporation of 4–15 wt% silica particles to commercial e-beam resists increased etch resistance in O_2 [71] without degrading the sensitivity and contrast. E-beam lithography of (20–100 keV) silica nanoparticle-incorporated resists exhibits a significantly enhanced resolution over their pure counterparts, giving a much better pattern definition with up to 100 per cent reduction of line broadening in some cases. Resist component outgassing from inorganic and organic–inorganic hybrid resist materials might have a serious impact on advanced lithographic technologies, so the type and number of outgassing molecules must be quantified and analysed. Post-etch transfer of LER and LWR of nanoparticle-filled hybrid resist may be different from conventional resist materials, and this should be studied. Finally, the behaviour of defects resulting from using resist materials filled with inorganic nanoparticles still needs to be investigated to make sure that there is not fatal flaw in this approach.

(iv) *Extreme ultraviolet non-chemically amplified resist materials*

Since non-chemically amplified resists operate by a chain scission mechanism, it is possible that these resists could exhibit lower outgassing than that observed in chemically amplified resists. PMMA has resolved line/space patterns down to 20 nm with EUV exposure and exhibited very small apparent LER and nearly vertical sidewalls [72]. To increase EUV absorption and reduce outgassing, α -trifluoromethane was substituted in PMMA and 50 nm 1 : 1 line/space patterns were resolved with EUV, with a photospeed 4.0 times higher than in PMMA. To increase sensitivity, glass transition temperature and etch resistance, linear polycarbonates with polysulfone backbones were evaluated and demonstrated initial resolutions of 35–50 nm lines/spaces, with low LER-increased sensitivity compared with PMMA [73]. Poly(1-butene sulfone) has been patterned with EUV photons, and this system has resolved 50 nm half-pitch patterns [74]. A key requirement for the successful implementation of non-CAR materials will be the demonstration of enhanced plasma etch resistance while maintaining good EUV sensitivity. This could be difficult to achieve, since the molecular structural considerations for plasma etch resistance and sensitivity are generally in opposition.

(c) *Nanoimprint*

Nanoimprint is a process where a polymer coats the surface and an imprint template forces the polymer into areas where the image is to be retained [75]. The polymer is then ‘fixed’ by exposing the polymer to UV radiation [76] and cross-linking or cross-linking the polymer with a thermal cure [75]. After the cure, the imprint tool is removed and the polymer image remains on the surface. This image can then be used as an etch mask. The critical challenges for this technology are fabricating the imprint template with features that are $1\times$ without defects,

imprinting the pattern in the polymer without defects and with high-throughput, aligning the imprint to earlier structures, compensating for systematic changes in feature size, and compensating for systematic overlay errors.

Because the imprint template has to create features at the same size as on the wafer, the generation of the master tool features will be much more challenging than generating a $4\times$ mask. Thus, the generation of a defect-free master will be critical [77]. In addition to generating the pattern in resist, it must be transferred to the imprint master with tight control of size and roughness. In addition, the master must not have defects and detection and correction must be enabled. If the features are to be reduced below 10 nm, even small particles would have the opportunity to get into the master tool and cause defects that would be replicated in each product that was imprinted. Since the polymer dimensions will change in curing and processing structures different size will change differently and the tool design must accommodate these differences.

Integrated circuits use many mask layers and each of these must be aligned to previous structures with tight tolerances across areas greater than 1 cm. During processing, the wafer can change dimensionally owing to incorporation of dopants and other processes, so the imprint tool and alignment system must be able to accommodate these small variations in locations of structures. Currently, these are accommodated with small changes in magnification of the optical system, but integrating these into the tool design would more closely couple the process and the tool design.

Imprint polymers must have good adhesion to the wafer and materials on the wafer surface, but not adhere to the imprint tool after cure. Adhesion to the tool could leave residue in the tool features that could result in defects being imprinted in any subsequent wafers. Thus, detection of residue on the imprint tool or defects in the imprinted pattern will be crucial.

For this to be cost-effective, the effective throughput must be of the order of minutes, so the time for the UV or thermal cure must be of the order of minutes.

A potential advantage of nanoimprint is the ability to directly deposit and pattern materials in one process, for example deposition of a low dielectric constant material such as an ILD [78,79]. This could result in significant process simplification.

(d) Directed self-assembly for lithography extension

DSA refers to the alignment of self-assembled patterns in desired locations with predictable shapes, controlled dimensions and registered within a lithographically generated pattern. The goal of DSA would be to print features with either 193 nm lithography or EUV lithography and have block copolymers assemble smaller features with higher density than was printed lithographically. The lithographically defined features would be considered 'sparse' patterns. Progress has been made in alignment to sparse patterns, and demonstration of 7 nm features, and lithographically useful rapid annealing times have been demonstrated.

(i) Directed self-assembly critical challenges

If DSA is to be considered a viable and competitive patterning option, it must be able to form a desired set of structures at dimensions at least a factor of 2 smaller than and with twice the density that can be achieved by conventional

lithographic methods. This corresponds to resolution, LER and LWR targets of less than 12 nm, less than 1.3 nm and less than 1.7 nm, respectively. The structures must form in predefined locations with respect to existing structures, and with a very low defect density (less than 0.01 cm^{-2}). The net time required to form and fix a pattern must be compatible with conventional inline process requirements and a throughput of one hundred and twenty 300 mm wafers h^{-1} . Also, the ability to achieve pattern registration, required feature sizes, density, low defect levels, etch resistance and process times must be demonstrated simultaneously in an experiment with the same material.

(ii) *Directed self-assembly state of the art*

Recent research has brought progress in each of these aspects, but no material/process combination currently satisfies all of these requirements. Block copolymer self-assembly can easily define a limited set of highly symmetric patterns, i.e. repeating lines/spaces and hexagonal arrays of cylindrical holes that may be useful in defining circuit elements. The ability to draw from a richer set of shapes would broaden its utility and range of application. A variety of DSA methods provide the means to position self-assembled patterns on a wafer, to orient the pattern with a specific directionality and to register the pattern with respect to previous lithography levels. Annealing times, which depend on the rate at which the system approaches thermodynamic equilibrium, have been reduced from multiple days and hours to a few minutes, through the use of solvent annealing, which represents a realistic time scale for potential processing applications. Self-assembled structures have been generated with dimensions well below 10 nm, providing evidence of this approach's extensibility. Defect densities represent a significant research challenge, as the best results observed to date are orders of magnitude larger than the requirement of less than 0.01 cm^{-2} .

Two distinct DSA methods have been widely practised. The first, a form of graphoepitaxy, employs a trench or other relief feature to confine self-assembly. In the second, a surface pattern with contrasting chemical properties directs self-assembly. Both of these techniques require a 'neutral' layer to enable assembly of vertically aligned structures over the substrate materials.

(iii) *Directed self-assembly graphoepitaxy*

In this approach, lithographically defined topographic features and boundaries direct the ordering of a self-assembled block copolymer film. The self-assembled patterns self-register to the lithographically defined and etched pattern and subdivide it into features with sublithographic resolution. The surface properties of the recesses control pattern alignment. For example, if the bottom of a groove is neutral but the sidewall is preferentially wetted by one block, then lamellae form in parallel with the groove. If all surfaces are neutral, then the lamellae orient perpendicular to the groove. Lines also tend to reproduce and track defects in the lithographically defined wall. Therefore, for the graphoepitaxy approach, the quality of the final self-assembled patterns depends on precise control of the lithographic process forming the guide pattern. A key challenge is to develop systems that are tolerant of small variations in the lithographic pattern.

These self-assembled block copolymeric systems exhibit placement errors that depend on template edge roughness and polymer domain non-uniformity. Registration accuracy is dictated by phase-separation thermodynamics, composition and polydispersity effects [80]. The projected requirement of 1.4 nm registration accuracy for 16 nm half-pitch corresponds to a spacing accuracy of approximately 0.04 per cent of the intrinsic period of the polymer pattern (termed L_0). This is considerably smaller than typical domain size/spacing distributions of $3\sigma \sim 0.09\text{--}0.3 L_0$ for sphere or cylinder-forming patterns [81]. Research is needed to develop less sensitive material systems or methods that maintain constant film thickness over substrate topography.

In an alternative strategy for graphoepitaxial DSA, a sparse lattice of nanoscale posts can template growth of a two-dimensional array of spherical microdomains. The guide posts substitute for a small fraction of the spherical domains in a regular fashion and thereby provide periodic constraints that induce long-range order with reduced defectivity [82].

(iv) *Directed self-assembly surface energy*

Directed block copolymer assembly on substrates bearing lithographically defined chemical nanopatterns offers a second route for aligning and registering patterns of block copolymer microdomains [83]. In this approach, a thin organic layer, for example a self-assembled monolayer or a polymer brush, is deposited on a substrate and lithographically patterned, and that pattern is transferred to the organic layer (for example, by an oxygen plasma etch) to define regions with distinct chemistry and surface energies. When the surface-modified substrate is coated with a thin block copolymer film and thermally annealed, preferential wetting drives each block to migrate towards chemically compatible surface regions, so as to minimize the free energy of the system. If the contrast in the surface pattern is strong, then significant mismatch in the periods L_s and L_o can be tolerated before increased defectivity is observed [84]. With strong polymer–surface interactions, the block copolymer domains can be directed into many of the essential features required for manufacturing integrated circuits with regular fabric architectures, including dense and isolated bends, jogs, spots, line terminations and T-junctions [83,85]. Improved CD control and LER at nanoscale dimensions are key benefits of this DSA approach: such films can correct for line width variations in the chemical surface pattern and maintain the copolymer pattern feature size equal to $0.5 L_s$ [86], and the polymer also appears to exhibit some self-healing behaviour.

Recent research has demonstrated the spatial frequency multiplication of sparse, lithographically defined chemical surface patterns using block copolymer DSA. Examples of forming cylindrical [87,88] and lamellar [89] microdomains have been described. In each case, the quality of the final microdomain structures is superior to that of the chemical surface patterns, as measured by placement error, dimensional uniformity and LER. These sparse patterning methods provide a means to bridge the gap between the dimensional scale accessible by advanced optical lithography and the sublithographic scale, where self-assembly offers the greatest benefit.

This approach depends on a multi-step process to produce the local alterations of the neutral layer's chemical properties. Further research is needed on materials

and one-step methods that would enable direct lithographically induced spatial variation in surface chemistry and functionalization.

(v) *Applying supramolecular and hybrid concepts to self-assembly*

As was mentioned earlier, although many of the critical capabilities have been demonstrated in individual experiments, they have yet to be demonstrated in one experiment and new materials with more flexibility are needed. Systematic studies of the self-assembly of new block copolymer and triblock copolymer materials and architectures will broaden their utility and improve functionality. For example, recent work using hybrid blends of block copolymers with organosilicate oligomers [90] and blends of homopolymers with triblock polymers [91] has demonstrated characteristic microdomain spacing well below 10 nm, an indicator of potential extensibility. In another recent report [92], supramolecular assembly of hydrogen-bonding units was combined with the controlled phase segregation of diblock copolymers to fabricate highly ordered square arrays of sub-20 nm via structures, instead of the hexagonal ordering that is normally observed. A more evolutionary path may require a hybrid resist formulation that incorporates phase-segregating diblock copolymers to yield a resist that can self-assemble within the patterned feature, and a proof of concept has been demonstrated [93]. However, significant research in these areas is needed for these systems to warrant consideration for sub-22 nm potential solutions.

(vi) *Process simplification*

A critical challenge is to simplify the process used to define the patterns that direct the alignment of the block copolymers, since the graphoepitaxy requires patterning and etching and surface energy patterning requires multiple process steps. The integration of photoresist functionality with self-assembly [93] could provide a potential path to process simplification, but significant research would be needed to make this viable technology.

6. Potential future needs for precision placement of atoms

In scaling transistors, electrical performance variability of devices may be affected by variations in placement of dopant atoms in the ‘channel’ region of the device. Experiments have demonstrated in large devices that dopants in periodic arrays had lower variability in electrical performance than devices with the same number of dopants in random locations [94]. More recent experiments indicate that dopants placed in periodic arrays closer to the drain of the device had improved electrical performance over those with dopants in periodic arrays uniformly along the channel or at the ‘source’ of the device [95]. As metal oxide semiconductor (MOS) devices are reduced in size, the number of dopants in the channel will continue to be reduced, so precise placement may be needed to meet performance requirements for a sub-10 nm devices. As new devices emerge beyond complementary metal oxide semiconductors (CMOS) with new functionality, the requirements on placement of atoms may become even more severe. The question is how can dopants or atoms be placed deterministically in required locations cost-effectively.

(a) Future device options

Future CMOS devices could use complex structures such as multi-gate devices or alternative channel materials such as InGaAs and Ge or possibly nanowire, nanotubes or graphene. The planar structures will be able to use evolutionary lithographic techniques, but the multi-gate structures will place additional demands on the lithographic and pattern transfer techniques, as seen in figure 5.

Beyond the lithography requirements, future MOS devices and possibly beyond CMOS devices may require precise placement of atoms to enable improved devices [96]. Recent work has demonstrated that placing dopants in periodic arrays can reduce variations in transistor electrical performance and reduced variability that improves circuit performance [94]. More recent studies indicate that dopants placed in periodic arrays in precise locations in the channel can improve performance [97]. This should apply to Si, Ge or InGaAs channel materials, but it is not clear how this would be applied to carbon nanotube or graphene devices. This may offer opportunities to extend CMOS performance through precise placement of dopants in the channel region.

Multiple ‘beyond CMOS’ alternative state variables such as spin orientation or spin phase are evaluated in the ITRS Emerging Research Devices chapter, but the control of materials locations has not been determined yet. On the other hand, the ability to place dopants in precise locations or arrays could enable exploration of new device options in the future.

(b) Deterministic doping

Current ion implantation technology blankets the surface of a wafer with ions with controlled energy and uniform density, but statistically random ion placement occurs as do random scattering events in the semiconductor. The ability to place dopant atoms in precise locations has been demonstrated by saturating a semiconductor surface with hydrogen, selectively removing hydrogen atoms from a surface with a scanning tunnelling microscope, exposing the surface to dopants and then depositing a thin layer of semiconductor over the dopants with low-temperature molecular beam epitaxy [96]. Recently, single atom ion implantation has demonstrated the ability to fabricate individual devices [94,95]. While both of these capabilities have been able to fabricate individual devices, they would not be able to fabricate integrated circuits in high volume and the cost would be prohibitive. Deposition of a monolayer coating of self-assembled molecules on a surface has demonstrated the ability to place dopants in separated locations, defined by the molecule [97]. While this technique does not have the precision of the STM or single atom implanter, it offers a potential high-volume alternative for placing dopants in periodic arrays, but evolutionary approaches may emerge to improve placement accuracy in the future.

7. Summary

Dramatic improvements in information processing and communication technology have been enabled by the ability of the semiconductor industry to continue increasing the density of devices in an integrated circuit cost-effectively.

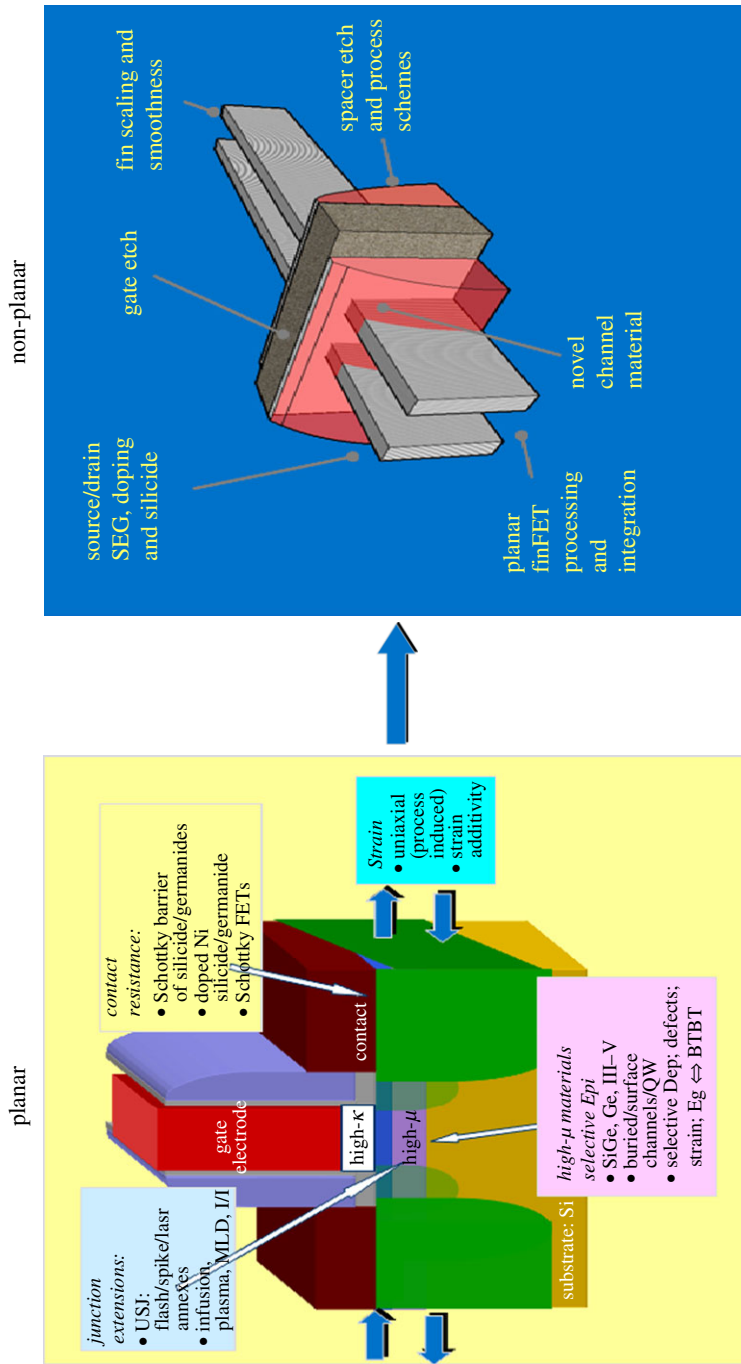


Figure 5. Planar and multigate transistor structures. Reproduced with permission from the Semiconductor Industry Association [39]. (Online version in colour.)

While early improvements in technology were driven by demand for improved lithography, etching and materials, the ITRS now serves as a document to highlight future needs for capabilities to researchers, equipment suppliers, material suppliers and process integrators. While precision manufacturing is required for fabrication of higher density devices, continued reduction in size of devices may also require precise placement of atoms within the devices.

I would like to thank the Semiconductor Industry Association, International SEMATECH, and the ITRS for their cooperation in preparing this paper in providing figures and allowing inclusion of modified selections from the 2009 ITRS Emerging Research Materials chapter. I would also like to thank Aubrey C. Tobey, of ACT International, Dave Markle, formerly of Ultratech, and John Carruthers, Portland State University, for providing insight into the early development of capabilities to enable development of pattern transfer. I acknowledge the valuable information on the history of computing and integrated circuit technology at the Chip History Center, (www.chiphistory.org), and Chris Mack's website on the history of photolithography at <http://www.lithoguru.com/scientist/lithohistory.html> for insight into the development and evolution of photolithography.

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