CURRICULUM VITAE

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Arseniy Vitkovskiy

Personal details

Date of birth:	20th May 1979
Place of birth:	Kemerovskaya obl./USSR
Education summary:	Dipl.Ing. (MIREA), M.Sc. (KTH), Ph.D. student (UNIBO)
Professional skills:	VLSI specification and design, modelling and validation, embedded systems, Networks-on-Chip, heterogeneous architectures and reconfigurable computing

Education

2005 – present (until Dec 2007) **University of Bologna (UNIBO), Italy**

Ph.D. student

- Doctorate program: European Doctorate on Information Technology (EDITH)
- Department: Advanced Research Centre for Electronic Systems (ARCES)
- Specialization: Information Technology

2006 – 2007 **Delft University of Technology (TUDelft), the Netherlands**

Guest researcher

- Computer Engineering Laboratory
- Faculty: Electrical Engineering, Mathematics and Computer Science (EEMCS)

2002 – 2006 **Moscow State Institute of Radio Engineering, Electronics and Automation (MIREA), Russia**

Postgraduate student

- Department of Cybernetics
- Specialization: Mathematical simulation, calculus of approximations and program systems

2002 – 2004 **Royal Institute of Technology (KTH), Stockholm, Sweden**

Master of Science

- Master's program: System-on-Chip Design
- Department of Microelectronics and Information Technology
- Specialization: Electrical Engineering

1996 – 2002 **Moscow State Institute of Radio Engineering, Electronics and Automation (MIREA), Russia**

Diploma Engineer

- Department: International Faculty of Computer Science
- Specialization: Automated control and information processing systems

Awards and scholarships

2005 – 2007
- Marie Curie Intra-European Fellowship within the Human Resource and Mobility programme ("Marie Curie" actions) sixth framework programme for RDT of the European Union

2002 – 2004
- Socware, Invest in Sweden Agency (ISA)

Work experience

2005 – present **STMicroelectronics & University of Bologna joint research lab**

Collaborative researcher

- Agrate Brianza Central R&D, STMicroelectronics
- ARCES, University of Bologna

2001 – 2002 **Centre of Information Technologies and Systems of Executive State Authorities of Russia**

Programmer

- Department of Information System Modelling
- Position: Programmer in Software Analytical Complex Development Team

Practical skills

CAD tools:	Mentor Graphics ModelSim, Synopsys DesignCompiler, Synopsys DesignWare Tools, OrCAD PCB Designer, MicroWind, CVS versioning system
Programming:	VHDL, SPICE, Assembly, C/C++, Delphi, Perl (basics), MatLab
HW architectures:	ARM, AMBA and PrimeCell peripherals, PiCoGA and PACT XPP reconfigurable processors, M2000 eFPGA, Nostrum NoC, STBus and STNoC
Research:	VLSI specification and design
	Modelling and verification
	Heterogeneous reconfigurable architectures
	Application mapping
	Low-power and error control strategies
	Networks-on-Chip: topologies, routing mechanisms, power issues
Languages:	Russian – native;
	English – fluent;
	German, Swedish, Italian - basic

Research interests

Novel computer architectures, Systems-on-Chip, Networks-on-Chip, embedded systems, HW/SW co-design, system modelling, heterogeneous architectures and reconfigurable computing

References

Refer to Appendix A

Publications

Refer to Appendix B

Reviews

Refer to Appendix C

Personal qualities

Responsible, diligent, communicative

Other interests

Historical fencing and archery, medieval reconstruction, music composing and arranging, playing guitar

Appendix A. ACADEMIC REFERENCES

1. Ph.D. **Fabio Campi**
   Agrate Brianza Central R&D, STMicroelectronics
   Bologna, Italy.
   Email: fcampi@deis.unibo.it
2. Prof. **Axel Jantsch**
   ECS, ICT, Royal Institute of Technology
   Stockholm, Sweden.
   Email: axel@imit.kth.se
3. Further references available upon request.

Appendix B. PUBLICATIONS

Degree works:

1. Master thesis: “A Study on Power Consumption in the Nostrum Communication Network”, Stockholm, Sweden, April 2004.
2. Engineer thesis: “Development of Structural-Graphical Component of Software Analytical Complex”, Moscow, Russia, March 2002.

Journal publications:

1. A. Vitkovski, A. Jantsch, R. Lauter, R. Haukilahti, E. Nilsson, “Low-Power and Error Protection Coding for Network-on-Chip Traffic”, IEE Proc. Computers & Digital Techniques. (CURRENTLY UNDER REVISION)

Conference and workshop proceedings:

1. A. Vitkovski, G. Kuzmanov, G. Gaydadjiev, “Memory Organization with Multi-Pattern Parallel Accesses”, submitted to DATE’08.
2. A. Deledda, F. Campi, A. Vitkovski, et al, “Design of HW/SW Communication Infrastructure for a Heterogeneous Reconfigurable Processor”, submitted to DATE’08.
3. F. Campi, A. Deledda, M. Pizzotti, L. Ciccarelli, C. Mucci, A. Lodi, A. Vitkovski, L. Vanzolini, “A dynamically adaptive DSP for heterogeneous reconfigurable platforms”, DATE’07.
4. A. Vitkovski, “Data Communication and Memory Hierarchy in Reconfigurable Heterogeneous SoC”, poster session, EDITH Workshop on Advance in Information Technology, Bertinoro (FC), 25-26 August, 2006.
5. F. Campi, P. Zoffoli, C. Mucci, M. Bocchi, A. Deledda, M. De Dominicis, A. Vitkovski “A Stream Register File Unit for Reconfigurable Processors”, ISCAS’06.
6. A. Jantsch, R. Lauter, A. Vitkowski, “Power analysis of link level and end-to-end data protection in networks on chip”, ISCAS’05.
7. A. Vitkovski, R. Haukilahti, A. Jantsch, E. Nilsson, “Low-Power and Error Coding for Network-on-Chip Traffic”, NorChip 2005.

Appendix C. REVIEWS

Conference reviews:

1. Design, Automation and Test in Europe 2007, DATE07.
2. IEEE International Symposium on Circuits and Systems 2007, ISCAS07.

Journal reviews:

1. Journal of Systems Architecture.