A low complexity all-digital DS-SS transceiver for power-line communications

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Abstract

In this paper we present an architecture for an all-digital binary phase shift keyed (BPSK) direct-sequence (DS) spread spectrum (SS) transceiver. The all-digital architecture incorporates a delay-locked loop for clock recovery, whereas phase recovery is implicit in the timing synchronization; this is possible due to the use of digital up and down converters. Spread spectrum modulation has been chosen for robustness and electromagnetic compatibility reasons, given its low power spectral density over a wide frequency band. The proposed architecture is intended for use in the 9-30 MHz ETSI band. The data rate is 128 Kbps, and the chip rate is 8.192 Mchips/s. The simulations carried out show that the proposed scheme is valid for medium rate applications which can make use of the power lines as their communication channel.

1. Introduction

In recent years, the use of communications through the electric power-line has been increasing. The electric power-line is found in most buildings, so no infrastructure is needed compared with other communication systems. There are many household applications that power-line communication can serve. In a first approach, these applications can be divided into two groups: those that use low data rate transmissions between transmitters and receivers, and those that use high data rate transmissions. The first group includes mainly control applications, such as remote handling of electrical appliances. The second group includes data transmission applications, such as local area computer networks. In between we can think of cheaper devices than high rate modems that can provide other services than those supported by low rate modems, mainly devoted to control tasks. In this sense, the purpose of this work is the development of a medium-rate all-digital power-line communications modem, which at a low complexity level can provide tranmission rates compatible with audio applications. Thus, our major design premise has been simplicity. The modem should provide a raw data rate of 128 Kbps with a BER less than 10^{-3} in the frequency band from 9 MHz up to 30 MHz; this band has been specified by the European Telecommunications Standard Institute (ETSI) for coexistence of access and in-house power-line systems. Up/down conversion will be entirely digital, thus avoiding analog oscillators and closed-loop phase recovery schemes. A $Simulink^{TM}$ workspace has been used for simulation purposes, and the main results will be portrayed in the following sections.

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2. BPSK Direct-Sequence Spread Spectrum Transceiver Design

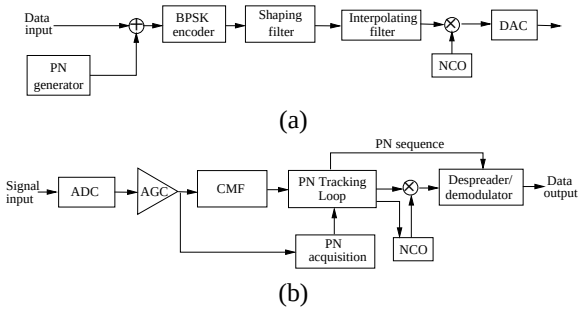

Figure 1: Block diagram of the DSSS system. (a) Transmitter block diagram. (b) Receiver block diagram.

A block diagram of the proposed Direct-Sequence Spread-Spectrum (DSSS) system is shown in Fig. 1. At the transmitter, the input data signal is spread with a PN

sequence and digitally up-converted. This modulated signal is then D/A converted and transmitted over the channel. The bit-rate is 128 Kbps, the number of chips per bit is 64, and the shaping pulse is a square-root raised-cosine with roll-off zero. Thus, the occupied bandwidth will be 8.192 MHz, from 16.384 MHz up to 24.576 MHz. These numbers have been chosen for the sake of simplicity, as will become clear later. However, these are theoretical bounds; finite length filters will impose some spectral spreading beyond these limits, yielding a residual aliasing in the receiver. Later in this paper some results concerning the quality of the transmission and the length of the filters are exposed. At the receiver, the transmitted data are recovered by despreading and demodulating the received signal. Note that the up and down conversion stages are entirely digital, thus avoiding analog oscillators.

2.1. Transmitter Design

The BPSK DSSS transmitter consists of three blocks: a PN generator, a BPSK encoder and a shaping filter. The spreader is simply an exclusive-OR (XOR) circuit. The shaping filter is a square-root raised cosine filter with a roll-off factor 0. The number of taps of this filter is examined in section 3.

The correlation properties of the pseudorandom noise (PN) sequence are very important in determining the overall performance of a DSSS system. One class of these sequences is known as m-sequences (maximal-length sequences). They have a period of $2^n - 1$ (n is the degree of the m-sequence generator). In this case, we take a 127-chip m-sequence $(n = 7)$ and then truncate it to length 64. The auto-correlation properties of the resulting sequence are as good as those of the original m-sequence.

For the frequency band chosen for transmission, namely, (16.384,24.576) MHz, within the ETSI band for PLC indoor services, the transmitter needs to include an interpolator and digital modulator before the D/A conversion. The minimum sampling rate can be readily shown to be 49.152 MHz, for a number of samples per chip equal to six. The frequency for the digital up-conversion corresponding to a sampling rate of 49.152 MHz is equal to $5\pi/6$ rad, which can be implemented with a very short look-up table of 12 positions.

2.2. Frame Structure

In order to minimize the effect of sudden changes of channel characteristics and lower the probability for a transmitted frame being hit by noise impulses, the frame length is made very short. In addition, short frames make timing synchronization easier. If the length of a data frame is short, the timing error accumulated within it will be so small that it can be neglected.

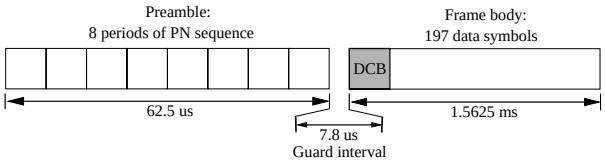

Figure 2: Frame structure. DCB denotes the DLL Convergence Bits.

As shown in Fig. 2, a frame is composed of 200 data symbols (i.e., 200 data bits), preceded by a preamble section for timing synchronization. The preamble is composed of eight periods of the spreading waveform (64-chip PN code). There is a short interval of one bit duration between the preamble section and the frame body, during which no signal is transmitted. This guard interval prevents interference between the preamble and the frame body, and gives the receiver enough time to switch its state from preamble detection to data reception.

The beginning of the frame body are the DLL Convergence Bits (DCB), which are three bits used to let the DLL achieve the optimum sampling instant. This is very important to carry out phase recovery correctly.

2.3. Receiver Design

Once the signal has been bandpass sampled at a rate of 16.384 MHz, the spectrum will look like that shown in Figure 3, corresponding to the spectrum of the BPSK signal spreaded and filtered by the channel, located between 0 and 8 MHz, i.e., 0 and π rad. The bandpass sampling yields a copy of this spectrum in the negative frequencies. Thus, the acquisition and tracking of the spreading code will be applied on the frequency shifted signal, and some minor modifications will be introduced in the corresponding blocks to cope with this bandpass signal. This is a major consideration in the overall design, focused on the avoidance of cumbersome phase recovery loops.

In the PN acquisition block, the locally generated PN sequence is coarsely aligned within one half-chip interval to the PN sequence of the received signal. In the PN tracking block, the locally generated PN sequence is precisely aligned with the PN sequence of the received signal. Once the PN sequence is properly aligned, the data are demodulated, and the BPSK decoder block can recover the transmitted data.

2.3.1. PN Acquisition Block

There are several methods for PN acquisition. Typically, these can be classified into a serial method and a parallel search method. For the parallel search method, fast

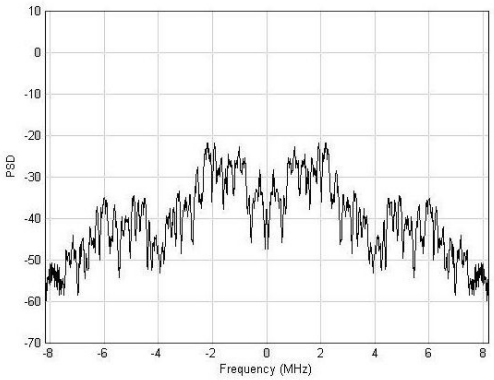

Figure 3: Example of simulated spectrum of the received signal. Note the increasing attenuation from 0 up to π, corresponding to the channel attenuation from 16.384 MHz up to 24.576 MHz.

PN alignment can be achieved, but more hardware is required as compared with the serial search method [1]. In our design, a serial search method is chosen because fast PN acquisition is not a critical factor, and the hardware complexity is reduced. A detailed structure of the PN acquisition block is shown in Fig. 4, where CMF denotes the chip-matched filter, a sinc pulse in this case. For the sampling rate of 16.384 MHz, and carrier frequency of 20.48 MHz, the corresponding discrete-time frequency happens to be $2\pi 20.48/16.384 = 2.5\pi$, equivalent to $\pi/2$ as detailed in Figure 4.

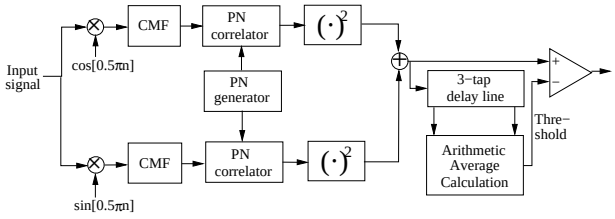

Figure 4: Block diagram of PN acquisition block.

The PN correlator reads in the baseband signal continuously and calculates the correlation values between the incoming signal and the spreading m-sequence code. If a preamble reaches the receiver, the output from the CMF will give large periodical peaks. Otherwise, only random noise can be observed at its output. Fig. 5 shows an example of the PN correlator output.

The PN correlator output then feeds the peak detection circuit and a three-tap delay line. A peak must have a correlation magnitude larger than a threshold. This thresholding procedure increases the probability of detection by using an

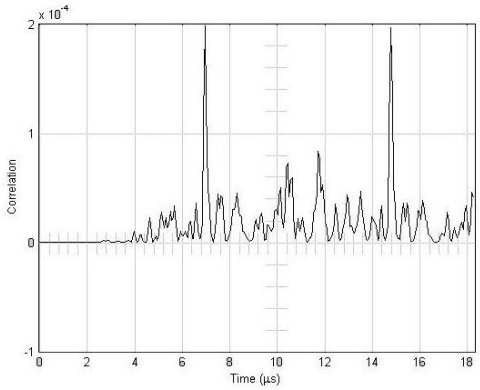

Figure 5: Example of CMF output.

adaptive threshold. The threshold value is determined by the arithmetic mean of the three previous correlation magnitude values, so it is adjusted dynamically according to channel condition.

If large peaks periodically reappear, they are counted until the number of peaks detected is eight, which is the length of the preamble. This marks the end of the preamble and the beginning of PN code tracking. It is important to note that we are making simultaneously PN code acquisition and frame synchronization.

2.3.2. PN Tracking Block

For PN tracking, either a coherent or noncoherent loop can be used. In this paper, a noncoherent loop is used, which is a delay-locked loop (DLL). In our delay-locked loop, two PN sequences are delayed from each other one chip interval, and they are used for the early and late signals.

The delay-locked loops are usually designed to work with a baseband signal at its input. As shown in Fig. 1(b), our delay-locked loop uses a passband signal, since no downconversion is done before acquisition and tracking. Thus, a baseband delay-locked loop is modified to work with passband signals. Fig. 6 shows the delay-locked loop used in this paper, a modification of that shown in [2]. Note that for the chip rate 8.192 MHz, and carrier frequency 20.48 MHz, we have that $\cos(2\pi 20.48/8.192) = \cos(\pi n)$.

In this diagram, the block labelled T_c represents a delay of one chip interval. The branch filters $H_b(z)$ are first order low-pass with bandwith B_b, and transfer functions given by

$$H_b(z) = \frac{1-a}{1-az^{-1}}, \qquad a \triangleq exp(-2\pi B_b T_c), \quad (1)$$

where T_c denotes the chip period. The bandwith B_b of the branch filters is set to be $1/T$, where T is the bit period.

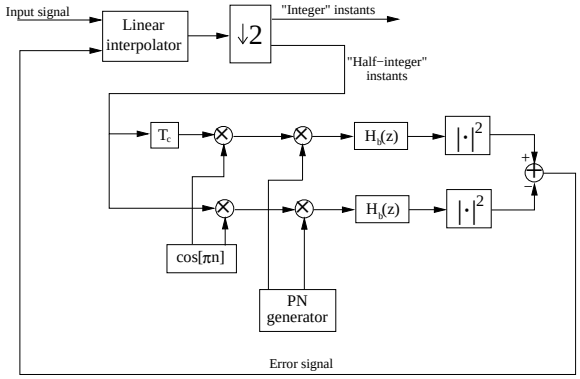

Figure 6: Block diagram of the delay-locked loop.

The DLL loop equation is given by

$$\varepsilon_{k+1} = \varepsilon_k - \gamma e_k, \tag{2}$$

where ε_k denotes the interpolating offset in the k-th sampling instant, e_k denotes the error signal in Fig. 6, and γ is the interpolator sensitivity, which is chosen to be 2^{-6}. As it is shown in the next section, the successful demodulation of the passband signal depends highly on the good behavior of the PN synchronization, and mainly on the DLL. For the DLL to work properly, the signal level at its input cannot be too low (PN tracking would be too slow) or too high (in this case, the DLL might get unlocked). Thus, the automatic gain control block (AGC) at the input of the receiver is a critical block.

2.3.3. Demodulation

In Fig. 1 it can be noticed that the discrete oscillator used to convert the input signal to baseband is placed just after the DLL. It is easy to check that the frequency of this oscillator working at the chip rate must be π rad. It is important to mention the absence of loops to carry out phase recovery. As we are trying to simplify as much as possible the hardware of the modem, phase recovery is performed in an open-loop way. For this method to work, the PN code synchronization must have been achieved. For this purpose, three bits are left in the beginning of the frame to let the DLL converge, i.e., achieve the steady state. Once the DLL has converged, the oscillator can be turned on at a known position; this is possible because the up-conversion in the transmitter side is also digital. Because of the steady state residual error of the DLL, this method leaves a resulting phase error that oscillates with a period equal to the bit period T; i.e., the timing errors amount also to phase errors. This resulting phase error modulates the baseband signal, although its impact on the transmission performance is negligible.

2.3.4. Despreader and BPSK decoder

The final step that allows to recover the transmitted data, is despreading and BPSK-decoding of baseband signal. This is achieved by multiplying the PN sequence used in the DLL with the baseband signal. The resulting signal then feeds an *integrate and dump* block, which integrates (adds) the input samples during a bit period, and resets its accumulator before performing the next integration. The sign of this integration is then used to decide whether the transmitted bit was 0 or 1.

3. Performance Simulations

This section shows some of the simulations carried out to analyze the modem performance.

As we are working with a PLC noise model, we cannot define a *noise power* N_0 as we do with AWGN. Thus, the SNR estimation method used in our simulations to evaluate the system performance is given by

$$\mathrm{SNR} = 10\log\left(\frac{\sigma_x^2}{\sigma_n^2}\right), \tag{3}$$

where

$$\sigma_x^2 = \frac{1}{N}\sum_{i=1}^{N} x_i^2, \qquad \sigma_n^2 = \frac{1}{N}\sum_{i=1}^{N} n_i^2, \tag{4}$$

and x_i are the signal samples (with no noise), and n_i are the noise samples. N is the number of samples taken to calculate the SNR.

Fig. 8 shows the noise power spectral density (PSD) used in the simulations. This PSD results from measurements made in a specific PLC channel, where the narrow band interference at 17.92 MHz results from a radio link [5].

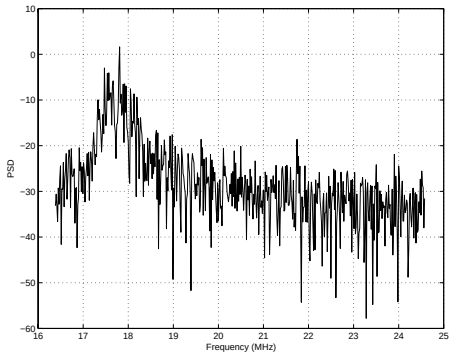

Figure 8: PLC noise PSD used in the simulations.

Fig. 9 shows the simulated BER performance of the proposed power-line modem, considering the existing noise in

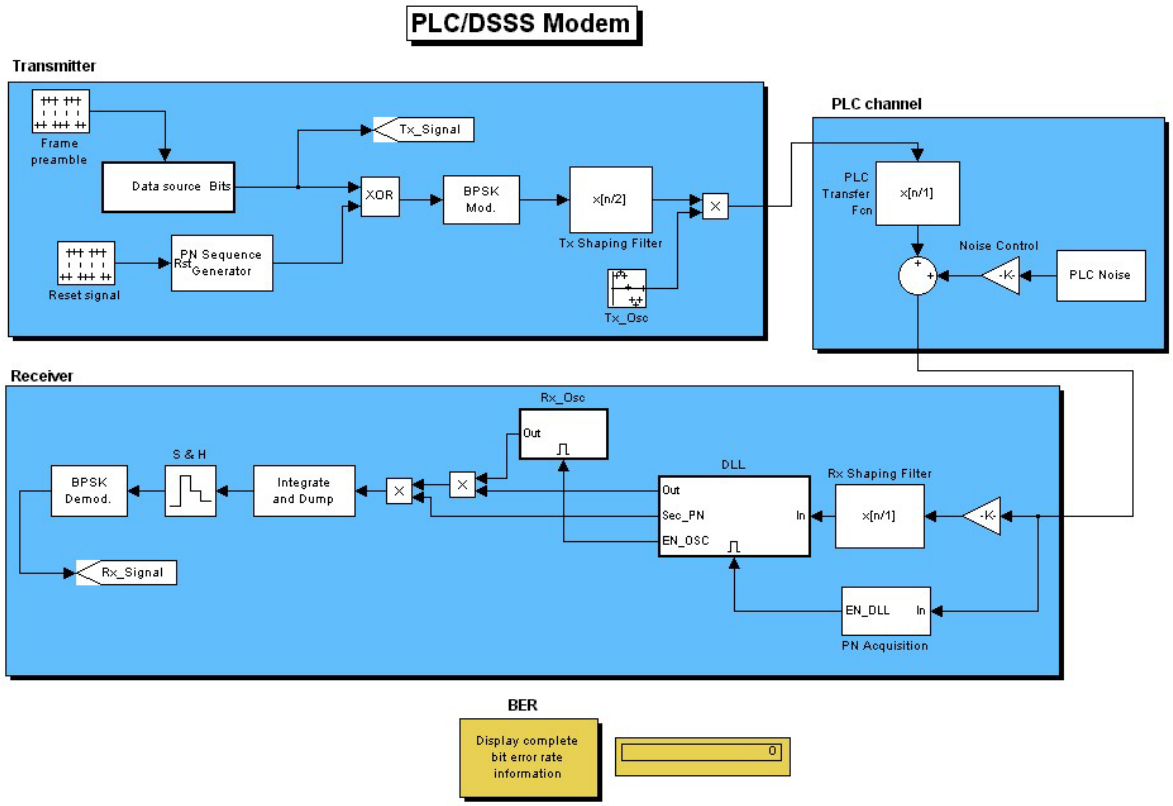

Figure 7: $Simulink^{TM}$ workspace

the PLC channel. We can see that to get a BER below 10^{-3}, the SNR at the input of the receiver must be between -5 dB and -4 dB. The use of spread spectrum is a good alternative towards the compliant of eventual limitations on the transmitted power. ETSI is currently working in the specifications for power line communications; in particular, frequency masks to preserve emission levels will be dictated.

A critical issue to reduce the complexity of the signal processing algorithms is the number of taps of the filters. Given the zero roll-off of the shaping filters, a high number of taps is expected, which should be reduced at minimum. The non-ideality of front-end filters and shaping filters will let noise beyond the frequencies stated above get into the receiver, and will generate aliasing in the sampling process. The impact of the aliasing in the overall performance was studied by simulation, with the results for the BER shown in Fig. 10. No degradation is appreciated for a number of taps higher than 41; this is the lenght used for the square-root raised cosine filters used in the simulations throughout this work.

Similar considerations can be done with respect to the number of bits for a fixed point implementation. Thus, for a

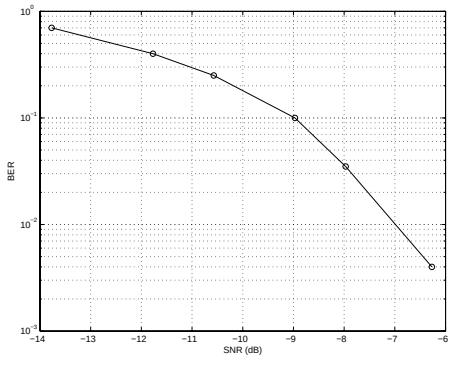

Figure 9: Simulated performance of the system with PLC noise.

reference signal to noise ratio at the input of the receiver of -5 dB (with floating-point operations), Figure 11 shows the required SNR to achieve the same BER. A 3 dB degradation has been measured for 12 bits; this is a reasonable number of bits for the range of speeds of the ADC converters which

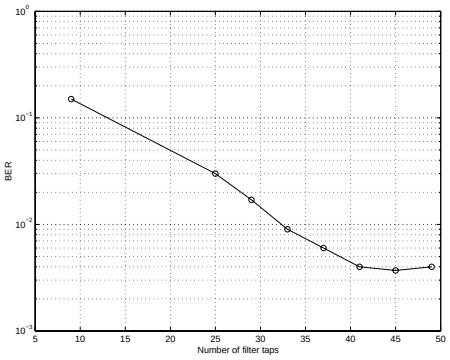

Figure 10: Simulated performance of the system versus the number of filter taps (SNR = -4 dB).

will be necessary in the final prototype.

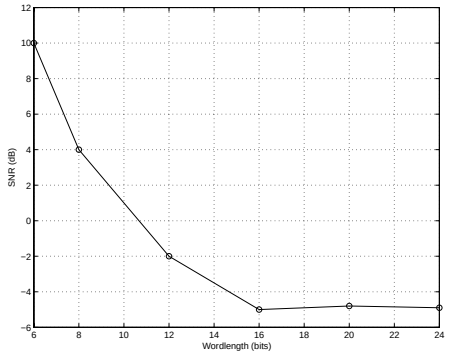

Figure 11: Simulated performance of the receiver with fixed-point operations (SNR = -5 dB).

4. Conclusions

By means of appropriate communication techniques, power lines can be used as a communication medium between electric or electronic devices. We have presented a medium rate modem for audio applications, for which simplicity has been the main design premise. In this sense, we have used an implicit phase recovery scheme, embedded in the timing synchronization, which avoids the use of phase recovery loops. Digital up/down conversion is proposed, given the range of frequencies assigned by ETSI for this systems, within the HF band. Spread spectrum has been considered as the best option, for emission levels and robustness reasons. Simulations have shown an acceptable performance, which will have to be confirmed by the final prototype, currently under development.

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