Low-Power 32bit x 32bit Multiplier Design with Pipelined Block-Wise Shutdown

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Abstract. This paper proposes a novel low-power 32bit × 32bit multiplier with pipelined block-wise shutdown scheme. When it idles, it turns off supply voltage to reduce both dynamic and static power. Restoring whole large-size functional block often causes severe power line noise, so the proposed multiplier shutdowns and wakes up sequentially along with pipeline stage. It is described in Verilog HDL and fabricated in standard cell library. Total gate count is about 22400 gates. Power simulation was performed in deep submicron technologies where static power due to leakage current increases significantly. In idle mode, the proposed multiplier consumes 0.013mW and 0.006mW in 0.13μm and 0.09μm technologies, respectively, and it reduces power consumption to 0.07%~0.08% of active mode. As fabrication technology becomes small, power efficiency degrades in the conventional clock gating scheme, but the proposed multiplier does not. The low-power design methodology in this paper can be easily adopted in most functional blocks with pipeline architecture.

1 Introduction

Recently, power consideration has become an important issue in VLSI design, especially for portable and battery-powered systems. In deep submicron fabrication technologies, leakage current increases exponentially according to device scaling [1]. Fig. 1 shows the trends of supply voltage, threshold voltage, dynamic power, and static power along with the progress of fabrication technology. As shown in Fig. 1, the leakage power may dominate total power in near future [2].

Shutting down some functional blocks in the chip is a promising approach to reduce both dynamic power and static power [3]-[5], where the supply voltage is cut off when the functional block idles. In the hardware implementation, multi-threshold voltage CMOS (MTCMOS) [2],[6]-[10] has been proposed and extensively investigated. However, severe power line noise due to the large current surge often causes system malfunction when the functional block is quite large [11], since large number of logic gates switch simultaneously during wakeup process. Recently, block-wise shutdown [11] was proposed to mitigate the power line noise. Many large-size

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functional blocks such as multiplier and arithmetic logic unit (ALU) employ pipeline scheme to increase the performance. When the supply voltage of the shutdown block is recovered sequentially along with the pipeline stage, the number of simultaneous switching gates reduces. Thus the power line noise significantly decreases [11].

In this paper, we propose a low-power 32bit × 32bit multiplier with pipelined block-wise shutdown. It was designed, fabricated, and verified by chip implementation, and the power reduction was evaluated by simulation.

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Fig. 2 shows the proposed low-power multiplier architecture. It exploits modified Booth algorithm to reduce hardware complexity. It has three pipeline stages for high performance. To reduce the power line noise, partitioning of pipeline stage is determined by minimizing the number of maximum simultaneous switching gates. Note that the power line noise increases as the number of simultaneous switching gates increases. First pipeline stage consists of partial product blocks which generate partial product of multiplicand. Second pipeline stage consists of two 8-to-4 compressors. Third pipeline stage consists of one 8-to-4 compressor, two 4-to-2 compressors, and a final adder. The proposed multiplier was described in Verilog HDL, and it was fabricated in standard cell library. The gate counts of first, second, and third pipeline stages are about 9800, 7800, and 4800 gates, respectively.

Fig. 3 shows the block diagram of the proposed low-power multiplier with shutdown circuitry. In the shutdown and wake-up processes, supply voltage of the whole circuit is cut off and recovered sequentially along with pipeline stage. At the same time, only one pipeline stage is shutdown and wakes up, and the number of simultaneous switching gates reduces. Thus, the power line noise is mitigated significantly.

In the conventional block-wise shutdown schemes, pipeline registers of each stage are connected to a high V_T line, and these registers are never shutdown. Thus the intermediate computation values are preserved and the block can wake up

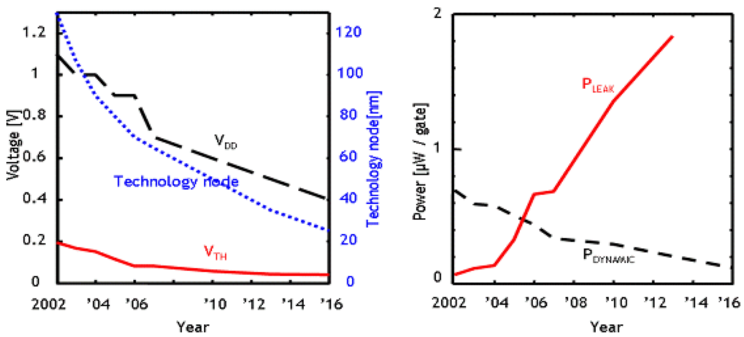

Fig. 1. Trends of supply voltage, threshold voltage, dynamic power, and static power

immediately. However, these pipeline registers still consume static power since their supply voltages are not cut off. In the proposed multiplier, the pipeline registers occupy about 40% of total gate count. Thus, we included all the pipeline registers in the shutdown blocks to reduce static power, and all logic gates and pipeline registers

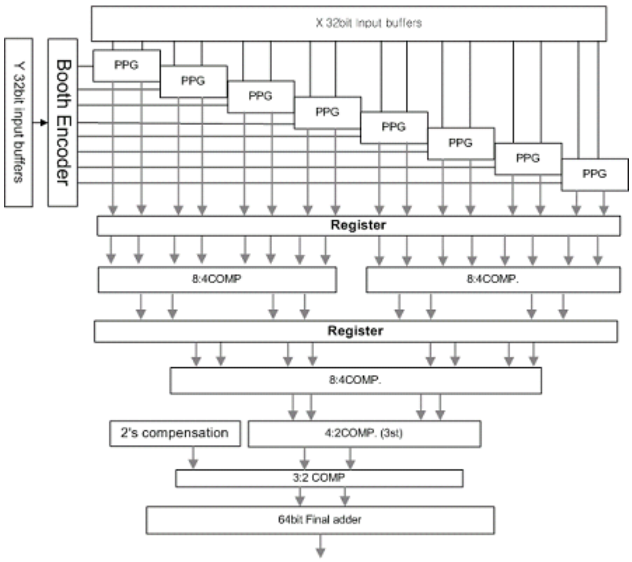

Fig. 2. Architecture of the proposed low-power 32bit×32bit multiplier

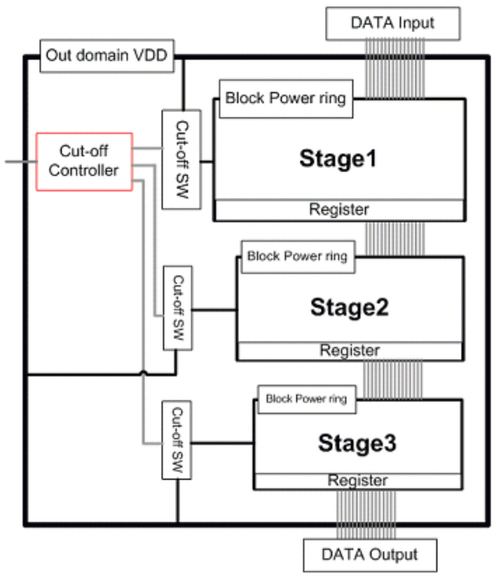

Fig. 3. Block diagram of the proposed low-power 32bit×32bit multiplier

are cut off during shutdown. Each pipeline stage has its own block power ring, and the supply voltages of all logic gates and pipeline registers are connected to it. Power is delivered in the flow as: external power supply → cut-off switch → block power ring → logic gates and pipeline registers. Cut-off controller turns on and off cut-off switches in a pipelined manner as shown in Fig. 4 when the multiplier enters into or exits from sleep mode. When sleep signal is activated from outside of the multiplier, the cut-off controller generates pipelined control signals as illustrated in Fig. 5.

In order to implement the proposed low-power multiplier in standard cell library, each pipeline stage should be registered as a macro cell in the placement and routing (P&R) design library. If this is omitted, the P&R tool recognizes the multiplier as a single macro cell in auto-route process, and all logic gates and pipeline registers are connected to a common power line. The detailed design process is as follows. First, each pipeline stage is described in Verilog HDL as separate blocks. These stages are synthesized into gate level. Each synthesized pipeline stage is placed separately, and the result is registered as a macro cell in the P&R design library. These macro cells are placed in the silicon area by manual placement. The macro cells should be placed so as to minimize interconnection length. Also they should be placed to effectively distribute heat dissipation. During auto-routing process, top-level file preserving macro cell hierarchy reads macro cell design information from the P&R design library. The resulting P&R pattern is shown in Fig. 6.

In the proposed low-power multiplier, two types of V_{DD} lines are required. Global V_{DD} line (VDDG) is connected between external V_{DD} and cut-off switches. VDDG is not cut off at all. Stage V_{DD} lines (VDDS1, VDDS2, VDDS3) are connected between cut-off switches and pipeline stages. All logic gates and pipeline registers in the pipeline stage n (n = 1,2,3) acquire their power from VDDSn. VDDSn is independently cut off and recovered by cut-off switches. When VDDSn is cut off, pipeline stage n is totally shutdown and no dynamic and static power is consumed. To reduce the number of cut-off switches, common GND line is used in the whole multiplier. GND line of the cut-off controller and those of all the pipeline stages are connected with each other. No cut-off switches are connected to GND lines.

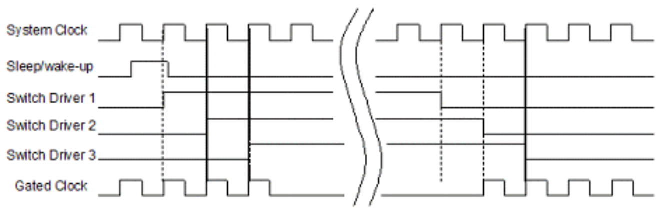

Fig. 4. Pipelined turning on and off the current switches

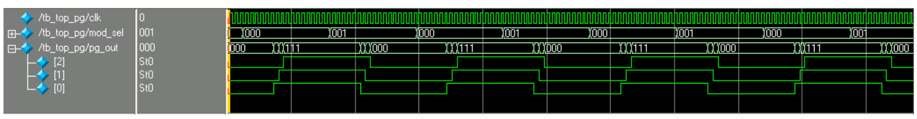

Fig. 5. Waveforms of control signals in the cut-off controller

Cut-off switches are large MOS transistors with very wide channels. PMOS transistors are used since there is no voltage drop across cut-off switches. PMOS size should be carefully determined. Cut-off process would be too slow if sized too small, and too much area is consumed if sized too large. Optimal channel width is calculated by considering power consumption of each pipeline stage. To increase channel width, PMOS transistors have many fingers as shown in Fig. 7.

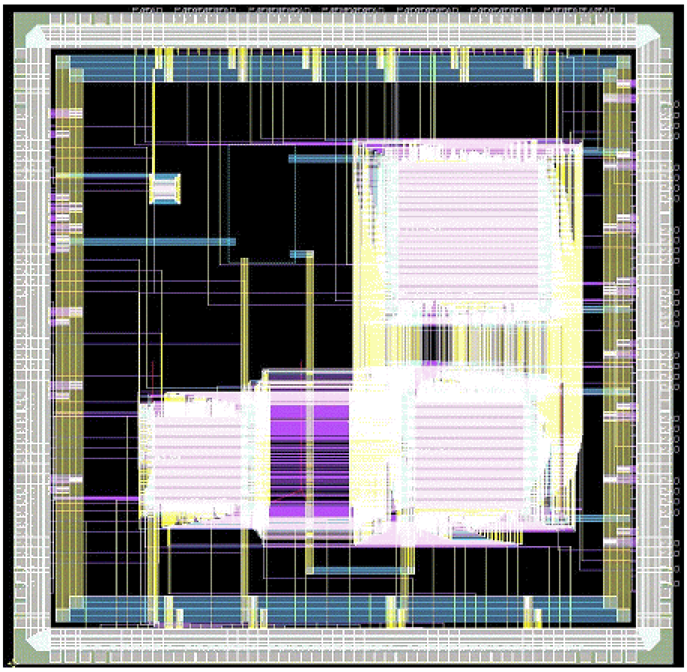

Fig. 6. P&R result using the standard cell library

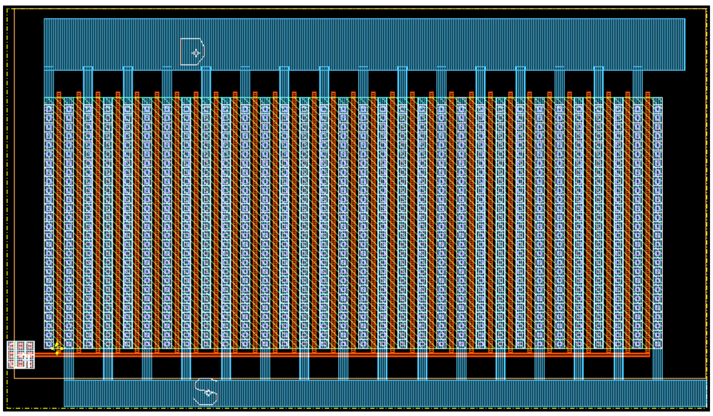

Fig. 7. PMOS cut-off switch

3 Simulation Results

In deep submicron fabrication technologies below 0.13㎛, static power due to leakage current dominates total power consumption. Therefore, it is essential to calculate both dynamic and static power to evaluate power efficiency of the proposed multiplier. In this paper, 0.13㎛ and 0.09㎛ TSMC standard cell library technologies are used in the power simulation. These technologies provide both dynamic and static power simulation.

We designed the proposed multiplier with Verilog HDL description. We synthesized two versions, 0.13㎛ and 0.09㎛, from the identical Verilog HDL description. Synopsys Design Compiler is used in the synthesis. It also extracts gate level netlist and delay information which are dumped into Verilog-format netlist (NETLIST) file and standard delay format (SDF) file, respectively. Mentor Graphics Modelsim generates two random 32bit input vectors as multiplicands, and performs behavioral simulation of the proposed multiplier. Then it dumps internal signal transition during behavioral simulation into value change dump (VCD) file. Power consumption of the proposed multiplier was simulated by Synopsys Prime Power. It reads power models in the standard cell library, and then calculates both dynamic and static power consumption using NETLIST, SDF, and VCD files. Fig. 8 shows a screen shot of power simulation using Synopsys Prime Power.

In the simulation, we assumed that the proposed multiplier runs at 333MHz. Supply voltage is assumed to be 1.08V in 0.13㎛ technology and 0.9V in 0.09㎛ technology, respectively. We carried out two low-power methods. The conventional clock gating [12] inserts some clock control logics in the clock driver, and disables clock transition when the block idles. Dynamic power consumption is zero in clock gating, but static power consumption cannot be reduced. On the contrary, the proposed block-wise shutdown [11] cuts off the supply voltage when the block idles, and both dynamic power and static power become zero.

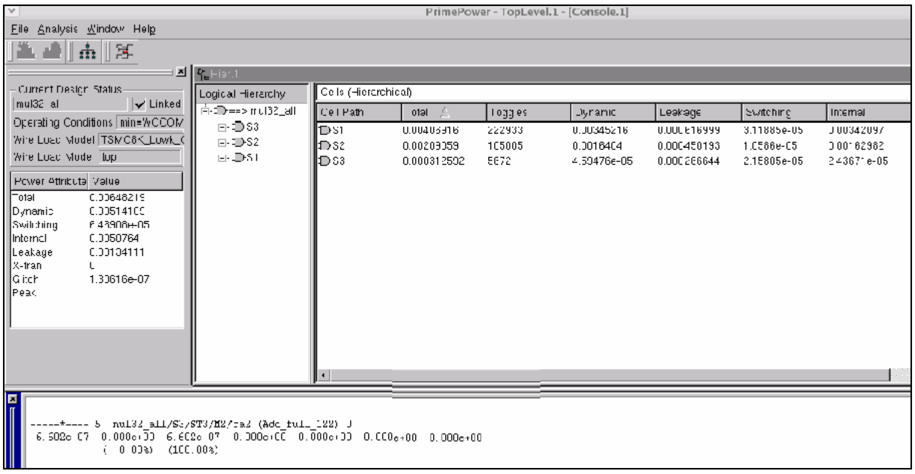

Fig. 8. Screen shot of power simulation using Synopsys Prime Power

Fig. 9 shows the power consumption of the proposed multiplier in active mode. In 0.13㎛ technology, combinational logics consume 5.156mW (29.76%), and pipeline registers consume 11.772mW (67.96%). Static power consumption is 0.393mW (2.28%). Consequently, static power is negligible in 0.13㎛ technology. In 0.09㎛ technology, the situation is quite different. Combinational logics consume 1.023mW (13.19%), and pipeline registers consume 5.396mW (69.55%). Static power consumption is 1.339mW (17.26%). As a result, static power is quite comparable to dynamic power in 0.09㎛ technology. Note that static power increases significantly as fabrication technology becomes small.

Fig. 10 shows power reduction efficiency of the proposed multiplier. In idle mode, two low-power methods, i.e. conventional clock gating [12] and proposed block-wise shutdown [11], are compared. In 0.13㎛ technology, the proposed multiplier consumes 17.5mW (100%), 0.436mW (2.49%), 0.013mW (0.07%) in active mode, idle mode with clock gating, and idle mode with block-wise shutdown, respectively. In 0.09㎛ technology, it consumes 7.785mW (100%), 1.334mW (17.14%), 0.006mW (0.08%) in active mode, idle mode with clock gating, and idle mode with block-wise shutdown, respectively.

In active mode, the proposed multiplier consumes both dynamic and static power. In idle mode with clock gating, dynamic power is greatly reduced, while static power is not reduced at all. Dynamic power is not zero, since input vector signal transition induces gate capacitance charging and discharging. In idle mode with block-wise shutdown, it consumes only dynamic power of cut-off controller, static power of cut-off controller, and dynamic power for gate capacitor charging and discharging. As shown in Fig. 10, block-wise shutdown is more effective than clock gating in power reduction. Furthermore, clock gating inserts control gates into clock distribution network, which may increase clock delay and clock skew. Note that power efficiency of clock gating degrades as fabrication technology becomes small, while that of block-wise shutdown does not depend on fabrication technology.

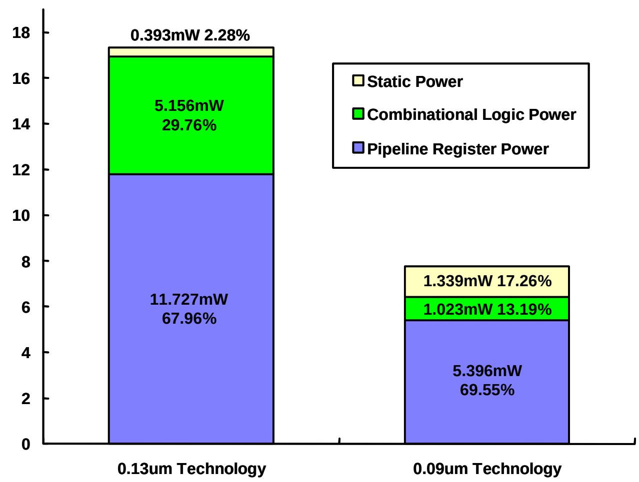

Fig. 9. Power consumption of the proposed multiplier in active mode

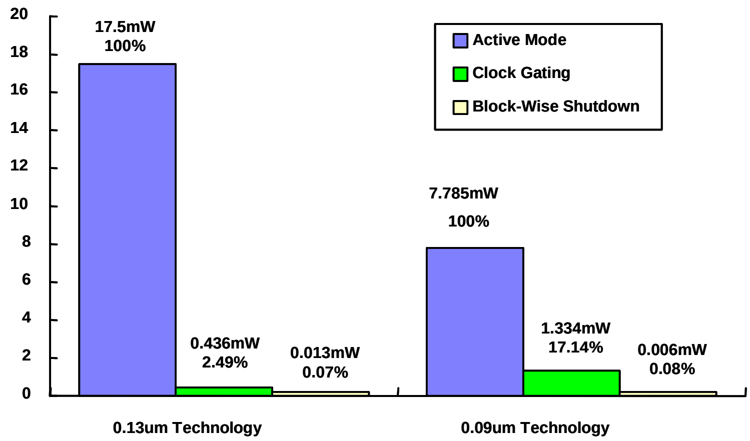

Fig. 10. Power reduction efficiency of the proposed multiplier

4 Conclusion

In this paper, we proposed a low-power 32bit × 32 bit multiplier with pipelined block-wise shutdown scheme. Using MTCMOS technology, it shutdowns supply voltage to reduce both dynamic and static power in idle mode. It has three pipeline stages for high speed operation. Supply voltage is cut off along with pipeline stage to reduce power line noise during wake up process. Partitioning of pipeline stage is determined by equalizing the number of gates in each stage in order to reduce the number of maximum simultaneous switching gates, because power line noise is proportional to it. Supply voltage of each stage is cut off by large PMOS switch. Channel width is optimized by considering the power consumption of each pipeline stage. Cut-off controller generates pipelined control signals to cut off these PMOS switches in sequential manner. The proposed multiplier is described in Verilog HDL and fabricated in standard cell library. Total gate count is about 22400 gates including cut-off controller.

Static power consumption increases significantly in deep submicron fabrication technology beyond 0.13㎛. We carried out power simulation in 0.13㎛ and 0.09㎛ technologies. In 0.13㎛ technology, the proposed multiplier consumes 17.5mW in active mode and 0.013mW in idle mode. In 0.09㎛ technology, it consumes 7.785mW in active mode and 0.006mW in idle mode. In idle mode, it reduces power consumption to 0.07%~0.08%, while the conventional clock gating scheme reduces it to 2.49%~17.14%. Power efficiency of the conventional clock gating scheme severely degrades as fabrication technology becomes small, while that of the proposed multiplier is hardly affected. This comes from the fact that the proposed multiplier significantly reduces static power due to leakage while the conventional clock gating cannot. The low-power design methodology in the proposed multiplier can be easily adopted in most functional blocks with pipeline architecture such as arithmetic logic unit, filter and systolic array.

References

1. Sakurai, T.: Perspectives on Power-Aware Electronics, Technical Digest of International Solid-State Circuit Conference (2003) 26-29.
2. Kao, J., Narendra, S., Chandrakasan, A.: MTCMOS Hierarchical Sizing Based on Mutual Exclusive Discharge Patterns, Proceedings of Design Automation Conference (1998) 15-19.
3. Srivastava, M., Chandrakasan, A., Brodersen, R.: Predictive System Shutdown and Other Architectural Techniques for Energy Efficient Programmable Computation, IEEE Transactions on VLSI Systems **4** (1996) 42-55.
4. Benini, L., Bogliolo, A., De Micheli, G.: A Survey of Design Techniques for System-Level Dynamic Power Management, IEEE Transactions on VLSI Systems **8** (2000) 299-316.
5. Moore, G.: No Exponential is Forever: But Forever Can Be Delayed, Technical Digest of International Solid-State Circuit Conference (2003) 20-23.
6. Mutoh, S., Shigematsu, S., Gotoh, Y., Konaka, S.: Design Method of MTCMOS Power Switch for Low-Voltage High-Speed LSIs, Proceedings of Asia South Pacific Design Automation Conference (1999) 113-116.
7. Usami, K. et al.: Automated Selective Multi-Threshold Design for Ultra-Low Sleep Application, Proceedings of International Symposium on Low-Power Electronics and Design (2002) 202-206.
8. Anis, M., Mahmoud M., Elmasry, M.: Efficient Gate Clustering for MTCMOS Circuits, Proceedings of International ASIC/SOC Conference (2001) 34-38.
9. Van Der Meer, P., Staveren, A.: Effectivity of Standby-Energy Reduction Techniques for Deep Sub-micron CMOS, Proceedings of International Conference on Circuits and Systems (2001) 594-597.
10. Grochowski, E., Ayers, D., Tiwari, V.: Microarchitectural di/dt Control, IEEE Design & Test of Computers **20** (2003) 40-47.
11. Choi, J., Kim, Y., Wee, J., Lee, S.: Pipelined Wake-Up Scheme to Reduce Power line Noise for Block-Wise Shutdown of Low-Power VLSI Systems, IEICE Transactions on Electronics **87** (2004) 629 - 633.
12. Benini, L., Siegel, P., De Micheli, G.: Saving Power by Synthesizing Gated Clocks for Sequential Circuits **11** (1994) 32-41.