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Ultralow-*k*/Cu Damascene Multilevel Interconnects Using High Porosity and High Modulus Self-Assembled Porous Silica

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We introduced a high porosity ultralow-*k* film into a Cu damascene interconnect without increasing the dielectric constant (k) of a low-*k* film after interconnect formation. A high elastic modulus (9 GPa) with ultralow-*k* value (<2.1) was achieved by using a self-assembled porous silica film formed with UV irradiation and a silylation anneal. Performing the silylation anneal after trench etching results in recovery of the k value and dielectric properties. A sidewall protection process carried out before metalization protects the low-*k* film against process-induced damage. The time-dependent-dielectric breakdown lifetime is 10 years at a high electric field of 2.3 MV/cm.
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To reduce signal propagation delay and power consumption, the time constants of Cu interconnects in large-scale integrations (LSIs) must be improved, which can be achieved by using ultralow dielectric constant (k) interlayer dielectrics (ILDs) between the interconnects. Reducing the density of a dielectric material lowers the k value of the dielectric film. However, it also causes an unacceptable reduction of mechanical strength. Self-assembled porous silica (Po-SiO) is a promising material for forming low-*k*/Cu damascene interconnects with high porosity and high mechanical strength, which can be extended over several generations of technology nodes.[1-4] In this study, we introduced self-assembled Po-SiO into low-*k*/Cu damascene multilevel interconnects and investigate the feasibility of a low-*k*/Cu damascene process for 200 nm pitch multilevel interconnects with 65 nm node technology.

Comparison of Effective Dielectric Constants

Effective k (k_{eff}) values of stacked ILD films for 100 nm pitch multilayered Cu damascene interconnects are shown in Fig. 1a. k_{eff} is calculated by using a two-dimensional capacitance simulator (Maxwell). The calculation process was as follows: The parasitic capacitance of an electrode (line) of a sample interconnect structure was calculated by using the simulator and by fitting the capacitance of a monolithic dielectric ($k = k_{eff}$)/Cu interconnect with changing k_{eff}. Figure 1 shows the cross section of the compared Cu interconnect structures with the Po-SiO film as a line and via low-*k* layers and with an air gap as a line low-*k* layer. The air gap structure must be thick enough for the cap film to avoid unlanded via issues due to lithography misalignment.[5] For the air gap structure, only a high modulus dielectric can be used for the cap layer and via low-*k* layer, as shown in Fig. 1b and Table I. The k_{eff} value using a conventional cap film ($k = 3.0$) and an etch-stop film ($k = 4.0$) can be reduced from 3.3 to 2.45 by applying an advanced Po-SiO film ($k = 1.9$), as shown in Fig. 1a. With a conventional k value and thick (45 nm) cap film, the k_{eff} of the proposed air gap structures is 2.66. Therefore, the k_{eff} value of the Po-SiO interconnect can be lower than that of the air gap interconnect if the same cap and etch-stop films are used.

Experimental

A self-assembled scalable Po-SiO film was formed, followed by a Xe excimer UV irradiation at 172 nm and silylation annealing with a mixed gas of 1,3,5,7 tetramethylcyclotetrasiloxane (TMCTS) vapor and nitrogen at 350°C.[1,6,7] The fabrication process of the Po-SiO film is shown conceptually in Fig. 2. A silicon substrate was spin-coated with a precursor of silica oligomer, which consists of tetraethylorthosilicate and a surfactant of block copolymers. The block copolymers formed micelles and grew as a result of the condensation of the solution during spin coating. The micelles were decomposed, leaving pores in the polymerized silica skeletal structure during calcination at 350°C in nitrogen atmosphere. The UV irradiation at 350°C and silylation anneal reinforced the mechanical strength of the silica skeletal structure and improved the hydrophobicity of the inner pore surface.

Young's modulus (E) of the blanket film was measured by nanoindentation measurement.[8] The Poisson coefficient used to calculate the modulus was 0.18, which is about the same as the value of fused silica.[9] Dielectric constant (k) and leakage current characteristics of the blanket film were characterized by capacitance–voltage measurement with a mercury probing system. Pore size distribution and cumulative pore volume were obtained from an analysis of heptane adsorption on Po-SiO film (150 nm thick) on a 300 mm wafer by ellipsometric porosimetry (EP).[10] Distributions of the resistance properties of the interconnect were obtained under the condition of a constant current of 0.1 mA. Capacitances of damascene interconnects were obtained under the condition of dc bias voltage of 1 V and ac signal frequency of 1 MHz. Leakage current was obtained from the current–voltage sweep measurement. High resistance spots in a wiring pattern were investigated by using an optical-beam-induced resistance change (OBIRCH) tool. The existence of copper clusters in a low-*k* film was investigated by high angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and energy-dispersive X-ray spectroscopy.

Sample Structure

The fabricated low-*k*/Cu damascene interconnects consist of stack films as ILD films, as shown in Table II. Po-SiO-ILD was fabricated by sequentially depositing an etch-stop film, Po-SiO film, and SiOC film as a cap film. SiOC-ILD was fabricated by sequentially depositing an etch-stop film and SiOC film. Porous-SiOC-ILD was fabricated by sequentially depositing an etch-stop film, porous SiOC film, and SiO_2 film. The etch-stop film was a stack of SiCN and SiC films formed by plasma-enhanced chemical vapor deposition (PECVD) with methylsilane and NH_3 gases and a precursor of organosiloxane without oxidant, respectively. The SiOC film was deposited by PECVD using ethoxymethylsiloxane. The porous

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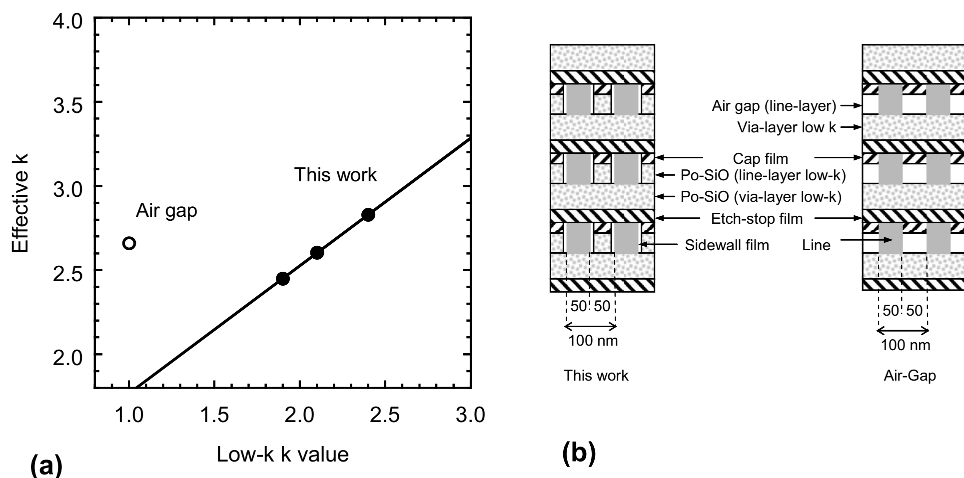

Figure 1. Comparison of effective k value of dielectric films for 100 nm pitch multilayer Cu damascene.

Table I. Thickness and dielectric constant for calculated k_{eff} of low-k/Cu interconnect.

	Po-SiO						Air gap	
Film	Thickness (nm)	k	Thickness (nm)	k	Thickness (nm)	k	Thickness (nm)	k
Cap film	20	3.0	20	3.0	3.0	3.0	45	3.0
Line layer low-k	70	2.4	70	2.1	4.0	1.9	45	1.0
Via layer low-k	60	2.4	60	2.1	60	1.9	60	3.0
Etch-stop film	20	4.0	20	4.0	20	4.0	20	4.0
SW film	5	3.7	5	3.7	5	3.7	no	no
Effective k	2.83		2.60		2.45		2.66	

Table II. Structures of ILD of the fabricated interconnects.

	Interconnect structure		
Dielectric stack	Po-SiO/Cu	SiOC/Cu	Porous SiOC/Cu
Cap film	SiOC	SiOC	SiO_2
Low-k film	Po-SiO	SiOC	Porous SiOC
Etch-stop film	SiC/SiCN	SiC/SiCN	SiC/SiCN

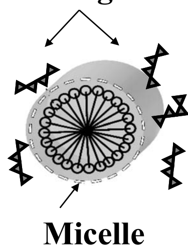

Figure 2. Concept of the formation process of the self-assembled scalable Po-SiO film.

SiOC film was deposited by PECVD using ethoxymethylsiloxane and an organic monomer. The SiO_2 film was deposited by PECVD using SiH_4 and O_2 gases. The low-k/Cu damascene interconnects were formed as shown in Fig. 3. The stack of ILD films was patterned by plasma etching with CF_4 and Ar gases with an ArF photoresist mask, as shown in Fig. 3a. The photoresist mask was removed by remote plasma ashing with hydrogen and helium gases and by wet cleaning with an organic solvent. Furnace annealing was carried out at 350°C. A mixture gas of N_2 and TMCTS vapor was used for the Po-SiO-ILD structure, as shown in Fig. 3b. N_2 gas was used for SiOC-ILD and porous-SiOC-ILD structures during annealing. A sidewall (SW) treatment process was carried out for SW protection, as shown in Fig. 3c. A SiC film was deposited by PECVD of the same chemical as the etch-stop layer, followed by

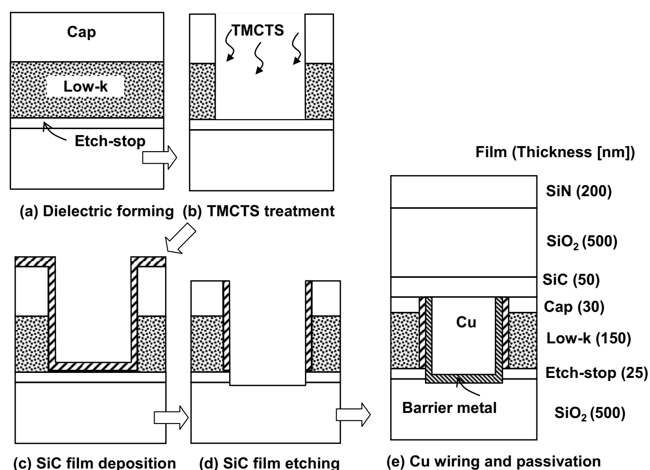

Figure 3. Process flow for formation of a Po-SiO/Cu damascene interconnect.

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Table III. Trench SW treatment process.

	Interconnect structure		
Trench SW treatment	Po-SiO/Cu	SiOC/Cu	Porous SiOC
Annealing gas	TMCTS and N_2	N_2	N_2
SW protection	Optional	No	No

anisotropic plasma etching of the SiC film and wet cleaning, as shown in Fig. 3d. Table III outlines the process. After deposition of a barrier of TaN and Ta (Ta/TaN metal), Cu sputtering, Cu plating, and chemical mechanical polishing (CMP) of Cu/Ta/TaN metals were carried out. The SiC/SiCN stack film, SiO_2 film, and PECVD-SiN film were sequentially formed as a passivation layer, as shown Fig. 3e.

Results and Discussion

Characteristics of Po-SiO film.— Figure 4 shows the EP measurement of the Po-SiO film. The porosity of 50% and pore diameter of 3.6 nm were obtained for a Po-SiO film with $k = 2.03$ and $n = 1.20$, respectively. Young's moduli of Po-SiO films decreased with decreasing k values, as shown by black circles in Fig. 5. These plots show the values for films formed by changing the molar ratio of the template surfactant of a silica oligomer, and then UV-irradiated at 8.4 J/cm^2. The moduli of the Po-SiO film using the same oligomer increased with increasing UV irradiation without an increase in the k value, as shown by white circles in Fig. 5. Kim et al. suggested the disadvantage of using UV irradiation for a porous low-k film due to the nonuniform mechanical stress in the film.[11] The UV irradiation of Po-SiO contributes to improving the properties due to the highly porous structure of Po-SiO and the following silylation anneal with TMCTS. TMCTS can reinforce the mechanical strength with cross-linking at defect sites on a pore surface and reach all of the pores due to the high porosity structure of the Po-SiO film. The estimated modulus of the pore wall material (E_W) reached 40 GPa.[12] The modulus of SiOC and porous SiOC, which were deposited by using the same precursor, are on the same E_W line and are lower than 23 GPa. Figure 6 shows the dielectric constant vs porosity for Po-SiO

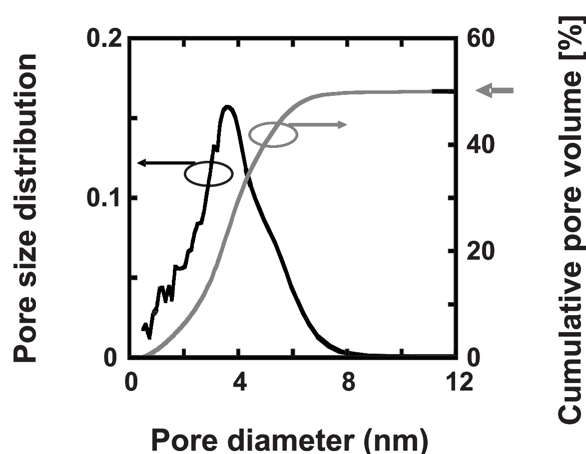

Figure 4. Pore size distribution and cumulative pore volume of Po-SiO.

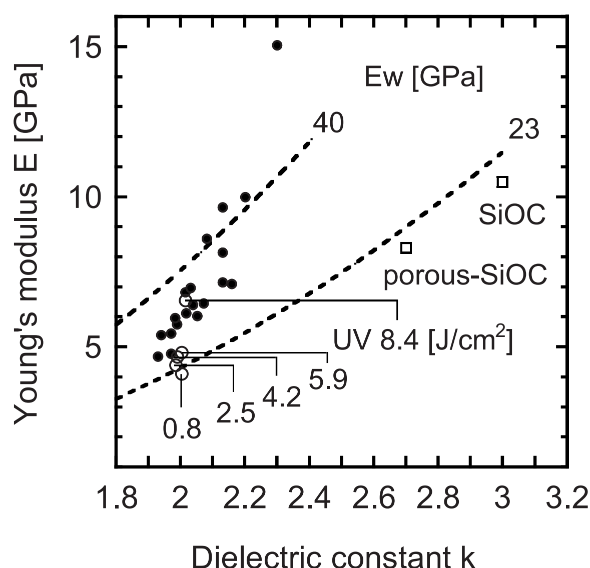

Figure 5. Young's modulus vs dielectric constant of Po-SiO films.

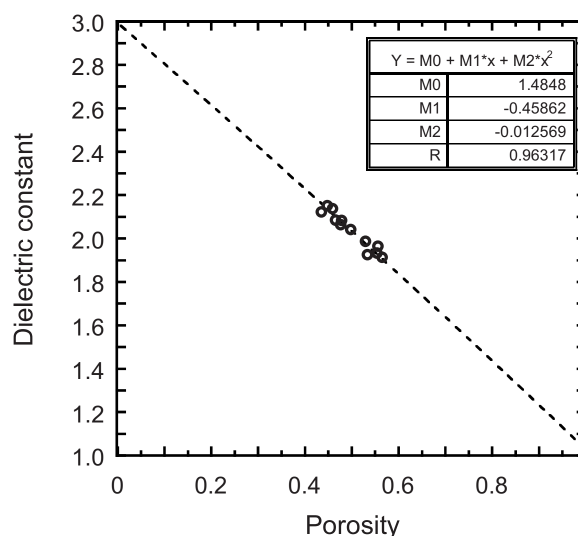

Figure 6. Dielectric constant vs porosity for porous silica films.

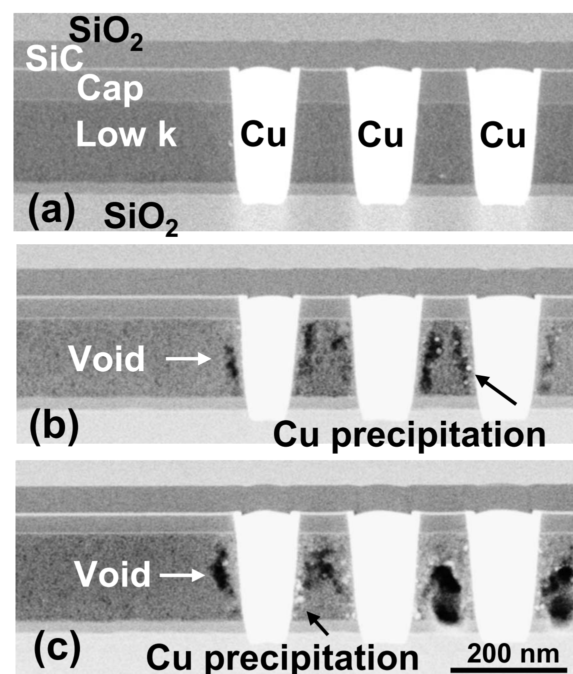

Figure 7. Cross-sectional HAADF-STEM micrographs of Po-SiO/Cu damascene structures: (a) Treated by optimized silylation anneal, (b) weak treatment, and (c) untreated.

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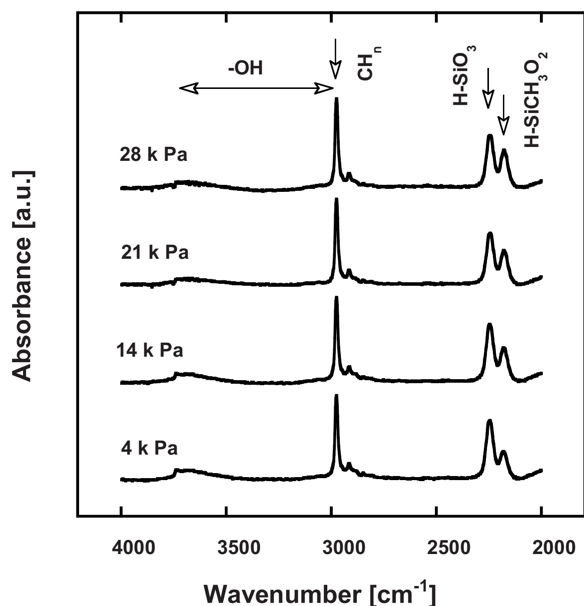

Figure 8. FTIR spectra of Po-SiO film as a parameter of pressure of TMCTS vapor treatment.

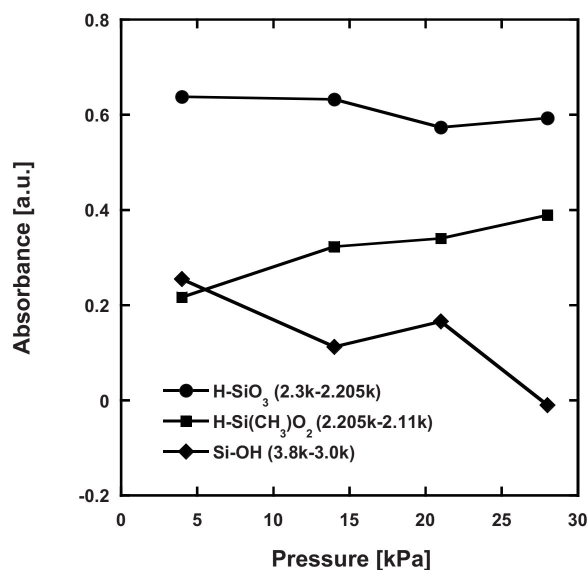

Figure 9. Peak area of FTIR spectra assigned to $H–SiO_3$, $H–Si(CH_3)O_2$, and Si–OH as a function of pressure of TMCTS treatment.

films with different surfactant concentrations. The dielectric constant decreases with increasing porosity. The porosity (P) was calculated by the Lorentz–Lorenz equation as

$$P = 1 - \frac{(n_{PS}^2 - 1)}{(n_{PS}^2 + 2)} \cdot \frac{(n_{SiO_2}^2 + 2)}{(n_{SiO_2}^2 - 1)}$$

where n_{PS} is the refractive index of Po-SiO and n_{SiO_2} is the refractive index of SiO_2, the value of which is assumed to be 1.46.[13] The dotted line is the result of fitting with a quadratic function, as shown in the inset of Fig. 6. The projection of the k value of a dense film (porosity = 0) is 3.0, which suggests that Po-SiO becomes closer to SiOC as the concentration of surfactant is reduced.

Effect of silylation hardening.— Figure 7a-c is the cross-sectional HAADF-STEM micrographs of Po-SiO/Cu damascene interconnects. Bright areas are assigned to heavy metal because the intensity of the secondary scattered electron in HAADF-STEM is proportional to the square of the atomic number of the scattering material. The sample treated with an optimized TMCTS silylation anneal after etching showed no dark areas and a few bright regions in the low-k film (Fig. 7a). The bright spots were assigned to metal contamination from the sample holder. These results indicate that there were no low-k voids and no Cu precipitation in the ILD treated with optimized TMCTS silylation anneal. However, a cracklike void along the side of the lines and Cu precipitations on the void surface were observed in the sample treated with TMCTS with an inhibitor, as shown in Fig. 7b. More serious deformation of large voids occurred without TMCTS treatment after trench patterning of the ILD, as shown in Fig. 7c. These results indicate that the TMCTS coverage on the surface of the Po-SiO prevents Cu penetration. Figure 8 shows Fourier transform infrared (FTIR) absorbance of Po-SiO films with the gas pressure of the TMCTS treatment as a parameter. As the TMCTS gas pressure increased, the broad peak from 3000 to 3740 cm^{-1} decreased, indicating that water adsorption was suppressed. $H–(CH_3)O_2$ at 2175 cm^{-1} increased, while $H–SiO_3$ at 2232 cm^{-1} stayed constant as the pressure increased, indicating that the pore surface was covered with TMCTS. The peak intensities of the chemical bonds vs TMCTS gas pressure are shown in Fig. 9. The TMCTS particles were generated as the pressure increased, as shown in Fig. 10a, whereas the porosity and dielectric constant did not change, as shown in Fig. 10b. This would indicate that as the TMCTS pressure increased, a vapor phase reaction occurred, resulting in the formation of TMCTS particles in the vapor due to agglomeration. Consequently, the TMCTS gas pressure from 4 to 14 kPa was the optimum condition with respect to particle density, cross-linkage, and moisture adsorption. The dielectric constant and the porosity did not change very much with increasing pressure.

Effect of SW protection film.— An SW film was formed after the silylation step, followed by anisotropic etching. The SW formation process should provide significant step coverage and not damage the low-k film. The direct deposition of SiC on blanket Po-SiO caused a

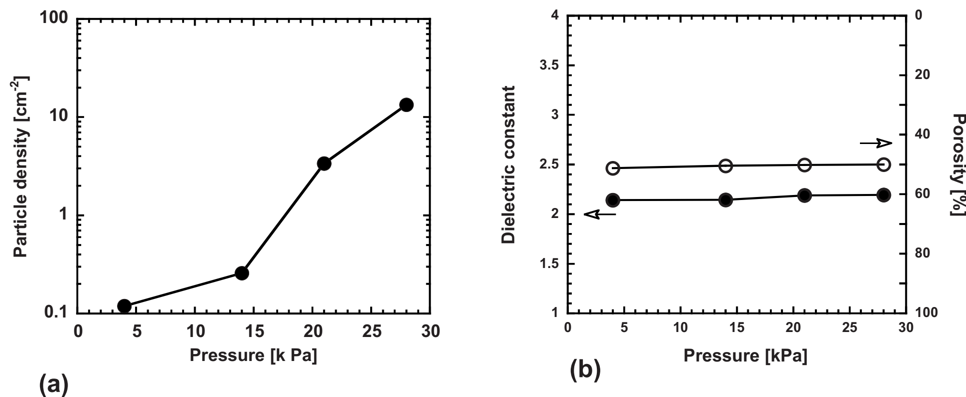

Figure 10. (a) Particle density on Si wafer and (b) dielectric constant and porosity of Po-SiO treated by TMCTS as a function of treating pressure.

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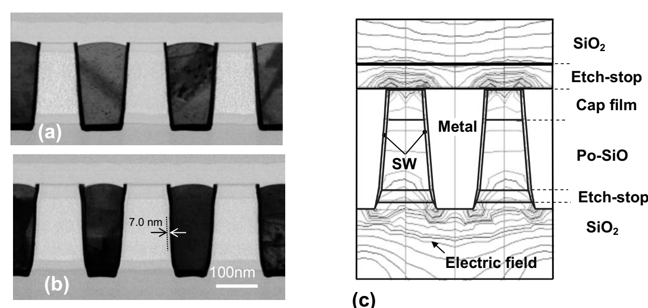

Figure 11. Cross-sectional TEM micrographs: (a) Without SW protection for 100 nm spacing, (b) 7 nm SW protection for 100 nm spacing, and (c) two-dimensional capacitance simulation to derive the dielectric constant of the ILD films.

small increase in the k value (+0.16) of the Po-SiO film. Figure 11a shows a cross section transmission electron microscopy (TEM) image of a Po-SiO/Cu interconnect without SW formation. The interline spacing increased 14 nm due to the 7 nm thick SW formation, as shown in Fig. 11b. The SW forming process provided sufficient conformality with coverage of 35% (=remaining SW thickness/deposited top thickness). A two-dimensional capacitance simulation was carried out to derive the k values of the Po-SiO in a sample. The dimensions and capacitances for the calculation were measured from the same samples. An image of a calculated electric field in a Po-SiO-ILD system with an SW film is shown in Fig. 11c. The k values of the Po-SiO layers of the Cu damascene increased from 2.1 to 3.15 for the structures without SW formation and slightly increased to 2.2 those with the 4.5 nm thick SW film, as shown in Table IV. Adsorption of moisture could occur during the damascene fabrication; however, moisture does not penetrate the Po-SiO layer during Cu plating because the SW film is formed before sputtering. Figure 12 shows the cumulative probabilities of interline capacitances for 100, 120, and 140 nm spacing with and without the SW film. The distributions are sharp for every pattern. The median capacitances for 100, 120, and 140 nm spacing with the SW films are less than those for the patterns without them by 20.5, 18.2, and 16.3%, respectively. The SW formation contributed to effectively reducing the interline capacitance for narrower spacing.

Figure 13 shows a fabricated seven-layer Po-SiO/Cu damascene stack, which is equivalent to a four-layer single damascene interconnect. No serious problems, such as delamination during the CMP process, were observed. This suggests that the Po-SiO/Cu damascene process provides possible adhesion/cohesion properties that would be useful for multilevel interconnect mass production.

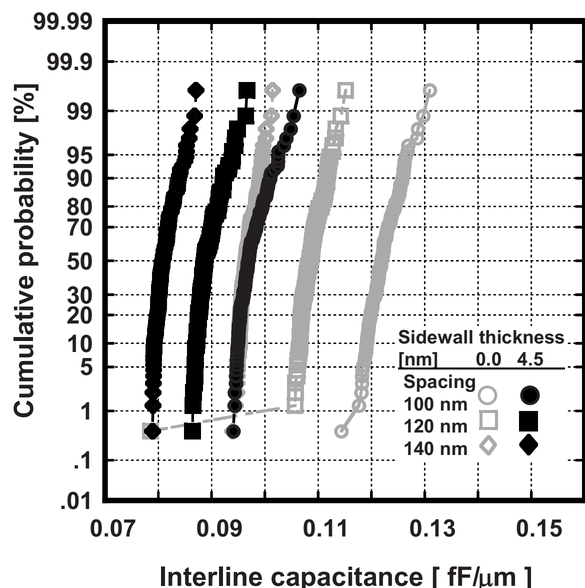

Figure 12. Cumulative probability of interline capacitance for the spacing of 100 nm pattern with and without SW protection as a parameter of spacing.

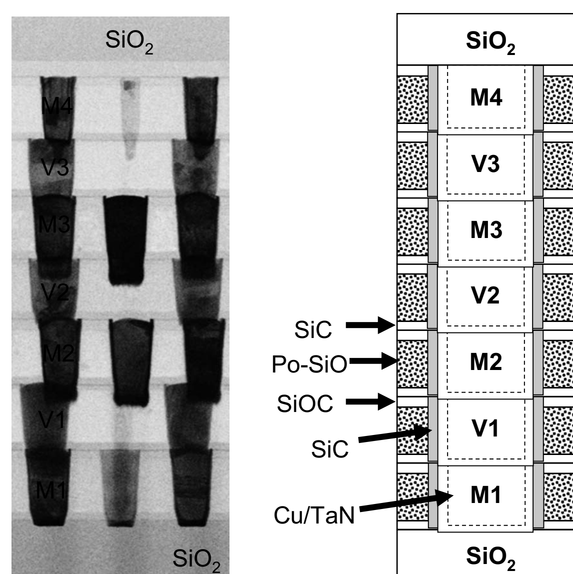

Figure 13. Cross-sectional TEM micrograph of four-layer Po-SiO/Cu damascene.

Figure 14a shows the calculated k_{eff} of the ILD system with SW formation as a function of the k value of the Po-SiO layer in the ILD system. The Po-SiO layer is between the lines and the porous SiOC layer is between the vias in the Cu damascene structure, as shown in

Table IV. Dielectric constants of films used for two-dimensional capacitance simulation.

Films	Dielectric constant		
	Best fit value for SW protection structure	Best fit value for without SW protection structure	Measured k value for blanket film
Po-SiO	2.2	3.15	2.1
Cap SiOC	3.0	3.0	3.0
SiO_2	4.2	4.2	4.2
SW SiC	3.7	3.7	3.7
Etch-stop SiC/SiCN	4.0	4.0	4.0

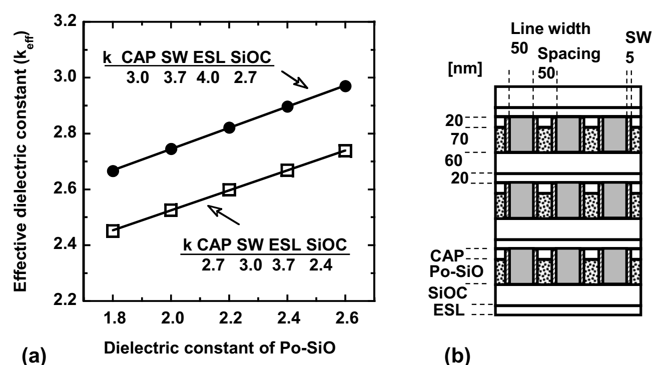

Figure 14. Effective dielectric constants of ILD films as a function of the dielectric constant of Po-SiO.

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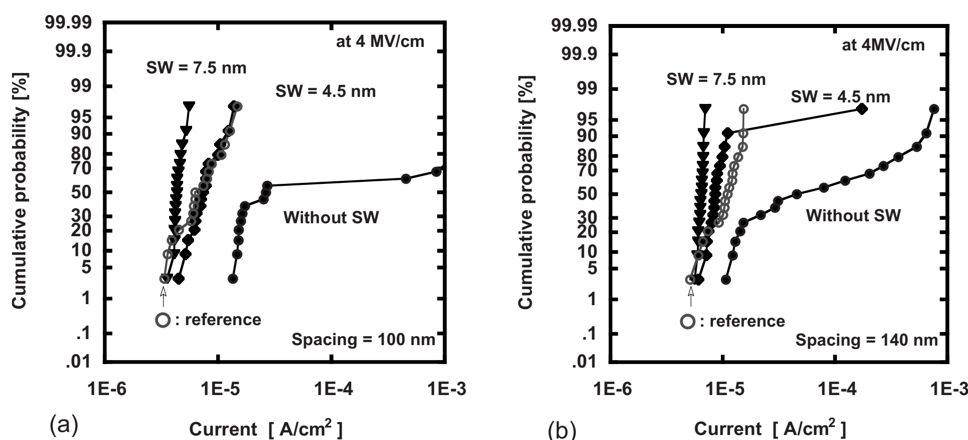

Figure 15. Cumulative probability of interline-leakage current with and without SW protection. (a) Interline spacing is 100 nm and (b) interline spacing is 140 nm.

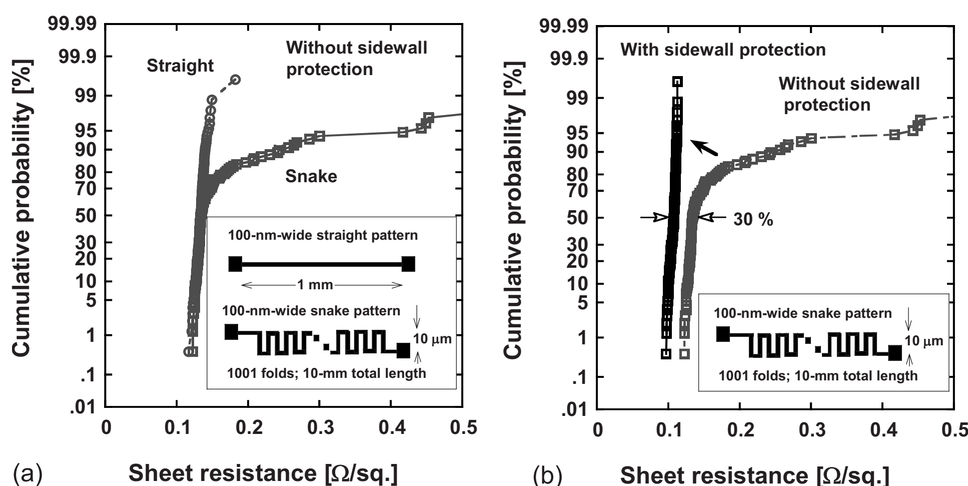

Figure 16. Cumulative probability of sheet resistance. (a) Straight and snake pattern of Po-SiO/Cu without SW protection and (b) snake pattern with and without SW protection.

Fig. 14b. Closed circles show the k_{eff} values of ILD systems using conventional films. k_{eff} is 2.82 with the Po-SiO ($k = 2.2$) and conventional films, such as a cap film ($k = 3.0$), a SiC SW film ($k = 3.7$), an etch-stop film ($k = 4.0$), and a SiOC ($k = 2.7$). The k_{eff} values can be reduced to 2.60 with the Po-SiO ($k = 2.2$) and advanced films, such as a cap film ($k = 2.7$), an SW film ($k = 3.0$), an etch-stop film ($k = 3.7$), and a SiOC ($k = 2.4$), as shown by the open square plots in Fig. 14a.

Cumulative probabilities of interline-leakage current as a parameter of the SW film thickness are shown in Fig. 15a and b for spacings of 100 and 140 nm, respectively, with reference data obtained from a SiOC/Cu damascene structure without SW protection. The measurement was performed at a high electric field of 4 MV/cm to investigate the current at the pore surface caused by some kind of ionic attachment due to the process, such as moisture adsorption. This type of leakage current is obvious at high electric field because the conduction process is expressed by the field emission process[14] as

$$J \propto V^2 \exp(-b/V)$$

where J is the current, V is the applied voltage, and b is the positive constant. Median values of the leakage current of the Po-SiO/Cu structure with SW protection and SiOC/Cu without it were the same levels (lower 10^{-5} A/cm^2) for the 100 and 140 nm spacing. However, the current of Po-SiO/Cu without SW protection was obviously high and distributed to a higher level for both spacing structures. This indicates an influence of moisture adsorption in the Po-SiO-ILD system without SW protection.

Figure 16a shows the cumulative probability of sheet resistance of isolated straight and dense snake wirings of the Po-SiO/Cu damascene interconnect without SW protection. The distribution is sharp for the straight patterns. However, the distribution for the snake patterns spreads to higher resistance. Figure 16b shows the cumulative probability of the sheet resistance of the dense snake wirings with and without SW protection. The SW protection structure improved the uniformity in the sheet resistance distribution. The median resistance was reduced by 30%, also due to the SW film formation. Figure 17 shows an OBIRCH observation. Localized high resistant spots were observed around the folds of the snake pattern by OBIRCH, as shown in Fig. 17a and b. From the plan-view TEM observation (Fig. 17c), we identified the spot as a large Cu void, and

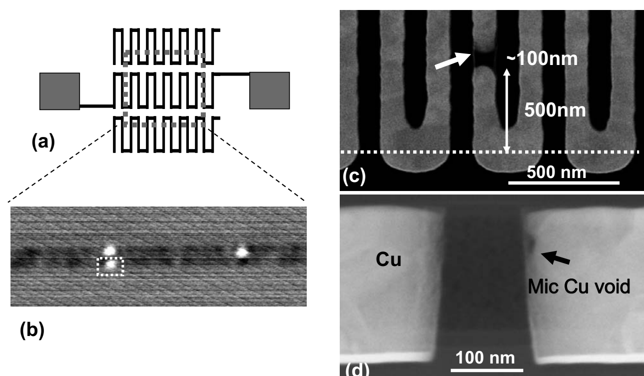

Figure 17. Failure analysis of snake patterns without SW protection. (a) Schematic layout of snake wiring, (b) OBIRCH image of a high resistance spot, (c) TEM micrograph of giant Cu void as detected by OBIRCH, and (d) microvoid located at folding portion of the pattern.

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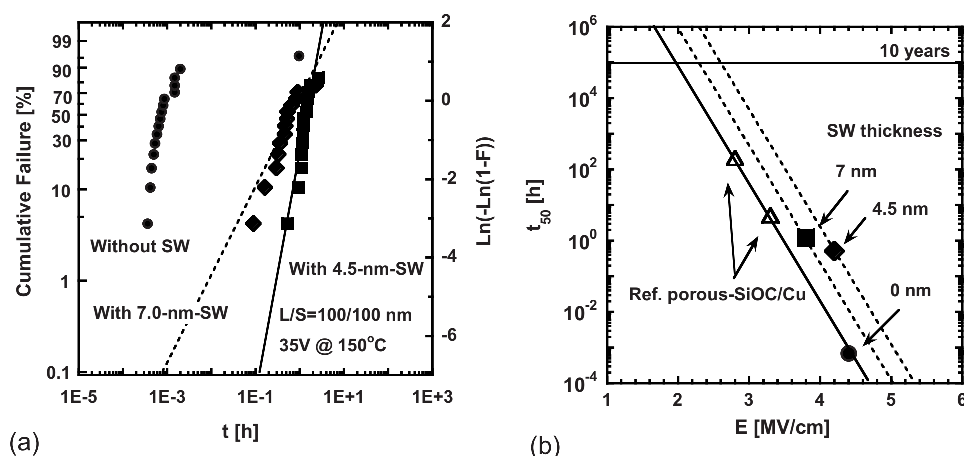

Figure 18. (a) Cumulative failure of TDDB lifetime and (b) estimated t_{50} TDDB lifetime as a function of applied electric field.

only barrier metal layers remained at both sides of the Cu line. A Cu void was observed on the side of the barrier metal layer of the folded portion in a cross section TEM image, as shown in Fig. 17d. These results suggest that the large Cu void grew due to the migration and agglomeration of voids along the SW of Cu interconnects near the folds of the wiring.

Figure 18a shows the time-dependent dielectric breakdown (TDDB) distribution of a Po-SiO/Cu interconnect of a 100 nm wide, 100 nm spacing comb pattern as a parameter of the SW film thickness at high applied voltage of 35 V and high temperature of 150°C. The largest values in the distributions are almost the same. The mean lifetime of every structure with SW protection was longer than that of the structure without it by more than three decades. This indicates that the SW film served to protect the weak portion of the porous low-k/Cu. Figure 18b shows the mean lifetime as a function of electric field. The slope of extrapolations for Po-SiO/Cu (dotted lines) was assumed to be the same as that of the reference porous SiOC/Cu structure. The extrapolation shows the lifetime of 10 years under the stress of 2.3 MV/cm.

Conclusion

A high porosity, low-k structure effectively works to maintain the ultralow-k property of the self-assembled Po-SiO film through Cu damascene integration. We achieved a high elastic modulus (9 GPa) with an ultralow-k value (<2.1) by using UV irradiation and a silylation anneal, and confirmed that no degradation of mechanical strength occurred due to the integration. Performing the silylation anneal after trench etching resulted in the recovery of the k value and dielectric properties. An SW protection process carried out before metalization protects the low-k film against process-induced damage. The electrical properties and reliability of the Po-SiO/Cu damascene interconnect are sufficient for mass production LSI application.

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