ECS Transactions, 3 (8) 75-80 (2006)
10.1149/1.2356337, copyright The Electrochemical Society

Front and Back Channel Properties of Asymmetrical Double-Gate Polysilicon TFTs

F. V. Farmakis[a], D. N. Kouvatsos[a], A. T. Voutsas[b], D. C. Moschou[a], G. P. Kontogiannopoulos[a], and G. J. Papaioannou[c]

[a] Institute of Microelectronics, NCSR Demokritos, Agia Paraskevi 15310, Greece
[b] LCD Process Technology Laboratory, Sharp Labs of America, 5700 NM Pacific Rim Boulevard, Camas, Washington 98607, USA
[c] Department of Physics, University of Athens, Athens 15784, Greece

Polycrystalline silicon TFTs with different front- and back-gate lengths are investigated. In addition, the laser annealing process yields high quality directional grains that enable us to orient TFT channels parallel or perpendicular to the grain boundaries. It is demonstrated that double-gate TFTs are fully depleted and therefore back interface properties exert critical influence to the overall TFT electrical performance. More specifically, it is demonstrated that the back interface contains a large number of defects, resulting in a deterioration of carrier conductance.

Introduction

Polycrystalline silicon thin film transistors (TFTs), fabricated at low temperatures, are essential for flat panel display applications. In particular, high resolution and small form factor displays with advanced input / output functions can only be realized by high performance TFTs fabricated at low temperatures (1). Breakthroughs have recently occurred in the polysilicon crystallization process using various excimer laser anneal (ELA) methods (2-4), particularly with the advent of the sequential lateral solidification technique (SLS) (5). Such advances have greatly improved TFT performance, reaching the point of allowing the use of TFTs for the monolithic integration of circuits on display substrates; thus, silicon on insulator (SOI) and system on glass applications are facilitated. The SLS ELA technique yields polysilicon films with an excellent intragrain material quality and grains with very elongated or engineered shapes. In the case of films with elongated grains, it is possible to locate the TFT channels so as to be either parallel or perpendicular to the grain boundaries.

Such monolithic integration in circuits demands absolute control of electrical TFT parameters, such as turn-on voltage, subthreshold swing and transconductance. Towards this direction, double-gate (DG) TFTs have been developed that enable electrical parameter control through the application of an electric field on the opposite gate. However, even though DG fully depleted SOI MOSFETs have been extensively studied, DG TFTs lack such an investigation. In this paper, we attempt to clarify the electrical properties of DG TFTs with asymmetrical top and bottom gates in terms of length.

Experimental

TFTs were fabricated in 50 nm thick polysilicon films, formed at low temperature by ELA crystallization of a-Si, using the SLS technique (4,5). This process results in polysilicon films with grains much longer than the TFT channel lengths, separated by roughly parallel boundaries. Moreover, the polysilicon channel was lightly doped with boron resulting in inversion-mode n-type devices. The TFTs were directed either parallel or perpendicular to the elongated direction, as shown in Figure 1. The double gate (DG) device structure consisted of self-aligned front gates, with a 30nm thick PECVD SiO_2 gate dielectric, and non-self-aligned back gates, with a 50nm thick PECVD SiO_2 gate dielectric. The channel width W was 8 μm and the front and back gate lengths L_t and L_b were 1.6 μm and 0.5-1.3 μm. In addition, top and bottom gate devices were fabricated to serve as references. The devices were characterized using a semiconductor analyzer HP4140B and a Keithley 230 voltage source, with the transfer characteristics and the parameters extracted in the linear regime (V_D=0.1 V) for both front and back channel operation.

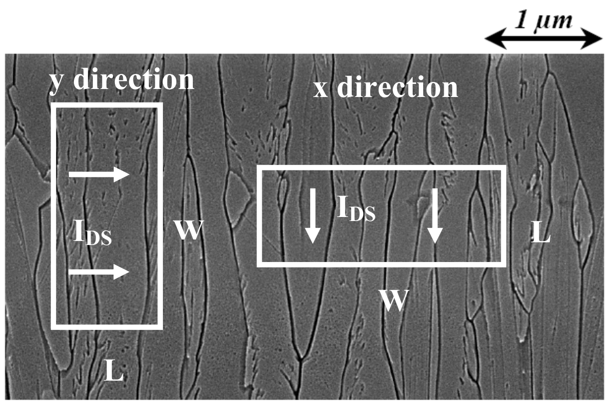

Figure 1. SEM micrograph for directional polycrystalline silicon. TFT y-direction and x direction representation is schematically shown.

Discussion

Before discussing our data it is important to note that for front operation $L=L_t$ and for back operation $L=L_b$. Since a gate mask with $L=L_t$ was used for source and drain doping, back operation TFT may be simulated as that of a TFT with $L=L_b$ connected to series resistances that may be modulated by front-gate biasing. We apply the terms "front operation" and "back operation" to indicate electrical measurements and parameter extraction having the opposite gate at constant bias.

Dependence on opposite gate biasing

Figure 2 shows the turn-on voltage dependence as a function of the opposite gate biasing for front and back operation. In both cases, we observe an almost linear behavior that reflects the polycrystalline silicon fully depleted condition, already expected from the thickness of the active layer (50 nm). Moreover, it is demonstrated that there is no effect of the TFT orientation on the turn-on voltage variation, leading to the conclusion that the grain boundary defect density can be neglected in the following analysis. It is noted that the turn-on voltage variation is more pronounced for back operation and this cannot solely be explained by the difference in gate oxides ($t_{ox,b}/t_{ox,f}$=50/30). This behavior also reflects the interface trap density difference in both interfaces ($N_{ss,f}$ and $N_{ss,b}$). For fully depleted devices (6), we can estimate $N_{ss,f}$ and $N_{ss,b}$ for devices with $L_b=L_t$ by using the following equation for front operation:

$$\Delta V_{ON,f} = -\frac{C_{ox,b} C_{Si}}{C_{ox,f}(C_{Si} + C_{ox,b} + C_{ss,b})} V_{G,b} \qquad [1]$$

where $C_{ox,f}$ and $C_{ox,b}$ represent the gate capacitances of front and back interfaces respectively, C_{Si} the silicon (in our case polysilicon) capacitance and $C_{ss,b}$ the back interface capacitance due to surface states. An analogous equation is applicable for back operation. Applying the previous equation to our data and taking into account that $C_{ss,b}=qN_{ss,b}$, we evaluate the back interface surface state density for our devices; it has values ranging from 3-6x10^{11} cm^{-2} eV^{-1}.

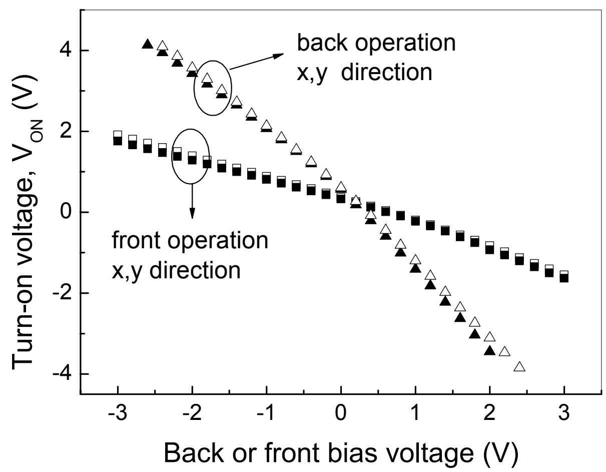

Figure 2. Turn-on voltage dependence on back or front gate bias voltage in the case of a double-gate TFT ($W/L_b/L_t$=8/0.8/1.6 μm).

However, in the case of back operation, the transfer characteristics (not shown here) indicate that the drain current is most efficiently controlled by the front gate and thus it is assumed that carriers flow mostly through the front polysilicon/SiO_2 interface. This is further supported by the high surface state density of the back interface, as evaluated above. Therefore, an equation analogous to [1] cannot be applied for back operation.

Figure 3 shows the subthreshold swing dependence on opposite gate biasing (back or front gate biasing for front or back gate operation, respectively). In the case of front operation, the subthreshold swing takes its minimum value when the back interface accumulates (holes) at around $V_{G,b}$=-1V and it remains constant for lower $V_{G,b}$ values, indicating that the drain current flows mainly along the front polysilicon/SiO_2 interface. For positive back gate bias, the subthreshold swing is drastically increased, indicating that the inversion layer becomes thicker, as shown in the following equation (7):

$$S=\frac{kT}{q}\cdot\ln 10\cdot\left[1+\frac{q^2(D_{bulk}t_{inv}+N_{ss})}{C_{ox}}\right] \qquad [2]$$

where kT is the thermal energy, q is the electron charge, D_{bulk} is the mean bulk density (eV^{-1} cm^{-3}), t_{inv} is the inversion layer thickness and N_{ss} is the surface state density in the front gate interface (eV^{-1} cm^{-2}).

In addition, the grain orientation in the device channel affects the subthreshold swing value, but not its variation with back gate bias. That is, the difference in the S value for x-oriented or y-oriented TFTs remains constant for any given $V_{G,b}$. From this observation and from equation [2] it can be inferred that the variation of t_{inv} with $V_{G,b}$ is the same for both orientations.

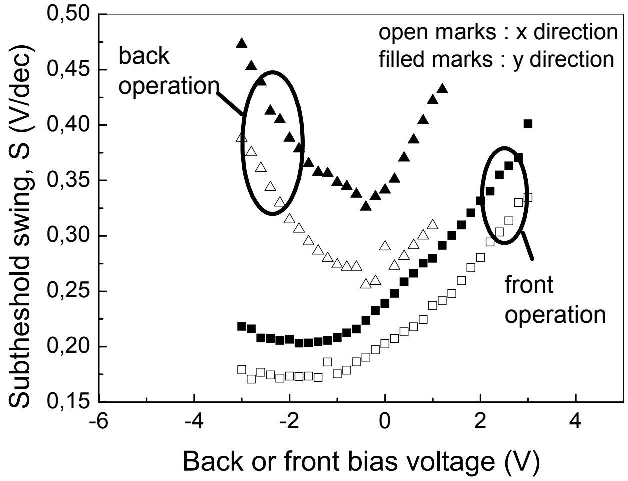

Figure 3. Subthreshold swing dependence on opposite (back or front) gate bias voltage in the case of a double-gate TFT ($W/L_b/L_t$=8/0.8/1.6 μm).

The back operation subthreshold swing dependence on front gate bias exhibits a U-shape behavior. It is noted that for accumulated front interface ($V_{G,f}$<0), the subthreshold swing is increased, demonstrating a high back interface state density, as the drain current is mainly controlled by back gate biasing. On the contrary, for inverted front interface ($V_{G,f}$>0) the subthreshold swing is also increased. Considering that in this case the current mainly flows through the front interface, one would expect a subthreshold swing improvement. However, it has to be noted that the subthreshold swing is measured from the back transfer characteristic, giving rise to an "apparent" value. This appears more evident by taking into account equation [2], where C_{ox} denotes the back oxide capacitance.

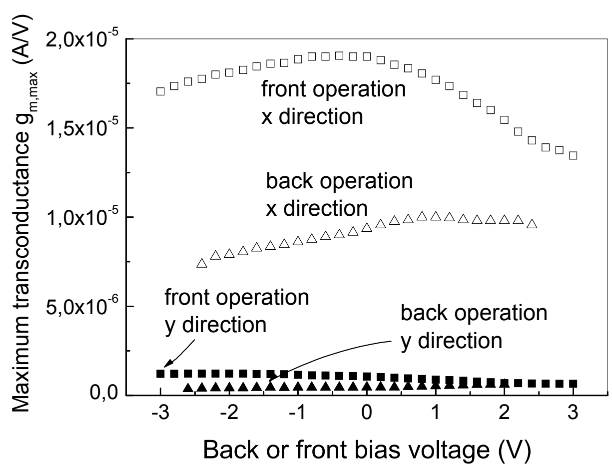

Figure 4. Maximum transconductance dependence on opposite (back or front) gate bias voltage in the case of a double-gate TFT ($W/L_b/L_t$=8/0.8/1.6 μm).

Figure 4 shows the maximum transconductance $g_{m,max}$ as a function of opposite gate biasing for front and back channel operation. In the case of front channel operation, $g_{m,max}$ is more than a decade higher in x direction than in y direction TFTs, indicating the important role of the direction of grain boundaries in device transconductance (8).

Moreover, a clear decrease in the transconductance is observed as the bottom interface reaches accumulation ($V_{G,b}$<0). This may be attributed to the increase of the electric field in the inversion region that leads to an enhanced carrier scattering in the front polysilicon/SiO_2 interface. In addition, we also observe a severe decrease of the transconductance as the bottom interface is inverted ($V_{G,b}$>0). In this situation, the current flows not only in the front interface but also deeper in the polysilicon bulk and/or the back interface and is thus affected by additional trapping mechanisms. Finally, it is also shown, that in the case of back operation, device transconductance is low and it also exhibits the same behavior regarding the grain orientation as mentioned for front operation. This further supports that back interface contains a large number of defects.

Dependence on back over front gate ratio

In order to further investigate carrier conductance through DG-TFTs, we performed electrical measurements on DG-TFTs with various L_b/L_t ratios, as well as on single bottom and front gate devices. Figure 5 shows the extracted turn-on voltage as a function of L_b/L_t ratio. Top gate (TG) and bottom gate (BG) TFT data are also added for comparison. It is observed that for front operation the turn-on voltage remains unchanged; top gate TFT exhibit the same turn-on voltage with DG-TFTs with L_b/L_t<0.5. In the case of longer bottom lengths (L_b/L_t>0.5), the turn-on voltage appears to increase almost linearly with L_b.

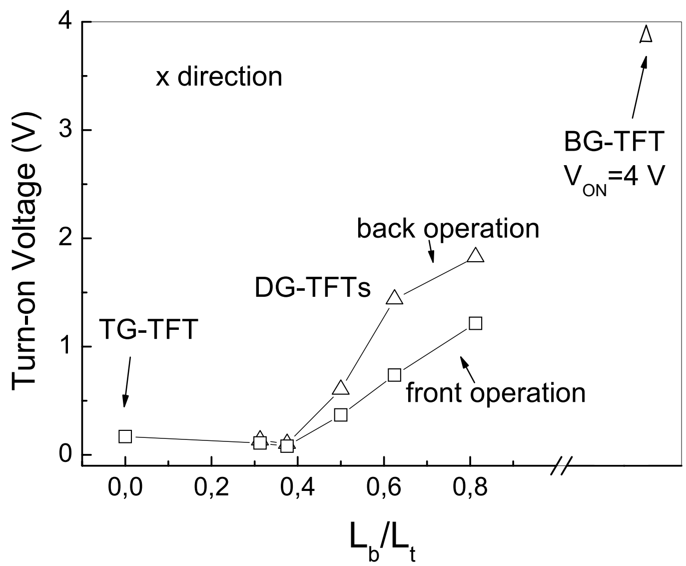

Figure 5. Turn-on voltage as a function of bottom and top channel length ratio for back and front operation. Top-gate and bottom-gate device data are also shown.

In the case of back operation, the turn-on voltage for DG-TFTs with L_b/L_t<0.5 exhibits the same behavior than for front operation. In addition, for longer bottom gates, it seems that back interface influence becomes more pronounced. Taking into account the large value of V_{ON} for BG-TFT, it is evident that the back interface defect density pins the Fermi level. Therefore, the inference that back operation in DG-TFTs is mainly due to the front gate potential is supported.

Conclusion

In this paper we investigated asymmetrical double gate TFTs for various bottom over top gate length ratios. Analysis of the electrical measurements functioning for front and back operation demonstrated that back interface contains a large number of defects that drastically modifies device electrical properties. Moreover, we suggested that for back operation drain current flows not only through the back interface but also from the bulk and/or the front interface. Finally, it was shown that grain orientation along the device channel influences mainly the transconductance and has insignificant effects on turn-on voltage.

Acknowledgments

The authors acknowledge financial support through the research project PENED 3ED550, administered by the Greek General Secretariat for Research and Technology.

References

1. T. Matsuo and T. Muramatsu, *Proc. SID Intern. Symposium*, 856, (2004).
2. S. D. Brotherton, D. J. McCulloch, J. B. Clegg, and J. P. Gowers, *IEEE Trans. Electr Dev.*, **40**, 407 (1993).
3. K. M. Chang, Y. H. Chung, G. M. Lin, C. G. Deng and J. H. Lin, *IEEE Electron Dev. Lett*., **22**, 475 (2001).
4. A. T. Voutsas, *IEEE Trans. Electron Dev*., **50**, 1494 (2003).
5. R. S. Sposili and J. S. Im, *Appl. Phys. Lett*., **69**, 2864 (1996).
6. F. Balestra, M. Benachir, J. Brini and G. Ghibaudo, *IEEE Trans. Electron Dev*., **37**, 2303, (1990).
7. M. Miyasaka and J. Stoemenos, *J.Appl.Phys*., **86**, 5556, (1999).
8. A. T. Voutsas*, Applied Surface Science* **208-209**, 250-262, (2003).