Journal of The Electrochemical Society, **153** (7) G603-G605 (2006)
0013-4651/2006/153(7)/G603/3/$20.00 © The Electrochemical Society

Suppression of Oxide Encroachment into Floating Gate by Shallow Trench Isolation Recess in an Electrically Erasable Programmable Read Only Memory Cell

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In this paper, we investigate the effects of the oxide recess in shallow trench isolation (STI) on the characteristics of electrically erasable programmable read only memory (EEPROM) cell with in situ-doped floating gate. It is found that the distribution of the program threshold voltage is improved with increasing of the oxide recess in STI. Transmission electron microscopy analysis shows that the oxide recess in STI results in the decrease of oxide thickness at the edge of STI and in the center of tunnel oxide. Also, it is observed that erase cell current is increased about 11% with oxide recess of 200 Å and 21% with oxide recess of 400 Å, respectively. Endurance measurements in the EERPROM cell reveal that both electron and charge generation increase with increasing recess depth when the cycling time exceeds about 1×10^3.
 [DOI: 10.1149/1.2196789]

Manuscript submitted May 16, 2005; revised manuscript received March 1, 2006. Available electronically May 4, 2006.

There has been increasing interest in electrically erasable programmable read only memory (EEPROM) for various embedded applications such as the smart card, microcontroller unit, and radio frequency tag.[1,2] The smart card is an especially promising area because future cards will require more intelligent and secured functions.[3,4] The important factors when EEPROM is embedded into a smart card chip are cell size and high endurance due to frequent programming and erasing operations.

One of the critical steps to fabricate an EEPROM cell is to make various insulators. It has a tunnel oxide under a floating gate and a thicker gate oxide to sustain high voltage, as well as a thinner gate oxide for low voltage operation. Also, there are oxide-nitride-oxide (ONO) triple layers between the floating gate and control gate to obtain high coupling ratio. Therefore, several thermal oxidation steps are required to make these layers.

The bird's beak in the tunnel oxide region during subsequent oxidation steps is a major problem with the scaling down of process technology. The oxide encroachment results in a thicker tunnel oxide, thus lowering program efficiency. We report that the oxidation recipe and doping method of the floating gate affect the bird's beak.[5] Also, the active width on an EEPROM cell is an important parameter. In this paper, we report the effect of oxide recess in shallow trench isolation (STI) on the bird's beak as well as characteristics of an EEPROM cell. Silicon dioxide (SiO_2) in the STI region of an EEPROM cell is partially removed before growth of the tunnel oxide. The EEPROM cell is fabricated with 0.18 μm logic process and its cell size is 0.95 μm^2.

Model

After formation of STI, logic and high-voltage wells are formed and tunnel oxide of 85 Å is grown by wet oxidation at 800°C. Before growth of tunnel oxide, the wet etch of 200 and 400 Å using diluted hydrogen fluoride (DHF) is performed to remove STI oxide after lithography, opening the EEPROM cell region only. Next, in situ-doped n-type polysilicon is deposited and patterned to form a floating gate. After growth of bottom oxide in ONO by dry oxidation, silicon nitride (Si_3N_4) is deposited by low-pressure chemical vapor deposition (LPCVD) and etchbacked to form the nitride spacer. During growth of the top oxide layer in ONO, oxygen penetrates to the floating gate region via the interface of Si_3N_4-SiO_2 and, thus, oxidizes polysilicon mainly at the edge of the floating gate.[6] After formation of ONO, thick oxide is grown for the control gate to sustain high voltage during programming and erasing. Again, polysilicon is deposited and patterned to form the control gate.

Results and Discussion

Table I shows bias conditions for cell operation. For programming, 16 V is applied to the word line while both the bit line and well are grounded with the floating source line. Note that the bit line of the unselected cells is maintained at 12 V to minimize disturbance of the cells, while the word line is biased to 2.5 V. The erase is performed by a byte unit. For this operation, 14 V is applied to the bit line and p-well, and the gate is grounded while the source line is floated. Table I also shows the bias condition of unselected cells during erasing. For reading, 2.5 V is applied to the word line with the 1 V in the bit line.

Figure 1 shows the distributions of programmed threshold voltage (V_T) with and without the oxide recess in STI. V_T measuring is performed in a 64 K bit cell array at room temperature. After initial erase, all cells are repeated for 10 cycles of programming and erasing. After that, the selected cell is programmed by applying 16 V in the control gate while the drain and substrate are grounded as mentioned earlier. Note that the source is floated during programming. For program V_T measurement, the control gate is swept from 0 to 5 V with the drain voltage of 0.1 V, while both the source and well are grounded.

Note that there is a wide distribution of program V_T without the oxide recess and the distribution is improved with increasing recess depth. Because programming V_T is closely related to the thickness of the tunnel oxide, the result of Fig. 1 indicates that the uniformity of tunnel oxide is very wide, possibly due to oxide encroachment during subsequent oxidation process. Although Fig. 1 implies that the encroachment is largely reduced with increasing STI recess, oxide growth still occurred in the floating gate during subsequent oxidation steps.

Figure 2 shows the cell layout and vertical transmission electron microscopy (TEM) picture of cell transistors. The cell transistors consist of a floating gate and two neighboring select gates. It seems that the main route of oxide encroachment is the bottom edge of the floating gate during ONO top oxidation because the sidewall of the floating gate is blocked by Si_3N_4. Various parameters including the active area, oxidation recipe, and cell structure affect later oxide growth.[7] Note that the lateral oxidation could result not only in oxide encroachment in the direction of the channel length, but also bring it about in the direction of the channel width as shown in Fig. 2a. In this study, we consider only the oxide encroachment in the direction of the channel width, which is depicted as Y in Fig. 2a, to investigate the effects of the oxide recess in STI.

TEM analysis is performed to investigate the degree of oxide encroachment. It revealed that severe oxide encroachment occurs when the oxide recess in STI is not performed, as shown in Fig. 3a. Also, the thickness of tunnel oxide is larger at the edge than the

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Table I. Bias condition during programming, erasing, and reading for both selected and unselected cells.

		Program	Erase	Read
Word line	Selected	16 V	0	2.5 V
	Unselected	2.5 V	11 V	0
Bit line	Selected	0	14 V	1.0 V
	Unselected	12 V	11 V	0
P-well	Selected	0	14 V	0
	Unselected	0	0	0
Source	Selected	Floating	Floating	0
	Unselected	Floating	Floating	0

center. It is 140 Å at the edge and 105 Å at the center. Because the original thickness is 85 Å, this result implies that the oxide encroachments starting from each side of the active edges meet each other at the center region,[8] and thus increase tunnel oxide thickness in the center region. When a SiO_2 is recessed in STI, the etch rate on the STI corner is faster and, therefore, a groove is formed as shown in Fig. 3b. This results in an increase of active area because polysilicon remained on the groove.

The remaining polysilcon on the groove retards lateral diffusion of oxidant during subsequent oxidation. In fact, there are two major diffusion paths of oxidant to reach the floating gate. One is the diffusion along the floating gate poly Si-SiO_2 interface and the other is the diffusion through less dense SiO_2 in the STI. When an STI oxide is recessed, the diffusion along the interface is prolonged due to increased diffusion length. Suppression of oxide growth with increasing etching time implies that the interface is a major path of oxidant diffusion. Also, polysilicon on the groove can play a role in retarding oxidant diffusion. It is known that the diffusion rate of oxidant in polysilicon is lower than that of oxide and thus delays the lateral oxidation in the edge of STI. The thicker tunnel oxide on the STI edge when oxide is recessed is due to enhanced oxidation rate on the corner region during tunnel oxide growth. It is shown that the silicon surface on the STI edge has a faster oxidation rate because it has ⟨111⟩ orientation. As shown in Fig. 1, program V_T still has wide distribution from 3 to 4.5 V, although a 400 Å oxide is recessed. The oxidant can diffuse not only from the STI edge, but also from the gate edge. Because the gate edge is not related to oxide recess, oxide is mainly grown on this region.

Figure 4a shows the distribution of erase cell current as a function of erase cell V_T with and without the oxide recess in STI. As shown, the erase cell current is increased with increasing of the oxide recess in STI due to increase of the active width by the oxide recess in STI. It is observed that erase cell current is increased about

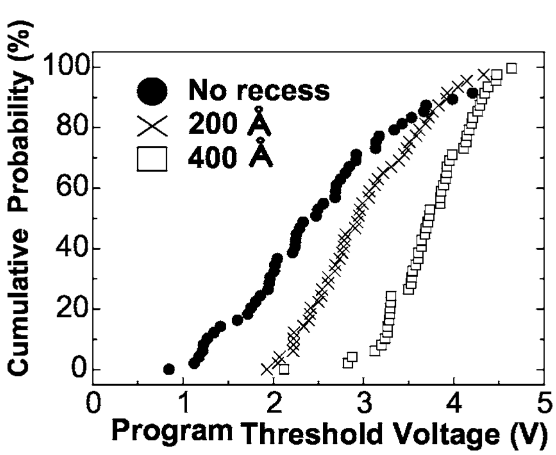

Figure 1. Distribution of program cell V_T with and without the oxide recess in STI in EEPROM cell with in situ-doped floating gate.

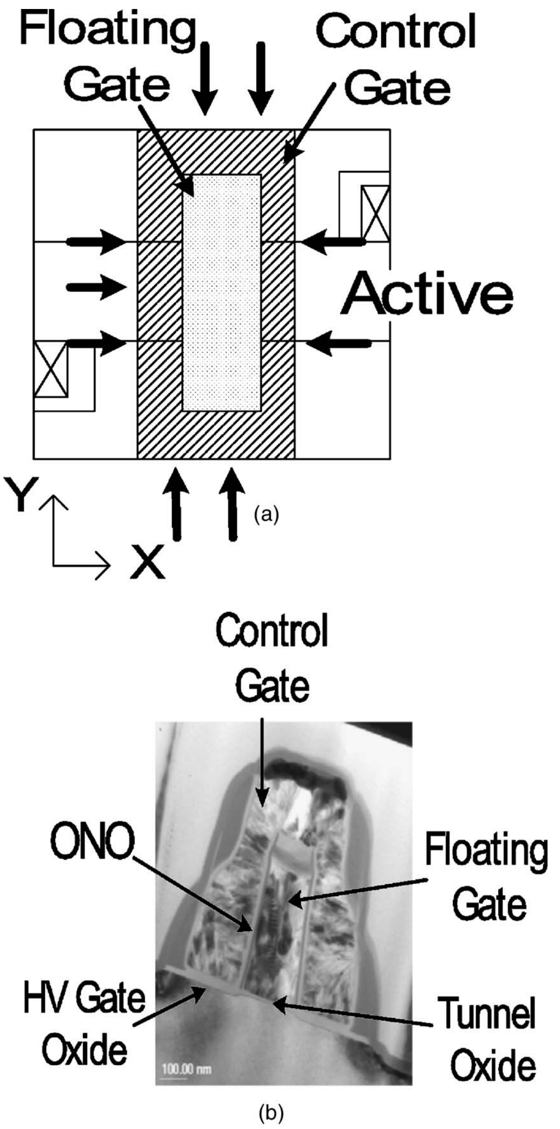

Figure 2. Cell layout and vertical TEM picture of cell transistors. (a) Layout of unit cell; (b) TEM view of EEPROM cell in direction of channel length. Arrows in (a) indicate the diffusion path of oxidant in oxidation process.

11% with oxide recess of 200 Å and 21% with oxide recess of 400 Å, respectively. Figure 4b reveals a relationship between erase cell current and leakage current. Note that leakage current is also increased with increasing STI recess due to increased junction area.

Figure 5 shows the endurance characteristics of EEPROM cell with and without the oxide recess in STI. They are cycled with alternating erase-program pulses of 14 and 16 V, respectively. As shown earlier, there is a wide distribution of program V_T. For comparison, cells having identical initial program V_T are selected. As shown, there is no difference of variation in program V_T up to 1×10^3 cycling. However, a larger decrease of program V_T is observed from 1×10^3 to 1×10^5 cycling when the STI recess is 400 Å. Note that the behavior of the cell with 200 Å recess is similar to the cell without recess. Because the large drop in program V_T is due to more electron loss in the floating gate, this result implies that retention time is reduced when the oxide recess is 400 Å. The main charge loss occurred on the STI edge. As shown in Fig. 3, thickness of the tunnel oxide near the STI edge is thicker than other regions. Therefore, faster loss of electrons in the STI edge indicates that electron diffusivity on this region is increased, possibly due to higher film stress of the tunnel oxide.

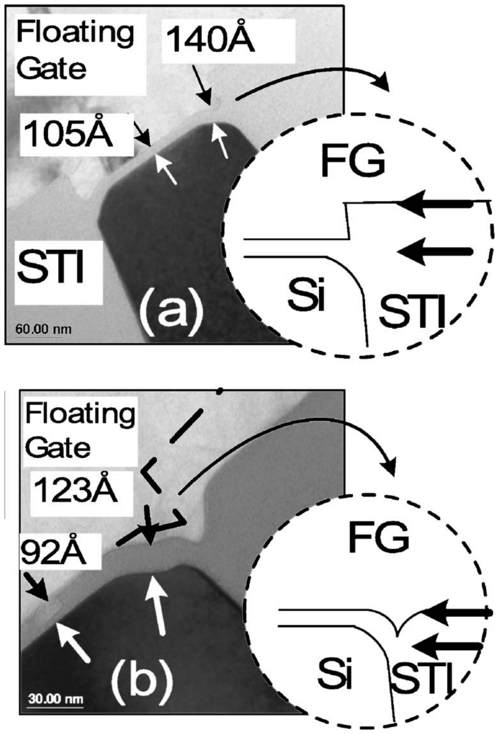

Figure 3. TEM view of the STI edge region and schematic diagram of floating gate. (a) TEM view of STI edge with the oxide recess in STI; dotted line shows the boundary of floating gate before the oxide recess in STI. (b) TEM view of STI edge without the oxide recess in STI; dotted circle is a schematic diagram in the edge of STI, in which arrows indicate the diffusion path of oxidant in oxidation process

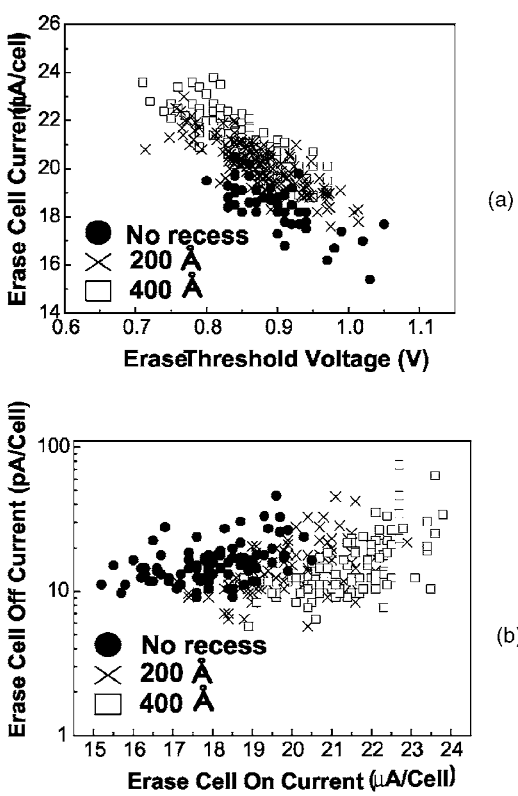

Figure 4. The erase cell current as a function of erase cell V_T. The read condition of erase cell current is that the control gate is biased to 2.5 V, and both the source and the well are grounded with drain voltage of 1 V.

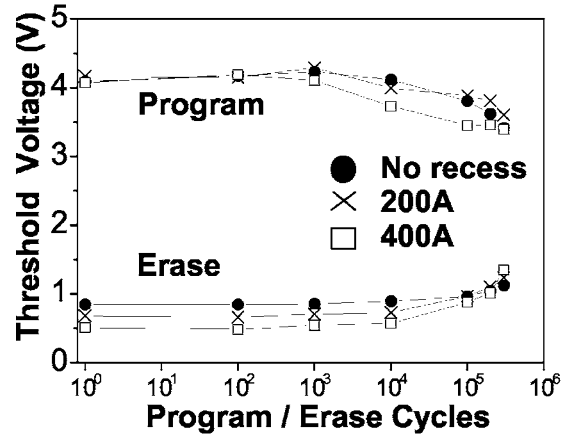

Figure 5. Endurance characteristics as a function of STI recess. All samples are cycled with alternating erase-program pulses of 14 and 16 V, respectively.

Figure 5 also shows the variation of erase cell V_T as a function of cycling time. As shown, a cell with no recess shows a slight increase in erase V_T after cycling time of 1×10^5, while a sharp increase is observed after 1×10^4 cycling for the cells with STI recess. Especially, the increment is larger with oxide recess of 400 Å. The result implies that more positive charges are generated on the channel region when the oxide recess depth is increased. This could also be due to increased film stress of tunnel oxide when the oxide recess is performed. Note that film stress is largely dependent on rounding at the STI edge.[9]

Conclusion

In this article, we investigated the effects of the oxide recess in STI on EEPROM cell with in situ-doped floating gate. It is shown that the distribution of program cell V_T is improved with increasing the oxide recess in STI. Also, it is observed that erase cell current is increased about 11 and 21% when the oxide recesses are 200 and 400 Å, respectively. It appears that the oxide recess suppresses the oxide encroachment of the floating gate during subsequent oxidation steps. The result of endurance measurements in EEPROM cell reveals that both electron loss and charge generation increase with increasing recess depth when the cycling time exceeds about 1×10^3.

Magnachip Semiconductor, Incorporated, assisted in meeting the publication on costs of this article.

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