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Passivation of Deep Levels at the SiO_2/SiC Interface

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The analysis of trapping phenomena in 4H- and 6H-SiC MOS capacitors from C-V and CCDLTS measurements is presented. Three categories of defect levels are distinguished: namely, oxide traps, semiconductor bulk traps, and interface states. NO annealing results in a dramatic decrease of the density of the interface states and the oxide traps in both polytypes, but does not reduce that of the SiC bulk traps.

Introduction

Silicon carbide (SiC) metal-oxide-semiconductor (MOS) transistors have the potential for high-power, high-frequency and high-temperature applications owing to attractive SiC material properties, such as the large band-gap above 3eV, bulk electron mobility comparable to that of Si, and excellent thermal conductivity. Moreover, MOS fabrication on SiC can follow Si technology, owing to the availability of silicon dioxide (SiO_2) as the natural oxide on both materials. However, the electrical properties of the SiC MOS system, for example the poor channel mobility compared to bulk values, are still the subject of intense research efforts. In particular, the release of C atoms during oxidation increases the density and the variety of interface states and the larger band-gap energy compared to Si makes the SiC MOS interface sensitive to a larger range of defect energy levels. The latter effect is apparent from the strong decrease in the electron channel conductivity at increasing band-gap energy, from 3eV for the 6H-SiC polytype to about 3.25eV for 4H-SiC. Post-oxidation treatments, such as NO annealing at 1175^{o}C for 2 hours, increase the electron channel mobility in 4H-SiC to values comparable to that in as-oxidized 6H-SiC MOS [1,2]. However, the residual presence of excess C atoms in SiC near the interface was found to be inversely related to the channel mobility [3].

With the aim of relating these electrical characteristics to the interface properties, the electron trapping phenomena in n-type MOS capacitors on the (0001) Si-face of 4H and 6H-SiC polytypes were characterized by constant-capacitance deep level transient spectroscopy (CCDLTS). Compared to other interface characterization techniques, such as high-low capacitance-voltage and conductance-dispersion analysis [4], CCDLTS provides more detailed information on the physical properties of interface states, as it allows for the simultaneous extraction of energy depth and capture cross-section of the interface states. In these SiO_2/SiC capacitors three different types of traps, including

interface states, bulk semiconductor traps and oxide traps, are characterized in terms of their response to the NO annealing passivation treatment.

Experimental

n-type 4H-SiC and 6H-SiC epilayers, 10-μm thick and doped with N at about $5\times10^{15}cm^{-3}$, were oxidized in flowing O_2 at 1150°C for 8 hours and subsequently underwent an Ar anneal at the same temperature for 30 min, yielding an oxide thickness of about 60nm on the (0001) Si-face. NO annealing was then performed at 1175°C, for different time lengths of 12min, 30min and120 min on the 4H-SiC samples. As previously shown, N is detected by secondary ion mass spectrometry (SIMS) only at the oxide/semiconductor interface with total densities of incorporated N atoms of 2.1, 3.5 and $6\times10^{14}cm^{-2}$, respectively [5]. A 4H-SiC sample without annealing has also been processed and characterized for reference. The 6H-SiC MOS capacitors were processed only in the conditions of no annealing and 120min, with a total N surface density in the latter, assumed to be similar to that measured in the corresponding 4H-SiC MOS device. 200nm-thick Al contacts, 500μm in diameter, were evaporated onto the oxide, whereas sputtered Au was used to ensure good ohmic contact to the substrate.

High-frequency C-V curves were recorded at temperatures (T) between 300 K and 80 K, from depletion to accumulation using the 1 MHz capacitance meter of the SULA DLTS spectrometer. The oxide capacitance (C_{OX}) value is obtained for voltage biases deep in accumulation, i.e. for large positive bias, and is about 130 pF for all the samples under study. The flat-band voltage (V_{FB}), i.e. the bias voltage for which the Fermi level at the oxide-semiconductor interface (F_P) is equal to the bulk Fermi energy (E_F), was extracted from each C-V curve, following the procedure explained in Ref. 6. The shift of V_{FB} with T, offset by the theoretical temperature dependence of E_F, provides an estimate of the density of interface states distributed within 0.2eV below the conduction band energy minimum (E_C). However, due to the lack of resolution in energy of this technique, only a total estimate of the interface states surface density (N_{IT}) will be obtained by using the expression:

$$N_{IT} = \frac{C_{OX}\cdot\left(V_{FB}^{80K} - V_{FB}^{300K} - \left(E_F^{80K} - E_F^{300K}\right)\right)}{qA} \quad , \qquad (1)$$

with A the area of the capacitor oxide contacts, and E_F decreasing from about -0.06eV to about -0.2eV with respect to E_C as T increases from 80K up to 300K.

DLTS spectra were obtained from the voltage transients that are generated to maintain a preset capacitance value by a feedback loop and are sampled at times t_1 and t_2. The detected voltage transients are a direct measurement of the charge trapped at interface states energetically located near E_C, within an interval determined by the filling pulse voltage (V_P) and the feedback capacitance (C_F) values. The latter was set to about 35pF, corresponding to a ratio C_F/C_{OX} of about 0.25, for all the samples investigated. The sampling times corresponded to an emission rate (e_0) of $465.1s^{-1}$ [7]. The filling pulse width was always set to 25 ms.

The estimate of the density of interface states as a function of energy (D_{IT}) can be obtained from the dependence of the CCDLTS signal intensity on F_P, as determined from V_P. In the simple case of an interface trap located at E_T, the amplitude of the DLTS signal will be proportional to the occupation probability f_T of the level, which is given by:

$$f_T = \frac{1}{1 + e^{\frac{E_T - F_P}{kT}}}, \tag{2}$$

having a maximum of the first derivative with respect to F_P, when

$$F_P = E_T. \tag{3}$$

The trap emission rate, e_n, is defined by

$$e_n = \sigma \cdot v_{th} \cdot N_C \cdot e^{\frac{E_T}{kT}}, \tag{4}$$

with E_T the trap energy with respect to E_C and with N_C equal to $3.25\times10^{15}\times T^{3/2}cm^{-3}$ and $1.73\times10^{15}\times T^{3/2}cm^{-3}$, for 4H-SiC and 6H-SiC polytypes, respectively. A peak in the CCDLTS spectrum occurs when

$$e_n = e_0, \tag{5}$$

which is the basic equation for standard DLTS analysis [6]. By combining equations (3)-(5), the capture cross section is related to the value of F_P corresponding to the maximum change in the DLTS signal amplitude

$$\sigma = e_0 \Big/ \left(v_{th} \cdot N_C \cdot e^{\frac{F_P}{kT}} \right) \tag{6}$$

F_P values are extracted from a point-by-point inversion of the C-V characteristics, based on a model of the MOS capacitance as the series connection of C_{OX} and the semiconductor layer capacitance (C_D), and on the analytical calculation of the latter from the Poisson equation applied to uniformly doped layers [8].

Equations (3) and (6), can be also applied to the case of broad distributions of interface states, provided that the CCDLTS signal is monitored across F_P steps of the order of a few kT [9]. In this case, an average D_{IT} as function of energy (E_T) can be determined from the expression

$$D_{IT} = \frac{C_{OX} \cdot \Delta V}{qAkT\ln(t_2/t_1)}, \tag{7}$$

where ΔV is the CCDLTS signal amplitude and t_2/t_1 is equal to 2.5.

Finally, it is important to point out that the above analysis for CCDLTS spectra relies on the condition expressed in (2), which applies only to interface states, whereas CCDLTS spectra may contain emission signals from other types of defect levels, specifically traps in the SiC (bulk traps) or in the oxide near the interface (oxide traps). Nonetheless, it will be shown in the following that inconsistencies arising from the loss of validity for condition (2) can be easily identified and interpreted, thus providing general information on the spatial distribution of defects across the MOS structures.

Results

Fig. 1(a) and (b) show the CCDLTS spectra for the series of 4H-SiC and 6H-SiC capacitors obtained in saturated conditions (or nearly saturated for sample 4H-0), i.e. at V_P yielding the maximum DLTS signal. Samples are labeled according to the NO annealing time in min. As was previously reported [10], it can be seen in Fig. 1(a) that the CCDLTS signal for the 4H-0 capacitor is about one order of magnitude larger than for the 4H-120 device. The latter, in turn, has a maximum intensity very close to that of the spectra for the 6H-0 and 6H-120 MOS interfaces shown in Fig. 1(b). This trend is consistent with previous measurements of interface state density and channel electron mobility in MOS transistors [1,2]. The comparison between the effects of NO passivation on the spectra from the two polytypes also reveals that the 4H-SiC interface states are reduced quite uniformly over the entire temperature range, whereas the 6H-120 capacitor differs from the 6H-0 one, primarily in the high-temperature portion of the spectra, namely at T>150K. The latter suggests that a localized deep energy defect distribution is preferentially passivated by NO annealing in 6H-SiC.

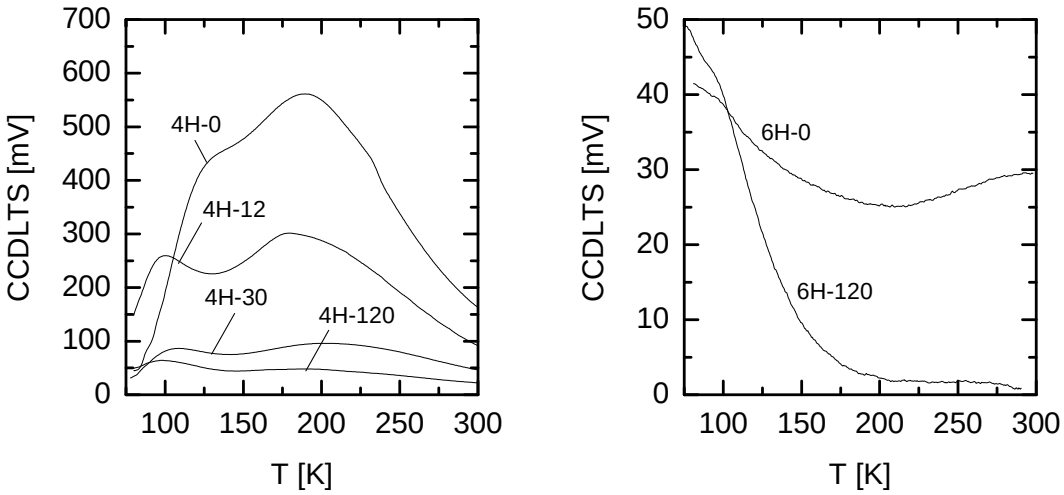

Figure 1. CCDLTS characteristics obtained at saturating V_P conditions for the (a) 4H-SiC and (b) 6H-SiC series capacitors. Samples are labeled according to the NO annealing time.

The identification of the energetic and spatial location of the defects contributing to the saturated DLTS spectra in Fig. 1 was obtained by carrying out an F_P-resolved analysis of the emission signal, as discussed in the previous section. For the sake of brevity, only data for samples 4H-30 and 6H-0 MOS will be shown as examples of this analysis.

4H-30 MOS

Fig 2(a) shows the C-V characteristics, at temperatures of 80K and 300K, along with those at two intermediate temperatures 100K and 200K. V_{FB} increases from 0.1V around 300K up to 1.2V at 80K. From expression (1), a rough estimate of the total amount of trapped charge within about 0.2eV below E_C is $N_{IT} = 4\times10^{11}cm^{-2}$.

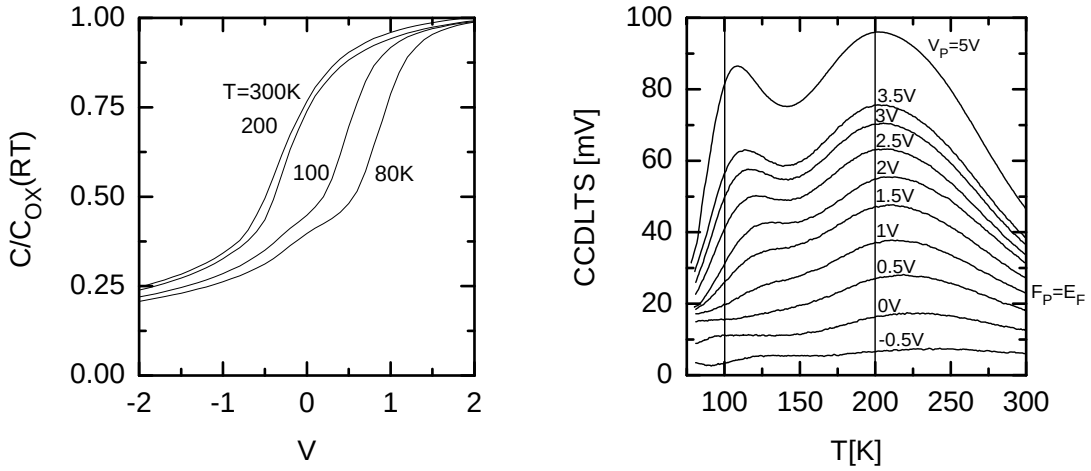

Figure 2. Experimental data for the 4H-30 capacitor. (a) High-frequency C-V characteristics at the extremes of the measurements temperature range, and at the DLTS peak temperature values. (b) CCDLTS spectra at different filling-pulse conditions. The label $F_P = E_F$ indicates the flat-band bias conditions at 300K.

Two peaks in Fig. 2(b), located at 100K and 200K, are clearly visible. The behavior of the DLTS signal with F_P at temperature 200K can be thoroughly appreciated. This peak is already apparent when the sample is biased in depletion, i.e at $V_P < 0V$ ($F_P < E_F$), and it strongly increases in amplitude as V_P is increased to accumulation ($F_P > E_F$). This indicates that the corresponding D_{IT} extends over a wide range of energies and it is peaked within 0.13eV below E_C. However, from expression (6), it was found that σ varies over several orders of magnitude from $10^{-16}cm^2$, corresponding with the signal below F_P, up to $10^{-22}cm^2$, for the portion of the spectra above E_F. While the former value may be associated with interface traps, the latter is clearly too small to represent a physical capture cross-section. This anomalous value can be understood if the condition specified by equation (2) is not valid for these traps, i.e. if they are located in the oxide, but close to the interface where trapped electrons are emitted to the 4H-SiC conduction band.

At low T, namely around 100K, a peak is generated only for $F_P > E_F$, whereas rather featureless spectra are obtained for $F_P < E_F$. The largest increase of the latter signal with increasing F_P occurs at around $V_P = 0V$ ($F_P = -0.3eV$) and it saturates around $V_P = 1V$ ($F_P = E_F = -0.1eV$), i.e. when the sample is biased in depletion. The application of expression (6) to estimate the capture cross-section yields values of σ which are orders-of-magnitude larger than the upper physical limit of $10^{-13}cm^2$. This again indicates that equation (2) cannot be applied to these traps. That trapping is detected at very low T, suggests that these traps must be energetically as shallow as E_F, The range of F_P values indicates that the traps are located in the SiC (semiconductor bulk traps) and are distributed near the MOS interface over a depth of ~100 nm, the latter corresponding to the depletion width for F_P at -0.3eV.

Estimates of the average D_{IT} for all the trap categories were obtained at the two peak temperatures. At 200K, interface states account for a D_{IT} of about $5\times10^{11}cm^{-2}eV^{-1}$, from the signal below flat-band, whereas oxide traps feature a density of $2.4\times10^{12}cm^{-2}eV^{-1}$, from the rest of the intensity above E_F. Similarly, at 100 K, a D_{IT} of $\sim4\times10^{12}cm^{-2}eV^{-1}$ is

obtained for oxide traps, from the portion of the spectrum above flat-band. Finally, an equivalent D_{IT} of $1\times10^{12}cm^{-2}eV^{-1}$ was obtained for the semiconductor bulk traps described above, showing that their impact on the trapping phenomena as detected by CCDLTS is nearly comparable to the dominant effect by the oxide traps.

6H-0 MOS

The comparison of the trapping phenomena in the 6H-SiC capacitor without post-oxidation annealing and the 4H-30 sample, can provide additional insight about the effectiveness of NO annealing with respect to the nature and energy location of interface traps. In fact, the similarity in transport properties repeatedly reported for transistors fabricated from as-oxidized 6H-SiC and NO-annealed 4H-SiC indicates that the energy position of the large majority of the interface defects that are passivated by NO treatment are resonant with the 6H-SiC conduction band and must therefore be less than ~0.2 eV below the 4H-SiC conduction band [11]. In agreement with this, the temperature dispersion of the C-V characteristics for the 6H-0 capacitor in Fig. 3(a) shows a V_{FB} variation from -0.8V at 300K up to 0V at 80K, and yields $N_{IT} = 2.7\times10^{11}cm^{-2}$, comparable to that estimated for the 4H-30 capacitor.

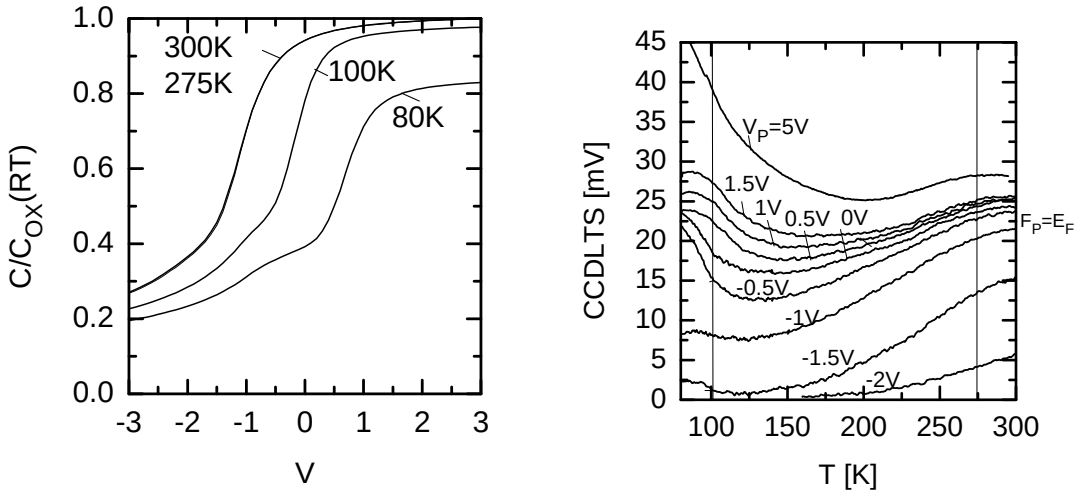

Figure 3. Experimental data for the 6H-0 capacitor. (a) High-frequency C-V characteristics at the extremes of the measurement temperature range, and at the DLTS peak temperature value. (b) CCDLTS spectra at different filling-pulse conditions. The label $F_P = E_F$ indicates the flat-band bias conditions at 300K.

CCDLTS spectra in Fig. 3(b) show that, despite the general similarities in the electrical properties, the spectroscopic composition of the total N_{IT} differs noticeably from that presented here for the 4H-30. In particular, the high-temperature portion of the spectra in Fig. 3(b), along the vertical line at T = 275K, displays a dependence on F_P that closely follows Eq. (2). The DLTS signal shows a large increase for V_P = -1V (F_P = -0.5eV) and saturates around V_P = -0.5V ($F_P = E_F$ = -0.2eV). Moreover, the estimate of the capture cross-section by expression (6) from these parameters, namely trap energy depth of 0.5eV and peak temperature of 275K, yields σ values of $\sim10^{-15}$ cm^2. Similar values have been already obtained for interface states distributed in the upper half of 6H-SiC

band-gap by long-time-constant CCDLTS, that have been associated with graphite-like carbon-clusters [12].

The low temperature portion of the spectra in Fig. 3(b) shows large similarities with the corresponding part in Fig. 2(b) for 4H-30. In particular, two different dependences of the CCDLTS amplitude on F_P can be identified. Namely, the largest increase occurs at around V_P = 0V (F_P = -0.3eV) and saturates around V_P = 1V ($F_P = E_F$ = -0.1eV), thus appearing as the signature of shallow bulk traps spatially extending over 100nm from the interface, as described for the 4H-30 sample. For $F_P > E_F$, the F_P dependence typical of oxide traps is observed. Contrary to the 4H-SiC capacitors, the oxide trap peak position could not be determined within the temperature range and emission rates available with the spectrometer, i.e. at T higher than 80K and e_0 lower than 465.1s^{-1}. That we detect only the low energy tail of this trap distribution is consistent with the assumption that the majority of these trapping centers lie above E_C in 6H-SiC.

Estimates for the average D_{IT} related to both the oxide traps and the SiC traps yield values of ~1.2×$10^{12}$$cm^{-2}$$eV^{-1}$, thus showing that, as for 4H-30 MOS, trapping phenomena by semiconductor bulk traps may be as important as those by oxide defects. In addition, the deep interface states, arising from carbon clusters, would account for a D_{IT} of 4×10^{11} cm^{-2} eV^{-1}.

Summary and Conclusions

Table I reports for each sample the evolution of the integrated N density at the SiO_2/SiC interface [5], which is assumed to be similar for both 4H- and 6H-SiC, along with the N_{IT} extracted from the C-V measurements and D_{IT}, corresponding to the CCDLTS signals for the three categories of traps discussed in the previous section: namely, oxide traps yielding CCDLTS peaks for $F_P > E_F$ at 100K, interface states corresponding to surface band-bending at $F_P < E_F$ above 200K and semiconductor bulk traps corresponding to the DLTS signal at low T for $F_P < E_F$.

TABLE I. Evolution of the N-atoms incorporation, of N_{IT} of the D_{IT} for three different trap groups with NO annealing

Sample	N-SIMS 10^{14} cm^{-2}	N_{IT} 10^{11} cm^{-2}	Interface states 10^{12} $cm^{-2}eV^{-1}$	Oxide Traps 10^{12} $cm^{-2}eV^{-1}$	SiC Bulk Traps 10^{12} $cm^{-2}eV^{-1}$
4H-0	0	16	3	20	-
4H-12	2.1	13	2	14	-
4H-30	3.5	4	0.5	1.4	1.0
4H-120	6	3.9	0.5	1.5	1.5
6H-0	0	2.7	0.4	1.2	1.2
6H-120	6	6.4	<0.1	0.3	2.4

The identification of the three different categories by analysis of the F_P-resolved DLTS, was based on the fact that only traps observed for $F_P < E_F$ at T above 200K, feature a capture cross section typical of interface states. In contrast, the other two categories appear to have anomalous capture cross section values that can be accounted for only if Eq. (2) is not valid. Therefore, those signals were interpreted as corresponding to spatial distributions of defects in the oxide or in the SiC near the interface. As for the signal detected below 100K for F_P around -0.3eV, it can be understood as likely originating from energetically shallow trap levels distributed across 100nm in the depletion region of the SiC epilayer.

N incorporation at the SiO_2/SiC interface results in a decrease of the D_{IT} of the interface states and the oxide traps by about one order of magnitude in 4H-SiC, but only by a factor of about four in 6H-SiC. In contrast, the reduction of total N_{IT}, obtained from

C-V measurements, is less than a factor of four in 4H-SiC and is negligible in 6H-SiC capacitors, suggesting that all the electron traps are not detected by this method. The magnitude of the residual D_{IT} in 4H-SiC after two hours of annealing time, when N incorporation is essentially saturated [5], closely resembles that in as-oxidized 6H-SiC devices, consistent with the general similarity between the electrical characteristics of these two types of MOS transistors. This confirms that the effect of the wider 4H-SiC bandgap can be overcome by NO annealing. However, this residual D_{IT}, is still of concern for channel transport properties of SiC MOS transistors. We note that the incorporation of N atoms does not seem to affect the concentration of the low-temperature traps that are dominant in the 6H-SiC samples and which are also observed in nitrided 4H-SiC samples. These traps are likely energetically shallow defects spread over tens of nm in the SiC adjacent to the interface and thus may be related to the presence of excess C in SiC.

Acknowledgments

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