A CMOS Single Stage Fully Differential OP-Amp with 120 dB DC Gain

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***Abstract*— A single stage fully differential 120-dB op amp for standard 0.25μm process is designed based on folded cascode and "gain boosting" technique. This design demonstrates a DC gain of 120 dB with a unity gain frequency of 381MHz and a phase margin of 64°. The circuit's performance has been simulated with +/-10% voltage supply variation and 27°C-85°C temperature range.**

***Index Terms*—folded cascode, single stage, gain boost.**

I. Introduction

In many analog circuit applications such as A/D converters [1], switched capacitor filters [2] and sample-and-hold amplifiers, speed and accuracy are determined by the settling behavior of the op amp circuit. The settling speed mainly depends on the unity gain frequency and a single pole settling time while high settling accuracy is due to high DC gain of the op-amp circuit [3].

In order to achieve both high settling speed and high DC gain, several circuit approaches such as dynamic biasing of trnsconductance amplifier [4], triple-cascode amplifier [5], positive-feedback transconductance amplifier [6] were proposed, but the gain and unity gain frequency of those gain boosting techniques are not enough for the recent submicron CMOS circuit applications. In 1990, K. Bult and G. Geelen proposed the folded cascode op-amps with the gain boosting technique [7], which shows a DC gain of 90 dB and a unity-gain frequency of 116MHz with 16pF load. The gain boosting technique is introduced by Hosticka in 1979[8] and Bult and G. Geelen firstly applied this technique to op-amp.

Based on the folded cascode op-amp design with the gain boosting technique, this paper presents the state-of-the-art 120dB DC gain fully differential op-amp with 381MHz unity gain frequency using IBM 0.25μm CMOS technology.

The gain boosting technique is explained in section II and the circuit's frequency behavior is analyzed in section III. In section IV, the circuit implantation with 0.25 CMOS process is presented. The simulation results are given and discussed in section V.

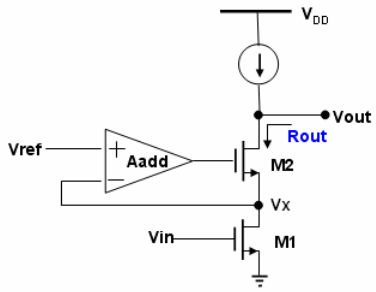


Fig. 1. Cascoded gain stage with gain enhancement

II. Gain Boosting

As shown in Figure 1, the idea of gain boosting is based on negative feedback loop to set the drain voltage of M2 [9]. Negative feedback drives the gate of M2 until V_x has the same value as V_{ref}. Therefore, the variation of V_{out} has much less effect on V_X, because A_{add} "regulates" this voltage. This topology is usually called "regulated cascode" or "active cascode". With the smaller variation of V_X due to the change of V_{out}, the output current becomes less sensitive to the voltage variation at V_{out} compared with conventional cascode structure. Therefore the output impedance increases as shown in equation (1):

$$R_{out} = r_{o1} + r_{o2} + \left[g_{m2}(A_{add} + 1) + g_{mb2}\right] \times r_{o1} r_{o2} \approx A_{add}\, g_{m2} r_{o1} r_{o2} \quad (1)$$

This increased output resistance results in several orders of improvements on the overall gain as shown in equation (2):

$$A_{vtot} = g_{m1} R_{out} = A_{add}\, g_{m1} g_{m2} r_{o1} r_{o2} \quad (2)$$

III. Frequency Analysis

A. Differential Folded Cascade Op Amp

For a fully differential folded cascode op amp like the one shown in Figure2, the dominant pole is the pole at output node (node B) which has the highest impedance and in most cases, the highest capacitance. The pole frequency is given by $w_{p1} = -\frac{1}{R_{out} C_L}$, where R_{out} is the op amp output impedance and C_L is the load capacitance [10].

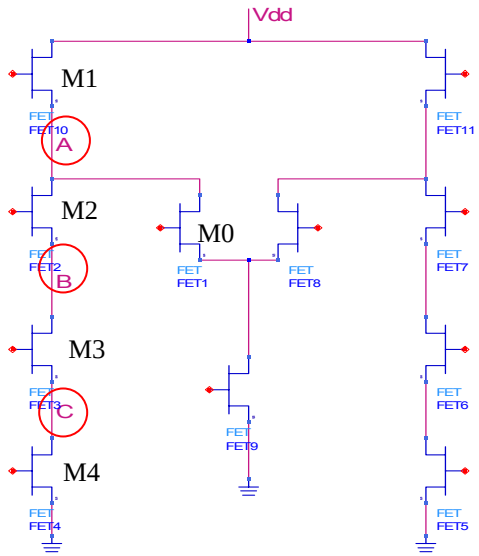


Figure 2. Fully differential folded cascade op amp

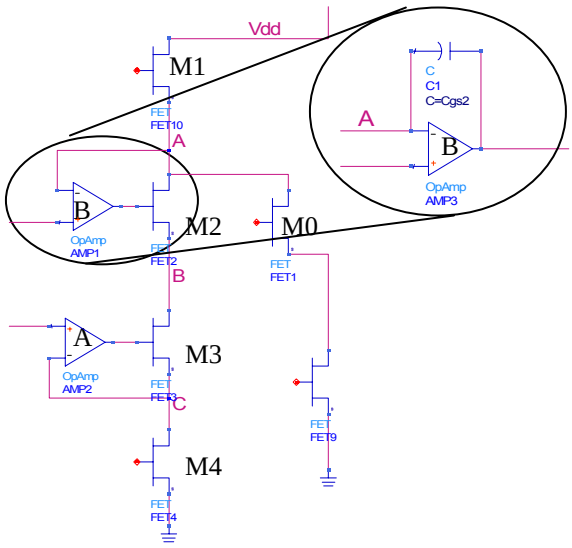


Figure 3. Half circuit of the regulated folded cascade op amp

The second pole is at the cascade transistor source node (node A). The pole frequency is given as:

$w_{p2} = -\frac{g_{m2}}{C_{LA}}$ where g_{m2} is the transconductance of the cascade transistor M2, and C_{LA} is mainly from the gate-source capacitance C_{gs} of M2 [10].

The third pole frequency is $w_{p3} = \frac{g_{m3}}{C_{LC}}$ and there is a zero at $-\frac{g_{m3}}{C_{LC}}$. The effect of this two will thus canceled out [10]. For the interest of our designed op amp, we only consider up to the second pole frequency.

The unity gain frequency is given by $w_u = \frac{g_{m0}}{C_L}$, the size of the input transistor M0 is thus designed accordingly to satisfy the 300 MHz unity-gain frequency specification with 2 pF load.

B. Regulated Folded Cascade Op Amp

As discussed in session II, additional amplifier stages are used to boost gain [7]. Figure 3 shows the half circuit of the proposed op amp.

With the addition of the gain boost amp, the second pole frequency is changed. The source-gate capacitance of M2 now forms a Miller cap which is connected between the input and output of the additional amp B. Therefore the capacitance seen at node A is not just C_{gs2} now, but $(1+A_B)C_{gs2}$ where A_B is the gain of the additional amp B. This reduces the second pole frequency w_{p2} and thus degrades the phase margin of the op amp. In order to overcome this effect, an extra cap is added at the output of amp B. The extra cap reduces the dominant pole frequency of amp B so that its gain drops to a much lower value around w_{p2}. This reduces the Miller effect and pushes up the second pole frequency.

A schematic of this technique is shown in Figure 4 and the simulated bode and phase plots with and without the extra cap are shown in Figure 5. It is shown that without the extra cap, the second pole effect is kicking in around 300MHz which is the unity-gain frequency of the designed op amp. By adding the extra cap (1pF in this case), the second pole is pushed up. This effect is shown more clearly form the phase plot.

For stability concern, the unity gain frequency of the additional stage (g_m /C_{ladd}) has to be larger than the first pole of the main stage ($1/R_{out}C_{Lmain}$) [7]. This can be easily achieved since R_{out} is typically much larger than $1/g_m$.

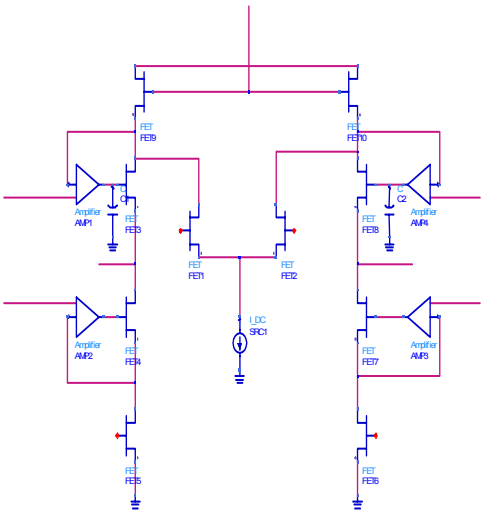


Figure 4: Regulated folded cascade op amp with extra capacitor

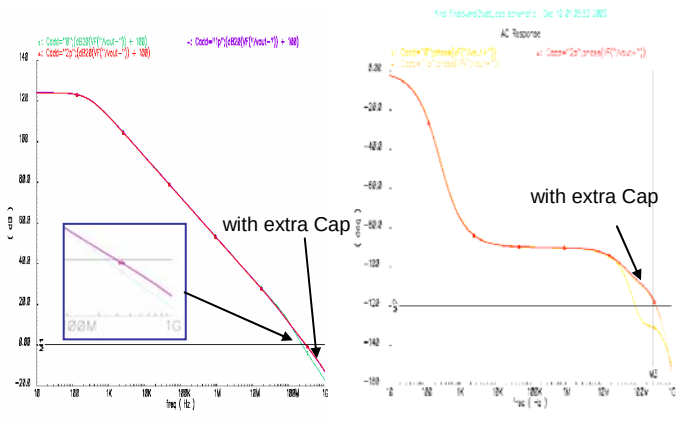


Figure 5. Bold and phase plots of the amp with and without the extra cap

IV. Circuit Implentation

A. Additional gain stage

The additional gain stages are again implemented with folded cascade op amps with single end output. Additional gain stage is applied to both the cascode transistor and current source of the main stage. NMOS differential pair is used for amp B (for cascode transistor) and PMOS differential pair is used for amp A (for current source). They are chosen based on the common-mode DC requirement. Low voltage cascode active current mirror is used in the additional amp. This results in a larger output DC range and only requires one bias voltage [9]. For example, Figure 6 shows the schematic of the additional stage A. Its maximum output voltage is set by V_{dd} -2V_{DSAT} which is around 2V.

B. Common Mode Feedback

The common mode feedback is achieved by controlling the biasing current for the folded cascode in the main stage. As shown in Figure 7, Current I1 and I2 add up and go through the current source M5. If $V_{cm,\ out}$ gets higher, current I1 increases and thus current I2 reduces. This lowers the voltage of node P and as the result, the I_{ds} of transistor M6, which is the biasing current for the cascode amp (main stage), increases. This increasing biasing current will lower down the $V_{cm,\ out.}$

The minimum common mode input is determined by V_{dd}-V_{GS}- V_{DSAT} which is about 0.9V. So the common mode input range is 0.9V-2.5V. This circuit implementation also allows for the output swing of 0.5-2V. This is basically determined by the two V_{DSAT} consumed by M1, M2 and M3, M4 (Figure 2). The dominant pole freq is about 200 Hz and the unity gain frequency of 300 MHz with 2pF differential load.

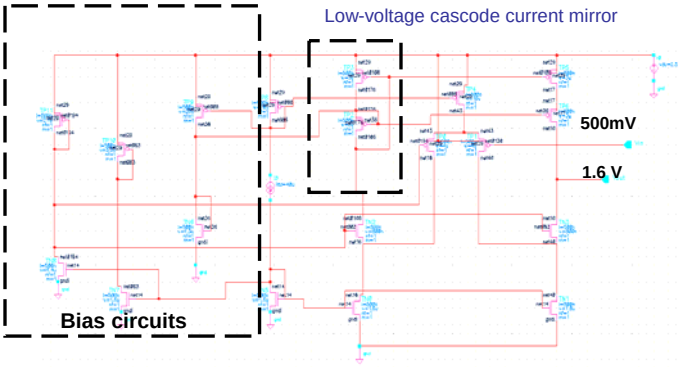


Figure 6. Schematic of the addition gain stage B

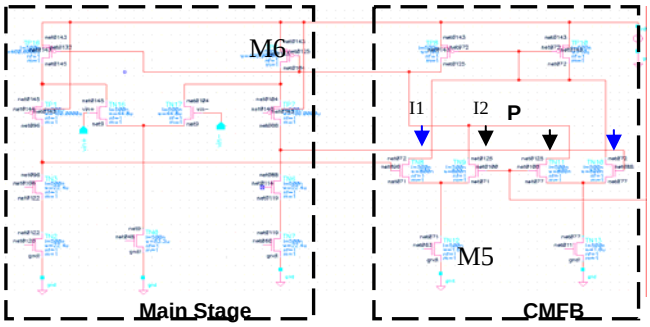


Figure7. Schematic of the main stage with common mode feedback

V. Simulation Results

Based on the design procedure described in the previous sections, a single stage 120-dB fully differential op amp was designed based on IBM 0.25μm CMOS process and simulated using Cadence Design Systems. As shown in Figure 8, the entire circuit's chip size is 0.1×0.3 mm^2, which includes the 5 μm wide power supply slab and ground slab. In this layout, besides the power supply and ground, only one reference current source are needed to provide proper biasing for the circuit. The two 1-pf capacitors were realized using metal-insulator-metal configuration between layers of Metal 2 and Metal 3. For the rest part of the circuit, only Metal 1 and Metal 2 were used in the layout process.

This layout has passed DRC and LVS comparison. In the simulations, the extracted circuit model based on the layout has incorporates the layout parasitic capacitances, which were omitted in the initial schematic simulations. In our layout, since the device's parasitic capacitances demonstrate effects similar with the extra capacitors loaded to the additional stages, the simulated results based on the extracted circuit model from the layout has a slight higher unity gain frequency compared with that from the schematic circuit model. Therefore, only the simulation results based on the extracted model with parasitic capacitances are shown in the following discussions. The capacitor load used in this design at the differential output is 2pF.

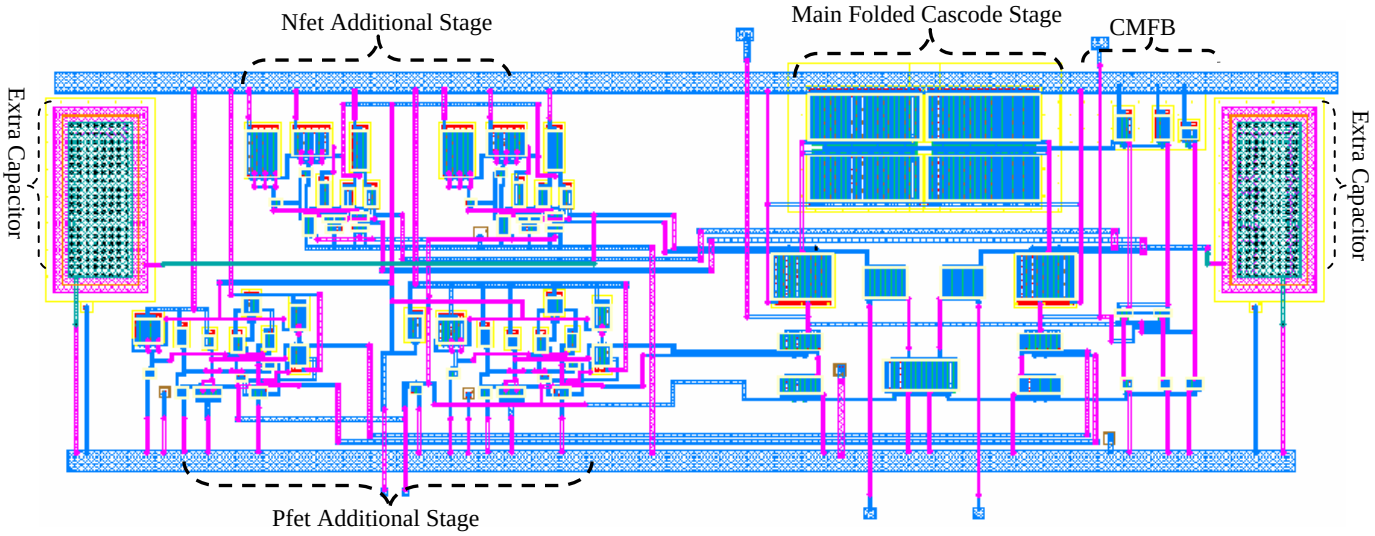


Figure. 8: Layout view of the completed op amp.

As shown in Figure. 9, when the power supply changes from 2.25 V to 2.75V (2.5V+/-10%), the simulated DC output responses demonstrate similar high gain responses with zero input voltage offsets. The output voltage swing is minimum (±0.55 V) under 2.25V power supply, which still satisfies the design specification of ±0.4 V. Also, under the same power supply variations, the AC responses of this design satisfy the gain (A_0≥ 90 dB), unity gain frequency (f_0≥ 300 MHz) and phase margin (PM ≥ 60^o) requirements (Figure. 10). Because the common mode feed back network stabilizes the output common mode voltage, the acceptable input common mode voltage can be as high as 2.5 V and can be as low as 0.9 V with DC and AC performance satisfying the desired design specifications (Figure 11).

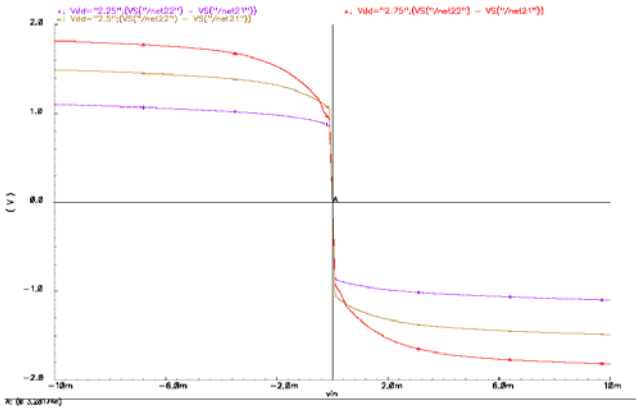
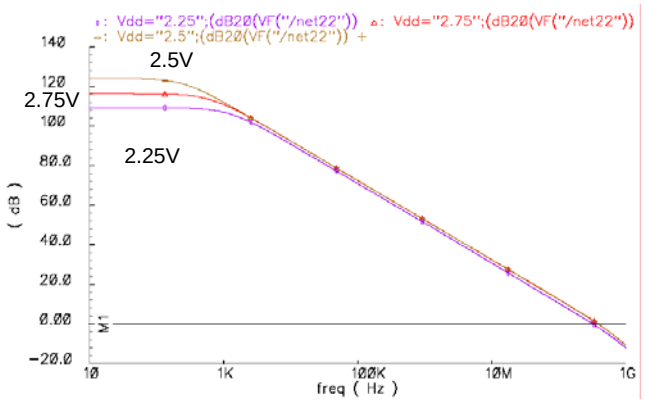
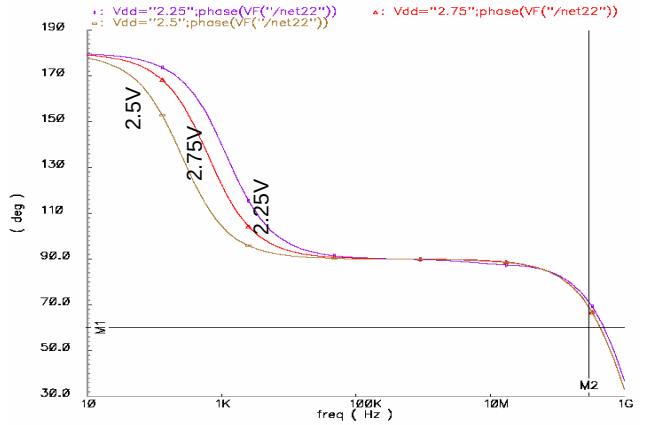


Figure 9: Differential output DC swing versus input voltage (vin+ only) under different power supplies.



(a) Bode plot (M1 marks out unity gain);



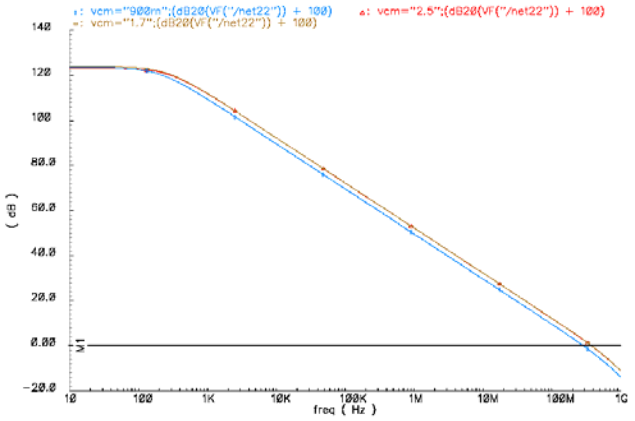
(b) Phase plot (M1 marks out PM of 60^o);

Figure 10: AC responses under different power supply.

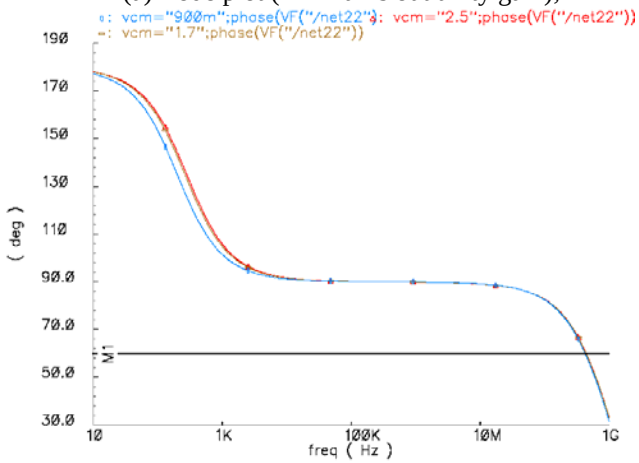
The simulated DC and AC responses under different power supply voltages and temperatures (25^{o}C and 85 ^{o}C) are listed in Table I. As shown in Table I, for all but one operating conditions, our design meets all the specification. Only at the worst-case scenario, (T=85 ^{o}C and V_{dd}=2.25V), the unity gain frequency drops to 156.8MHz, while the gain (94 dB) is still

TABLE I
SIMULATED RESPONSES OF THE OP AMP DESIGN UNDER DIFFERENT OPERATING CONDITIONS

Vdd (V)	Output Swing (V) (Desired:1.25±0.4)	DC Gain (dB) (Desired: ≥ 90)	Unity Gain f_0 (MHz) (Desired: ≥ 300)	Phase Margin (^{o}) (Desired: ≥ 60)
2.25(27^{o}C)	1.25±0.55	109	317	70
2.5 (27^{o}C)	1.25±0.75	124	381	64
2.75(27^{o}C)	1.25±0.9	116	387	63
2.25(85^{o}C)	1.25±0.55	95.1	156.8	82
2.5 (85^{o}C)	1.25±0.75	116.9	303	67
2.75(85^{o}C)	1.25±0.9	115	324	65



(a) Bode plot (M1 marks out unity gain);



(b) Phase plot (M1 marks out PM of 60^o);

Figure 11: AC responses at different input common mode voltage (Vincm:0.9V, 1.7V and 2.5V).

higher than the 90-dB requirement. By adopting some temperature compensation techniques in the bias circuit (such as band-gap based bias circuit), the unity gain frequency could be improved up to 300 MHz. Based on DC simulations under normal operation conditions, the obtained common mode gain of this design is –68dB and the common mode rejection ratio is larger than 300dB.

The total power consumption is 13mW under 2.5V power supply.

VI. CONCLUSIONS

In this paper, a single stage fully differential 90-dB op amp for standard 0.25μm process is designed based on folded cascode and "gain boosting" technique. When the differential output capacitor load is 2pf, this design demonstrates a DC gain of 124 dB with a unity gain frequency of 381MHz and a phase margin of 64^o. The performance of this op amp is comparable with the state-of-art designs in modern CMOS process.

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