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Design of PLC Timer System Based on ARM + FPGA

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Abstract: Based on the fact that a large number of timing controllers are needed in the applications like sequential logic control and programmable controller, this paper proposed a PLC timer system based on ARM+FPGA, in which ARM is used to execute user program while FPGA is used for timer operation in parallel. The FPGA timer module consists of timer controller, timer dynamic parameters and soft contact state register, the timer controller carries out counter operation for timing unit every 1ms, then results from timing operation would be saved in timer parameter list of a dual port RAM, when controller commands need to be executed via PLC, the timer will be used as a regular memory unit for W/R operation, thus no executing time of PLC program would be spared basically, which can well meet the system requirements where large number of controllers are needed. Simultaneously, principles of system composition, timing operation control and timing operation flow are all introduced followed by which a field test is also carried out for testament of the designed timer system.

Introduction

In the large-scale time order logic control and programmable controller(PLC) application system ,it needs to use a large number of timing control, its timing benchmark units has millisecond, second , minute , hour , etc. [1] . Because the number of timers is numerous, which sometimes are up to several hundreds, usually it applies the timing time of a timer in the microprocessor as the reference time ,each timing parameters of timing unit are stored in a storage unit , when the benchmark timing time reaches ,it uses time interrupt or inquiry method , executes the timing unit process program [2]; The more the timing unit of the timer system it has , the smaller the timing reference time it will take,and the longer the microprocessor CPU running time it occupies,which seriously impacts the execution speed of other program modules ; the more the requried timing unit of the microprocessor external expansion dedicated timer chip it has, the more the external expansion dedicated timer chip it has ,and the larger the circuit scale is .

At present, using FPGA designs electronic clock [3] , designs timer for the specific electronic system [4,5] , but the number of timer is less.About the autonomously developed small programmable controller which is composed of ARM + FPGA,it fully uses the function of FPGA high-speed parallel operation, and proposes the system that the embedded ARM microprocessor as the control module , FPGA as the timing parallel processing timer module , when the system is high-precision timing, it basically does not take up the PLC program execution time ,it's suitable for the requirement of syetem which requires a large number of timer timing and timing control.

Timer structure suggestion design

The PLC host of PLC structure which makes up ARM + FPGA is composed of the ARM module and the FPGA module two parts [6,7] ,The basic ideas of the design is based on the basic structure of the PLC host , and fully applies the functions of FPGA high-speed parallel operation processing,the specific timing operation of the timer is completed by the FPGA .

The timer system block diagram is shown in Fig. 1 , it’s composed of the ARM control module, dual-port RAM , FPGA timer modules.The FPGA timer module is composed of clock reference pulse signal generator ; timing controller ; timer contact bit unit memory , timing dynamic parameters memory etc.

In the FPGA , it establishes 256 dynamic parameters storage area of timer , 256 soft contact -bit units , there are 200 timer that the benchmark timing is 100ms , 10ms timer has 146, and 1ms timer has 10 . Each timer is corresponded to a dynamic parameter unit and a soft contact –bit unit . In the dual-port RAM ,establishes a timer parameter list , each timer corresponds to a static parameter unit and a soft contact-bit unit .

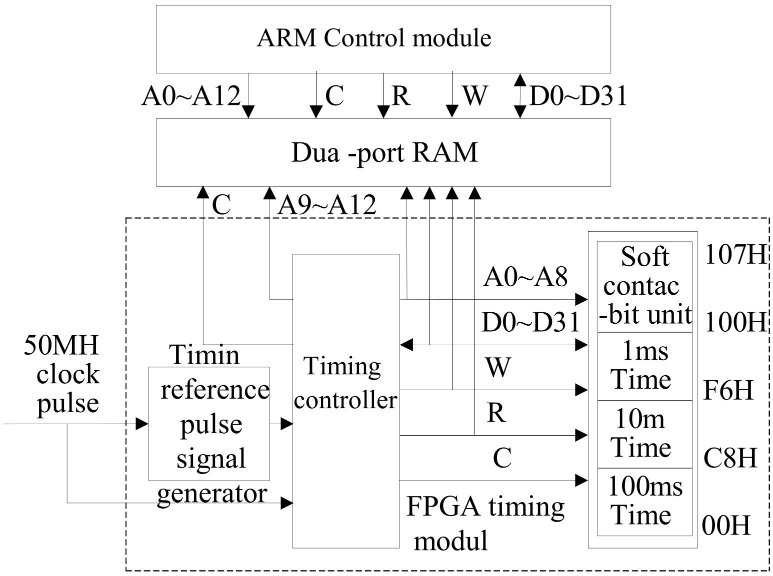


Fig. 1 Timer system block diagram

Timer system working principle

Timer working state parameter setting

In the timer system, each timer has a timer number, it’s coil is called a soft coil, contacts have move close contacts and move break contact , which are collectively referred to soft contact, the number of soft coils and soft contact is consistent with timer number, their number also can be understood as the address ; all timers have a same and minimal timing time, that is the timing reference time 1ms . Each timer needs to set the timing parameters in the program , timing time = reference time × timing parameter .

For a timer there are four states:

(1) application state : in the user program it whether appears the number of timer , sets the using flag bit , when using it’s set to "1" , otherwise it’s set to "0" ;

(2) energized state : timer soft coil whether gets electricity , sets the flag bit of getting and losing power , when it’s energized and set to "1" , otherwise it’s set to "0" ;

(3) timing working state : soft coil of timer gets electricity , when it’s conducting timing operation ,it’s set to "1", otherwise it’s set to "0 ";

(4) timing reaching states: timing time has reached , the number timer devices still get power and it’s set to "1", otherwise it’s set to "0 ".

For the four states of timer ,it adopts four flags-bit to indicate them. Each timer is respectively allocated a storage unit of 32-bit length as shown in Table 1 in the dual-port RAM and FPGA, in dual-port RAM , D27 ~ D0 store the set value of timer parameter , in FPGA ,they are the dynamic value of timer parameters .

Table 1 Timer 32 –bit storage unit setting table

D31	D30	D29	D28	D27~D0
Use flag bit	Energized flag	Timing operation	Timing reach	Timing parameters : The dual-port RAM : setting value FPGA: dynamic value

The operation control of the timer system

The operation of timer system is consisted of three parts : the first is the static compilation of the ARM control module to the PLC user program; the second is the dynamic compilation of the ARM control module to timer ;the third is the control of FPGA timing module to the timer.

PLC user program is stored in the memory of the ARM control module [6,7] . the ARM control module is a compiled agency of the PLC user program,which carries out static and dynamic two types of compilation to PLC user program , it conducts static compilation before the PLC user program is executed . the main function is that the PLC device is converted to directly address, and formes a new PLC program instruction sequence , and in the dual-port RAM establishes timer parameter list, timer parameters can be directly read and writtn by FPGA module .Dynamic compilation is the compilation of in the process implementing the new PLC program instruction sequence ,the main function is that the direct address of the operand in instruction is converted to the immediate data, dynamic operating status of the timer is transferred to the timer parameter table of dual-port RAM , the instruction sequence after dynamical compiled are transmitted to the dual port RAM, FPGA is the executive agency of the PLC program, the implement results are feed back to the dual-port RAM , FPGA timer module according to contents of timer parameter table, under the control of the system, conducts cycle counting control to each timing unit,the cycle time is 1ms , the timing results are feed back to the dual port RAM, ARM module and FPGA modules complete together the implementation of the ARM static compilation, the timer operation is controlled by the ARM module .

Fig. 2 is a simple timer ladder program ,in order to illustrate the process that ARM implements the timer operation .when static compilation, parameter 003 is written to the dual-port RAM timer parameter table corresponding to the timing parameter unit of T0 , sets the use flag-bit and it’s 1 .

The process of implementing the program in Fig.2 can be divided into four categories:

(1)when input signal X0 move and close is turned on , the timer T0 soft coil is energized ;

(2) timing time is reached,the X0 move- close stays on connection, the value of contact bit unit : "1" ;

(3) when input signal X0 from move –close is connected to move- break ,the timer T0 soft coil loses power , the value of contact bit unit : "0" ;

(4)when input signals X0 maintains a state of move- break , maintains the contact unit value of T0 is unchanged.

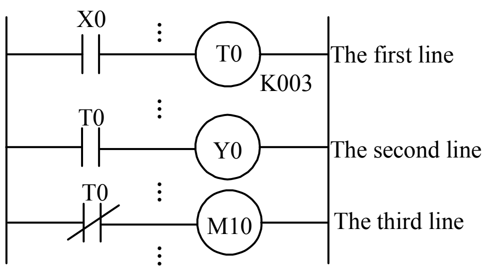


Fig. 2 Timer program ladder

For the frist case , when dynamic compilation, the timer corresponding to the getting electricity flag-bit is set 1.The ARM implements the second line program in Fig. 2 ,ARM directly read the contact unit value of T0 from the timer contact status storage area of dual-port RAM, FPGA timer control module in the handling timer timing process ,when the timing time is not yet reached , maintains contact unit value of T0 is unchanged; when the timing time is reached, T0 contact bit unit is set to1 . For the third case, when dynamic compilation, the timer corresponding to the getting electricity flag-bit is restored to 0 ,FPGA timer control module in the handling timer timing process , the contact bit unit of T0 is restored to 0 , and stops the timing operation of the T0 .

Timer operating procedure design

Compilation of ARM to the user program

When system is power-up , the storage unit contents of dual-port RAM are all cleared , when statical compilation that ARM PLC to user program, the D31 of timer used in the program is set to 1, 10ms timer parameters are expanded to 10 times ,100ms timer parameters are expanded to 100 times, the setting parameters are transferred to the D27 ~ D0 of that timer in the timer parameter list of dual-port RAM ; if the timer parameters is in the data register D ,then without conducting the parameter transmission, but D31 needs to set 1 . T0 in Fig.2, after statical compilation its parameters are : 8000_0003H .

Dynamic compilation is conducting read and write operations to the timer in the PLC program, the first is when the PLC instruction needs to read a timer contact information and participates logical operations .it only needs to remove the timer contact unit content from the timer contact information memory cell of the dual-port RAM ,the second is that when the PLC implements the instruction of timer soft- coil, judges the timer soft coil whether is energized , the timer parameters is from the D or immediate data, and carries out read and write operations , the program flow chart shown in Fig. 3 .

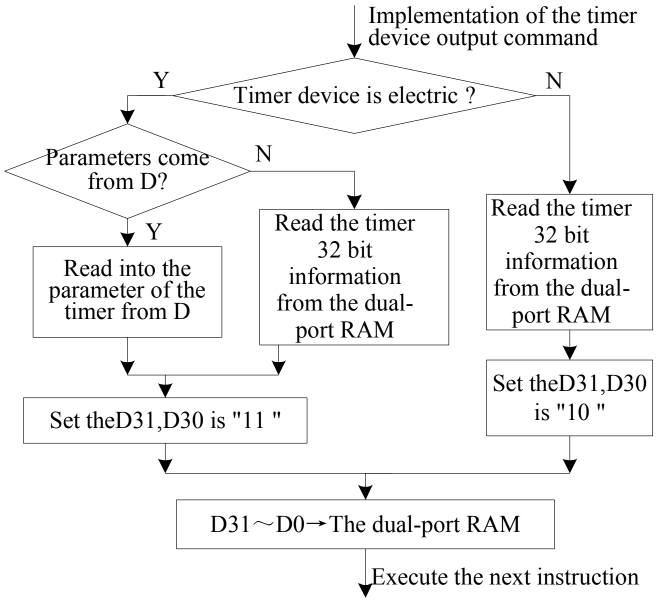


Fig. 3 Processing operation flowchart of dynamic compilation timer to output instruction

Set D30 bit , gets electricity is 1 , without geting electricity is 0 , and transmittes to the D30 bit of the timer in the timer parameter table .

FPGA timer module timing

Know from Fig. 1 , the 50MHz pulse as the system pulse of the FPGA timer module , the timing operation is executed under the action of system pulse, the clock reference pulse signal generator is dividing to system pulse,generates 1ms timing reference pulse,the timing controller circulatingly carries out once time operation to 256 timer every 1ms.

The contents of timer contact bit unit memory and timing dynamic parameters memory are all cleared when the system is reset. After the system is reset, FPGA timer module receives the starting commands which are sent from ARM, the timing controller starts running,Fig. 4 is a flowchart of the processing operation of the FPGA timing controller , see from that , according to the status of each timer D31 ~ D28 judges the outcome operation , the state of D29 and D28 are set by the timing controller , D31 and D30 are set when static compilation and dynamic compilation , timing operation to the timing unit is conducting the plus 1 operation , 110 × is the state that timer from never gets power " 0 " → " 1 " gets the power,the ×can be " 0 ",also can be " 1 " state.

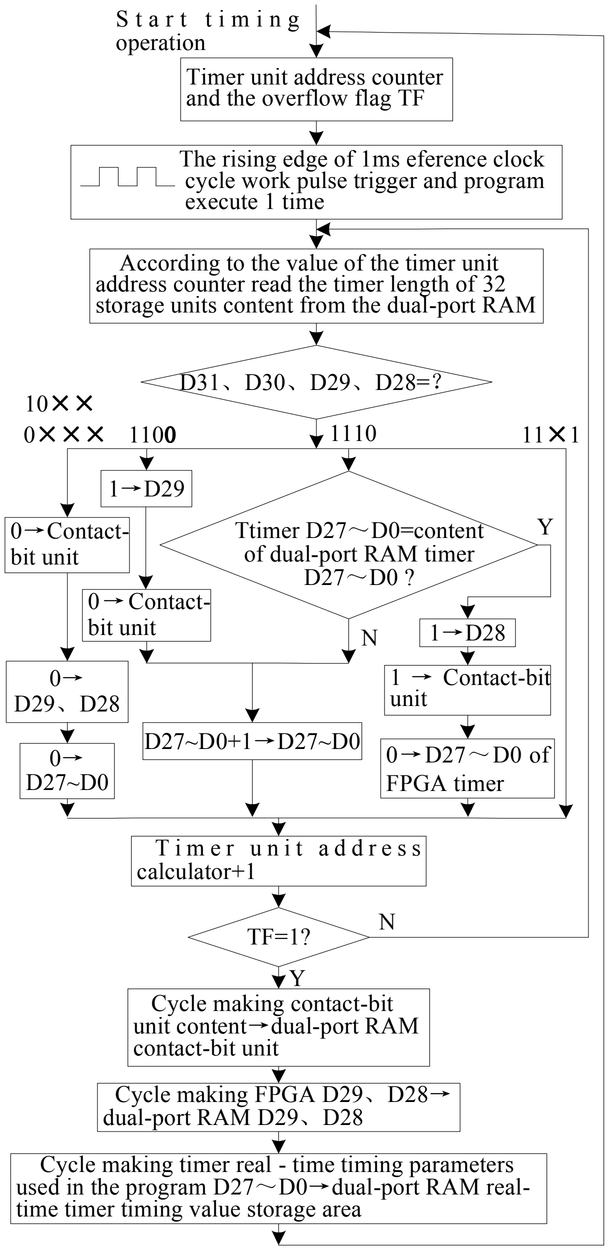


Fig. 4 The flow chart of the processing operation of the FPGA timer controller

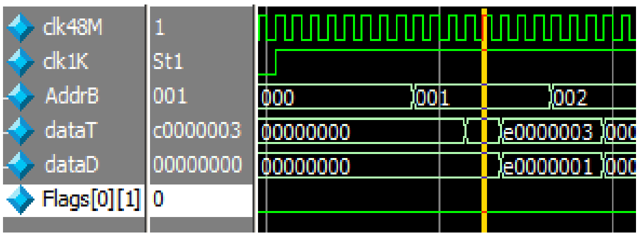
Function testing and simulation

The design uses the FPGA of Actel Corporation , under Actel Libero integrated development environment [8],it executes functional testing and simulation testing .

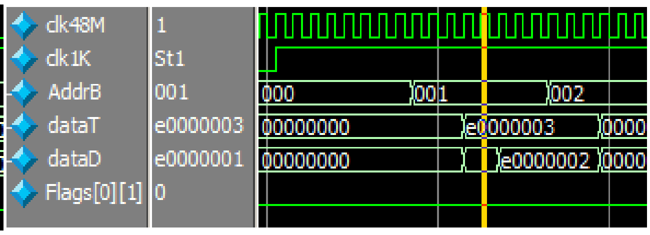
According to the timer processing operation flowchart of Fig. 3 , Fig. 4,when each rising edge of a 1ms pulse is triggerred, the timing controller starts working, conducts once timing counting operation to all the timing unit, The defined test parameters shown in Table 2 , the timing parameters which is set by the example of T0 as shown in Fig. 2 is 3ms, when static compilation D31 is " 1 ",when dynamic compilation D30 is "1 ", the test results of timer processing operation shown in Fig. 5 , Table 2 is the test parameters definition list in Table 5 .

Table 2 Test parameters definition list

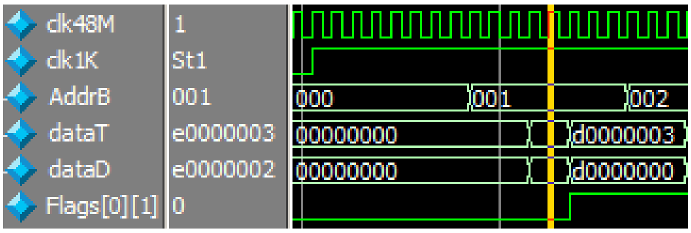
Code	Description
clk48M	48MHz System clock pulse
clk1K	1ms Timing reference pulse signal
AddrB	Timer address, that the timer number
dataT	Timer parameter setting values
dataD	Timer dynamic parameter values
Flags	Soft contact unit value



(a) The frist 1ms pulse action



(b) The second 1ms pulse action



(c) The third 1ms pulse action

Fig. 5 Under the action of 3 1ms pulse parameter status of T0

In Fig. 5, the four status bits of dataT of T0 initial value is " 1100 " .Under the action of first 1ms pulse, the D29 is set to "1", the high four bits of dataT is " 1110" , the dataD of T0 acts plusing 1 operation , shown in Fig. 5 (a) . Under the action of second 1ms pulse, the dataD of T0 acts plusing 1 operation again, other parameters are unchanged,shown in Fig. 5 (b) . Under the action of third 1ms pulse, the dataD of T0 pluses 1,and reachs the time of timing 3ms, the dynamic parameters of dataD of T0 are cleared , the setting value of dataT of T0 is unchanged, the status bit of static and dynamic is set to " 1101" , the corresponding bit Flags [0] [1] of T0 soft contact is set to 1 , shown in Fig. 5 (c),and meets the timing requirements .

Conclusion

A timer system which is mainly composed of the ARM control module, dual-port RAM and FPGA timer module , it applies the function of FPGA parallel operation ,and makes the ARM control module implement large-scale time control program or programmable controller user program , each timer meets the time operating conditions , the ARM control module transmits running status information through dual-port RAM to the FPGA timer module, under the conditions of doing not meet timer operation, it transfers the stopping running status information to the dual-port RAM module ; when the user program reads the storage unit information of the soft contact ,the ARM control module directly reads the contact status information from the dual-port RAM .It makes the PLC implement the timer instruction, timer as an ordinary storage unit conducts reading and writing operations . it basically does not take up the execution time of PLC program , improves the execution speed of user program, and high timing accuracy ,it’s applicable to the equipment which needs to a large number of timers and timing control .

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