Development of a Waveform Sampling Front-End ASIC for PET

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Abstract - We present a versatile method for signal processing as an alternative to conventional methods using discrete front-end electronics. A new Waveform Sampling Front-End (WSFE) ASIC for Positron Emission Tomography (PET) has been developed to digitize signals at an early stage. Each channel of the chip consists of a preamplifier, a variable gain amplifier (VGA) and a fast Analog to Digital Converter (ADC) per channel. Two such chips have been designed and experimental results are presented in this paper.

I Introduction

In Positron Emission Tomography, it is advantageous to digitize the signal from the detectors at an early stage for various reasons. Besides suppressing noise, it would allow one to choose from a number of options for extracting energy and time information. By utilizing ASIC technology rather than bulky, high power consuming conventional discrete analog electronics, it is possible to have large numbers of detectors.

A Waveform Sampling Front-End (WSFE) ASIC designed using Rohm 0.35 μ CMOS ASIC technology has been developed for such a purpose. Full custom ASIC technique allows us to integrate analog and digital circuits into one chip.

Each channel of the WSFE consists of a preamplifier, a VGA and a fast ADC. The preamplifier picks up detector signals and feeds them to the VGA which adjusts the amplitude to the maximum input range of the ADC. The ADC samples the amplified output signals of the VGA and converts them into digital waveforms.

II. First WSFE chip design and results

A first generation 8-ch WSFE chip has been designed and experimental results of each component are given below [1].

A. Charge Sensitive Preamplifier (CSA)

The cascode topology is the traditional architecture for CSAs. Here a regulated cascode topology [2] is adopted by adding a local feedback loop by to control the gate voltage of the cascode transistor. The schematic of the CSA is shown in Fig.1.

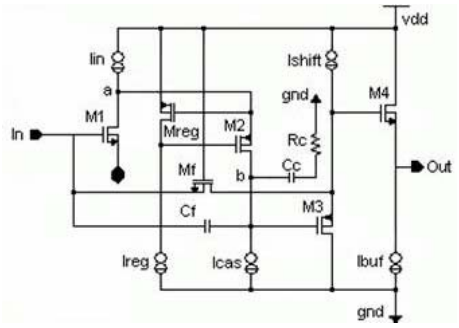

Fig.1 Schematic of the preamplifier

The rise time of the preamplifier is about 22 ns and the optimum Equivalent Noise Count (ENC) is about 4600 e-fwhm at shaping time of 6 μs, which is quite high.

B. Variable Gain Amplifier

The VGA is based on the Norton amplifier [3] and the schematic is shown in Fig.2. The gain can be varied from 3.6 up to about 25.

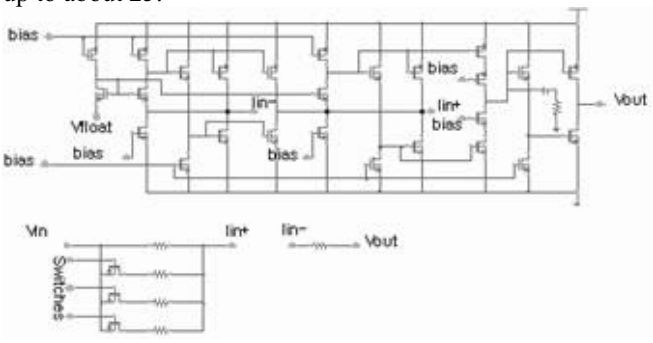

Fig. 2 Schematic of the VGA

C. Folding ADC

A 6-bit 100 MSPS folding ADC has been designed to sample the output of preamplifier [4]. The folding ADC is a

modified version of the Flash ADC but with folders to reduce the number of comparators needed and hence the power consumption while not losing its advantage of high speed and low latency. The schematic of the folding amp is shown in Fig. 3.

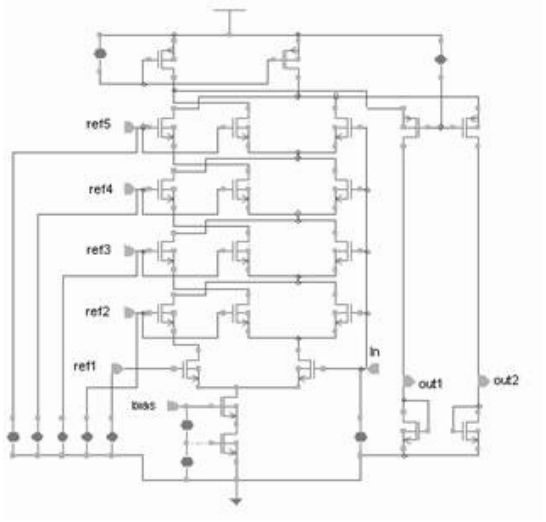

Fig. 3 Schematic of the folding amp

This folding ADC is linear and functions well at least up to a sampling rate of 50 MHz. The power consumption for 8 channels is approximately 1.2 W at that rate.

The differential nonlinearity (DNL) is 0.7 LSB while the integral nonlinearity (INL) was found to be 1.4 LSB. The Total Harmonic Distortion (THD) is -20 dB.

III. Improved WSFE chip design and results

Since the results from the first chip were not as expected, a new 10-ch chip was designed and tested [5]. The micrograph of this chip is shown in Fig. 4.

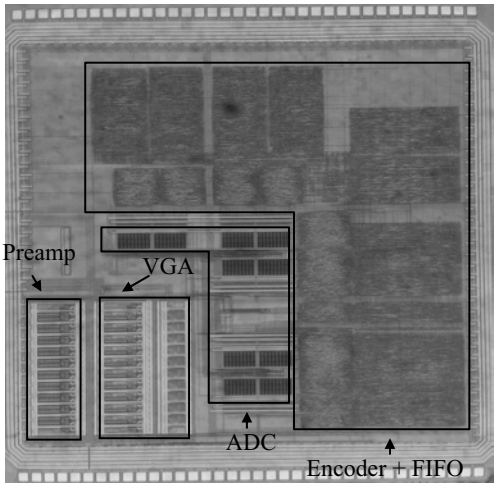

Fig. 4 Layout of the new 10-ch WSFE ASIC

The rise time of the preamplifier based on the telescopic-cascode structure, is about 25 ns although a faster rise time was expected. The optimum ENC is about 1300 e-fwhm at shaping time of 0.5 μs, several fold improvement over the previous chip..

A two stage VGA was designed. The rise time of the first stage was about 20ns and the gain could be varied from about 4 to 13. However, the second stage was not working as designed.

The new folding ADC was working at least up to a rate of 100 MHz. The DNL and INL are 1.1 LSB and 1.4 LSB respectively. One whole channel (excluding second stage of the VGA) was tested and the digitized 100mV input signals are shown in Fig. 5. The power consumption was about 1.2W for the whole chip.

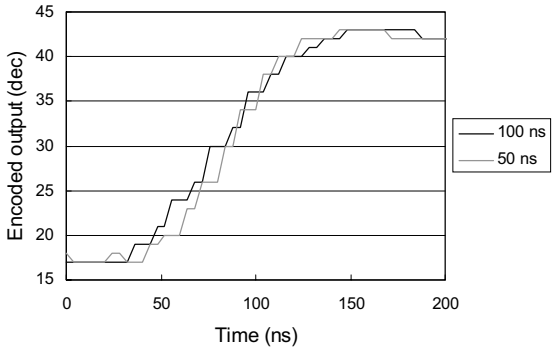

Fig. 5 Sampled step input of 50ns rise time

IV. Conclusions

Each component of the first WSFE chip was found to working although not as designed. Inconsistencies between simulation results and measured results arise from the inaccuracy of our simulation related to the layout process and the fabrication process parameters. Careful considerations of the layouts and testability of the chip produced a significantly improved second chip.

References

[1] JY. Yeom et al., "Design of New Front-End Electronics for APD-based Animal PET," IEEE Trans. Nucl. Sci., unpublished.

[2] D.M.Binkley, B.S.Puckett, et al., "A Power-Efficient, Low-Noise, Wideband, Intergrated CMOS Preamplifier for LSO/APD PET Systems," IEEE Trans. Nucl. Sci. NS-47: pp.810-817, June 2000.

[3] Hassan Elwan, Ahmed M. Soliman, and Mohammed Ismail, "A CMOS Norton Amplifier-Based Digitally Controlled VGA for Low-Power Wireless Applications," IEEE Trans. Nucl. Sci. NS-48: pp.245-254, March 2001.

[4] Michael P. Flynn and Ben Sheahan, "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," IEEE Journal of Solid-state circuits NS-33: pp 1932-1938, Dec 1998.

[5] JY. Yeom et al., "Development of a multi-channel Waveform Sampling ASIC for Animal PET with DOI Information,"Nucl. Instr. Meth. A, unpublished