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The Dual Sine Signal Generator Design Based on the Principle of Difference Frequency Filtering

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Abstract. The paper attempts to realize the processing scheme of low cost dual sine wave generator. It used single-chip microcomputer and CPLD(Complex Programable Logic Device) as the control core. It maked use of CPLD and discrete component simulations to implement DDS principle. It utilized the filter circuit, integrated op-amp circuit and multiplier circuit instead of DAC chip. The range of frequency, amplitude and phase difference are 1Hz~1000Hz, 1V~3V and 0^o~359^o, respectively. The results show that a 2-channel sine signal generator can be designed with adjustable frequency, amplitude and phase difference.

Introduction

As a kind of widely used signal source, sine signal source plays a very important role in the laboratory and in the design of electronic engineering[1].Currently, there are lots of people have designed and implemented a sinusoidal signal generator through making use of frequency synthesis technology[2,3,4,5,6]. In this paper, it uses the "MSP430 MCU + CPLD + analog discrete component" instead of a DDS chip to design a low-cost dual sine signal generator, which could be used as a analog signal source in the laboratory or a signal source in the teaching demonstration. The system provides a higher level of integration and simple operation, which makes it possible to be overhauled fast and accurately[7,8].

The Theoretical Principles of System Design

DDS Principle. The working principle of DDS is shown in Fig. 1.

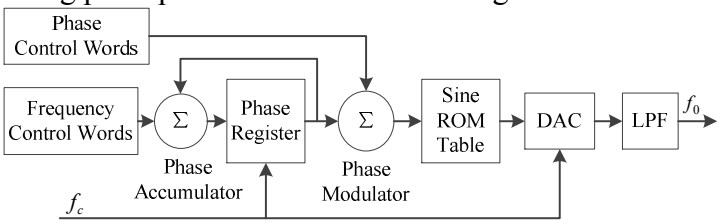


Fig. 1 The working principle of DDS

In Fig. 1, DDS consists of a phase accumulator, a phase modulator, a sine ROM lookup table, a digital to analog converter (DAC) and a low pass filter (LPF).At every clock, N-bit phase accumulator is accumulated with the feedback value. The result of the high L-bit is the address of the sine ROM table, and from the sine ROM table it reads the amplitude value to the DAC, and finally by a low-pass filter to convert a continuous sine signal output[9].

Adjusting Amplitude Accuracy Principle. The PWM signal is the periodic square wave signal with adjustable duty ratio. The trigonometric form of its Fourier series is shown in Eq. 1,.

$$f(t)=\frac{E\tau}{T_1}+\frac{2E\tau}{T_1}\sum_{n=1}^{\infty}Sa(\frac{n\pi\tau}{T_1})\cos(n\omega_1 t). \quad (1)$$

Where $f(t)$ denotes the PWM signal; E expresses the rectangular wave amplitude; τ shows the pulse width; T_1 is denoted as the period of the signal $f(t)$; $Sa(x)$ is expressed as sampling function.

From (1), it could obtain a DC voltage when making the PWM signal through a low pass filter. So the size of the DC component can be fully adjusted by the duty ratio of the PWM signal.

Difference Frequency Filtering Principle. After a sine signal multiplies a square wave signal, the result is given in Eq. 2.

$$f(t) = -\frac{AE}{\pi}\{\cos[2\pi(f_2+f_1)t+\varphi]-\cos[2\pi(f_2-f_1)t+\varphi]- \frac{1}{3}\cos[2\pi(3f_2+f_1)t+\varphi]+\frac{1}{3}\cos[2\pi(3f_2-f_1)t+\varphi]+...\} \quad (2)$$

Where A denotes the amplitude of the sine signal and E expresses the amplitude of the square signal. It can be designed to filter the components with f_2+f_1,$3f_2+f_1$,$3f_2-f_1$...frequendies out and restain the component with f_2-f_1 frequency. With this method it could get the signal with frequency f_2-f_1, phase φ, and amplitude AE/π.

The Overall System Design Solutions

The overall system design includes the minimum single-chip system unit, CPLD control logic unit, analog circuit unit and waveform output section. Wherein, in DDS principle, the DAC part is entirely replaced by amplification circuit and filter which is make up of simulation of discrete component unit. The overall system design is shown in Fig. 2.

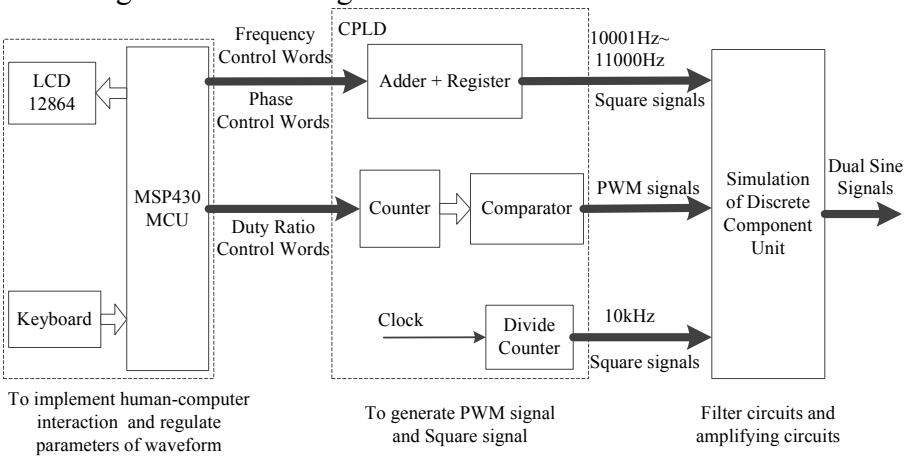


Fig. 2 The overall system design

Hardware Design and Implementation

Multiplier Circuits. In analog circuits, the core component is 74HCT4053, which is a triple 2-channel analog multiplexer / demultiplexer. The multiplier circuit connection design is shown in Fig. 3.

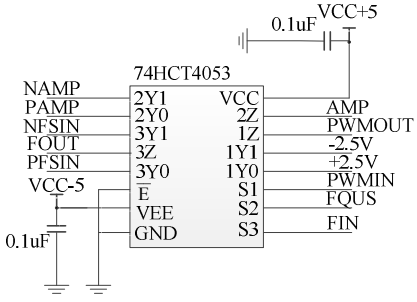


Fig. 3 Multiplier circuits

Standard Voltage Circuits. In order to generate a stable ±2.5V DC voltage, a DC voltage is applied to the ends of 5V circuit through the voltage-regulator diode and the phase inverter. The design is presented in Fig. 4.

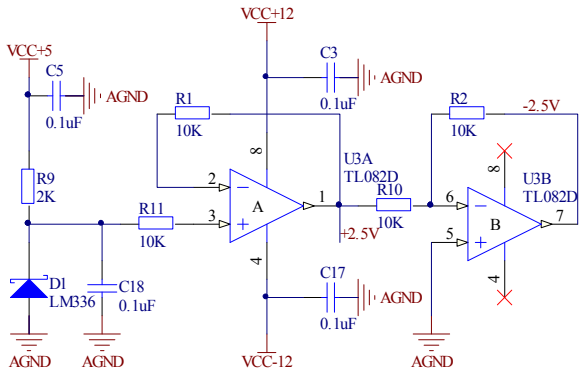


Fig. 4 Standard voltage circuit

Filter Circuits.In analog circuits. As the frequency characteristics of the system have no special requirements, it considers to use a third-order Butterworth I type low-pass filter[10].The design is presented in Fig. 5.

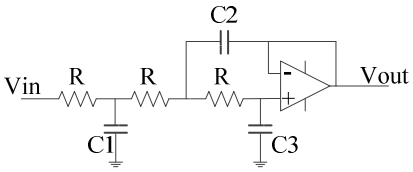


Fig. 5 Filter circuits

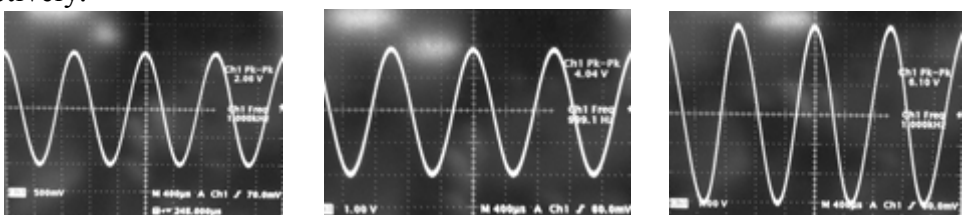
Software Design and Implementation

MSP430 Microcontroller Programming. In this design, it changes the size of the frequency, amplitude and phase through the keyboard input. MSP430 MCU makes use of LCD12864 to display values for each set, which achieves human-computer interaction, making the operation more convenient and faster.

CPLD Programming. In Fig. 2, it inputs control commands from the matrix keyboard (ie, to adjust the value of the amplitude, frequency and phase difference). Then it transfers duty ratio control words, frequency control words and phase control words from MSP430 MCU to CPLD. After analyzing the words, CPLD generated PWM signals with adjustable duty ratio, square signals ranging from 10001Hz to 11000Hz and 10kHz square signals[11].

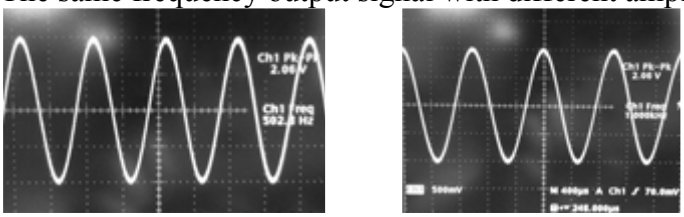
Index Test

The system outputs A and B, respectively connect to CH1 and CH2 of a digital oscilloscope to test the index of the system.The amplitude, frequency,and phase test results are shown in Fig. 6, Fig. 7 and Fig. 8, respectively.



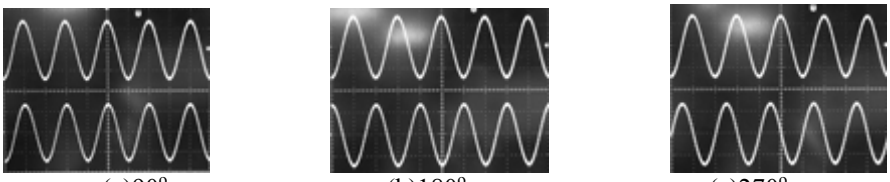
(a)1000mV (b)2000mV (c)3000mV

Fig. 6 The same frequency output signal with different amplitudes



(a)500Hz (b)1000Hz

Fig. 7 The same amplitude output signal with different frequencies



(a)90° (b)180° (c)270°

Fig. 8 The same amplitude and frequency output signal with different phase differences

From Fig. 8, when the frequency is constant , the amplitude error is small.From Fig. 9, when the amplitude is constant , the frequency error is small.From Fig. 10, when the amplitude and frequency are constant, the phase error is small.

Conclusions

The system has completed the design and implementation of dual sinusoidal signal generator.
1. It has studied the digital direct frequency synthesis technology in both the theoretical and practical aspects.
2. It has used CPLD and analog discrete components instead of a DDS chip to achieve DDS principle.
3. In particular, it has used analog filters, operational amplifiers and multipliers instead of a DAC chip to complete digital to analog conversion.

Acknowledgements

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