Review of Capacitive Threshold Gate Implementations

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Abstract. This is an in-depth survey paper on capacitive hardware implementations of threshold logic gates. The different VLSI solutions include the switched capacitor and the floating gate and their variations. It will be shown how the distinct original proposals from both categories have evolved to become quite similar. The problems with this kind of implementations are pointed out, and their applications are discussed.

1 Introduction

In the last decade the tremendous impetuous of VLSI technology has made neurocomputer design a really lively research topic. Research on hardware implementations of neurons has recently been very active. This has included extensive investigation on implementations of threshold logic gates (TLGs), one of the well-known neuron models. TLGs compute the weighted sum of their n inputs, x_1, x_2, …, x_n, and compare it to the threshold θ. They produce an output 1 iff the weighted sum is equal or greater than the threshold. They are defined by n+1 real numbers: threshold θ and weights w_1, w_2, …, w_n, where weight w_i is associated with input variable x_i.

In addition of being useful as a neuron model, there are many theoretical results showing that TLGs are more powerful/efficient than classical Boolean gates. These have been another motivation to investigate VLSI implementations of such gates.

The number of proposed TLGs implementations reported in the literature starting from the mid 50's is in the order of hundreds. Three different categories have been identified [1]: pure CMOS solutions, capacitive solutions, and conductance solutions. This paper focuses only on capacitive implementations.

The concept underlying capacitive TLGs is the use of an array of capacitors to implement the required weighted sum of inputs introduced as early as mid 60's [2]. Distinct circuits structures have been proposed which differ in the way the value of the threshold is set, and in the circuit techniques used to carry out the comparison involved in determining the output value. Capacitive threshold-logic gates have been classified into two major groups: Capacitive Threshold Logic (**CTL**), and Neuron MOS (ν**MOS)**, also known as multi input floating gate transistor (MIFG or MFMOS). The paper is organized as follows. Sections 2 and 3 describe CTL-based and νMOS-based solutions respectively. Finally, Section 4 summarizes the evolution, problems and suitable applications of the capacitive TLGs.

2 CTL Based Solutions

Originally introduced in 1987 [3], the main idea of capacitive solutions was to use switched capacitors, switches and inverters, and to take advantage of the inherent saturation of the inverters to implement the neuron non-linearity without additional elements. This first approach required a somehow complex three-phase clock. The principle of capacitive synapse was presented also in [4] with the same three-phase clock. It has quickly evolved into a simpler two-phase clock solution [5], known as the capacitive threshold logic (**CTL**) gate. Its conceptual circuit schematic is shown in Fig. 1 for an *n*-input gate. It consists in a row of capacitors C_i, $i = 1, 2, \ldots, n$, with capacitances proportional to the corresponding input weight, $C_i = w_i \times C_u$, and a chain of inverters which functions as a comparator to generate the output. This TLG operates with two nonoverlapping clock phases Φ_R and Φ_E. During the reset phase, Φ_R is high and the row voltage V_R is reset to the first inverter threshold voltage while the capacitor bottom plates are precharged to a reference voltage V_{ref}. Evaluation begins when Φ_E is at a logic 1, setting gate inputs to the capacitor bottom plates. As a result, the change of voltage in the capacitor top plates is given by $\Delta V_R = \left(\sum_{i=1}^{n} C_i (V_i - V_{ref}) \right) / C_{tot}$ where C_{tot} is the row total capacitance including parasitics. Choosing adequate definitions for V_{ref} and C_i as functions of the input weight and threshold values, the above relationship can be expressed as $\Delta V_R = \left(\sum_{i=1}^{n} (w_i x_i - \theta) C_u V_{DD} \right) / C_{tot}$. Together with the comparison function of the chain of inverters give the TG operation: $V_o = V_{DD}$ if $\sum_{i=1}^{n} w_i x_i \geq \theta$, and $V_o = 0$ if $\sum_{i=1}^{n} w_i x_i < \theta$. Computation of a large number of input vector between two consecutive reset phases is possible.

Experimental results from different CTL gates fabricated in a standard-CMOS technology [5], [6], have shown the proper functionality of this type of TLG and its large fan-in capability (fan-in < 128-256). This later feature is due to the auto-offset cancellation technique widely used in chopper-type CMOS comparators. Originally, CTL gates needed a double-poly process. In [6] the MOS capacitor is used with a small penalty on the fan-in (fan-in < 64). The main drawbacks of CTL gates are: their large delays, their large area (the estimated area of the unit capacitor is equivalent to several minimum sized inverters), their DC power consumption, and the threshold value programming mechanism. Developments after the CTL have been proposed which overcome some of its limitation. We briefly summarize some of them here.

The fact that the threshold value is set by an analogue reference voltage complicates its integration. This problem is solved by the improved CTL gate [6] which operates ex-

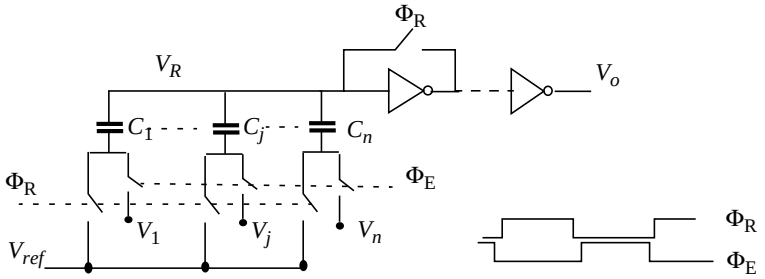

Figure 1: Capacitive Threshold Logic (CTL)

clusively with binary input logic levels. Another solution for this problem is the Capacitor Programmable CTL gate (**CP-CTL**), [7] which does not rely on the presence of additional external voltages. Fig. 2 depicts its circuit schematic. The CTL gate is augmented with a number of capacitors. The programming of the gate is now achieved by setting V_{ref}, V_{eval1}, V_{eval2}, and V_{reset} to readily available voltage levels. Different combinations of GND, V_{DD} and $V_{DD}/2$ (programming methods) can be used.

Finally, another variation called Balanced-CTL (**B-CTL**) [8] is shown in Fig. 3. The requirement for a highly precise reference voltage is eliminated by implementing functions with thresholds equal to 0. This is not a restriction on the class of functions that can be implemented, since any TL function (TLF) can be converted into an equivalent TLF with threshold equal to zero by inverting certain inputs, and changing the sign of their associated weights. The basic structure is formed by two banks of capacitors (Bank A and Bank B in Fig. 3). Both banks are connected to a differential amplifier that determines which bank has a larger number of inputs at logic one. That bank has a higher voltage level on its common line. This gate implements threshold functions with thresholds equal to zero if the inputs having positive weights are connected to one bank and the inputs having negative weights are connected to the other one. One additional half capacitor unbalanced the voltage level at the amplifier inputs in case both banks have an identical number of high-level inputs. B-CTL gates operate from one clock that switches the gate between two states: reset and evaluate. Their main characteristics are high fan-in and low power consumption.

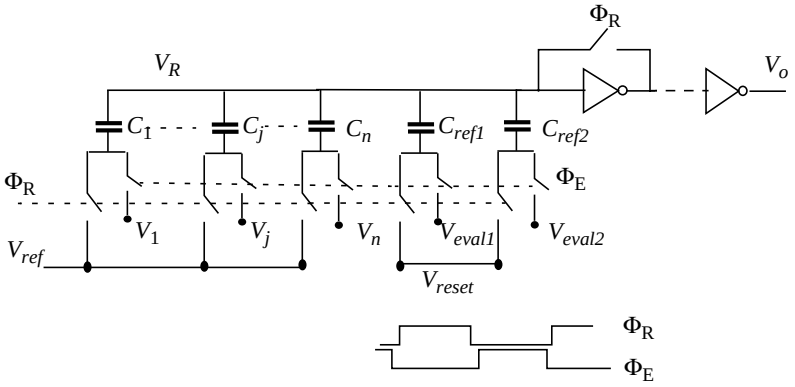

Figure 2: Capacitive Programmable CTL (CP_CTL)

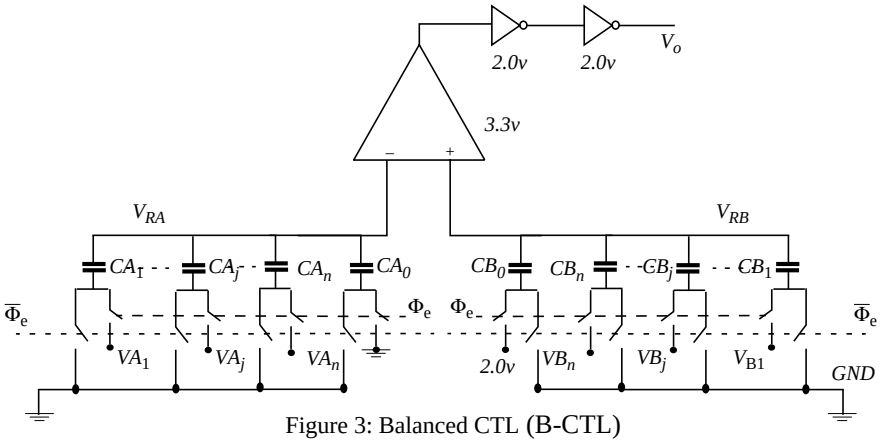

Figure 3: Balanced CTL (B-CTL)

3 Neuron-MOS Based Solutions

Neuron-MOS (ν**MOS**) TLGs are based on the νMOS transistor [9]. This transistor has a buried floating polysilicon gate and a number of input polysilicon gates capacitively coupled to the floating gate. The voltage of the floating gate becomes a weighted sum of the voltages on the input gates, and controls the current in the transistor channel.

The most simple νMOS-based TLG is the complementary inverter using both *p*- an *n*-type νMOS devices [10] [11] [12].A schematic of this TG is shown in Fig. 4. It consists of a floating gate, which is common to both the PMOS and the NMOS transistors, and a number of input gates (V_{x1}, V_{x2}, ..., V_{xn}), corresponding to the threshold gate inputs plus an extra input (indicated by V_C in Figure 4) for logic threshold adjustment, as will be explained later. Without using the extra control input, and assuming the charge in the floating gate is zero, the voltage in the floating gate is given by $V_F = \left(\sum_{i=1}^{n} C_i V_{xi} \right) / C_{tot}$, where C_i is the coupling capacitance between the *i*-th input and the floating gate, and C_{tot} is the total capacitance, including the parasitic capacitances at the floating gate C_c, $C_{tot} = \sum_{i=1}^{n} C_i + C_c$. As V_F becomes higher than the inverter threshold voltage, V_{TH}, the output switches to logic 0.

In the case of the simple, **static** ν**MOS**, the gate's threshold is adjusted via the threshold programming voltage V_C. It is obvious that this νMOS TLG is very simple and very compact. However, there are a number of well-known problems. Degradation in the long-term stability is anticipated due to the use of a floating gate. Sensitivity to parasitic charges in the floating gate and to process variations could limit its effective fan-in, unless adequate control is provided. In particular, ultraviolet light (UV) erasure is required for initialisation/reprogramming. This gate also has large DC power consumption. Different schemes have been proposed to alleviate at least part of these problems.

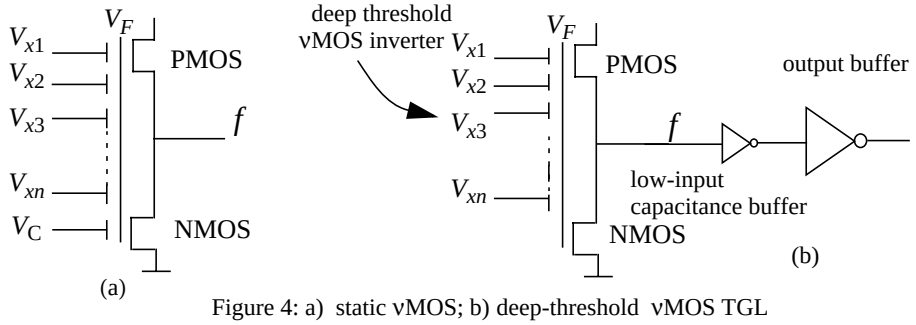

Figure 4: a) static νMOS; b) deep-threshold νMOS TGL

The problem of large power dissipation in the simple static νMOS TGL was solved by the **deep-threshold νMOS TLG** [13]. The gate is composed of a deep-threshold νMOS inverter and a two-staged buffer as depicted in Figure 4b. Deep-threshold inverters have transistors (NMOS and PMOS) with a threshold voltage large enough so that there is not DC pass current at whatever multiple logic levels the potential of the common floating gate is. This gate dissipates significantly less power than conventional static νMOS TGL (a reduction by a factor 1/30 has been reported for a case study consisting of a number detector). There is a penalty in speed. However the power reduction compensates the increase in delay. Thus, this gate exhibits better power-delay products. For the above case study the PDP figure of merit are 1/3.5 and 1/6 of those using standard CMOS technology and a conventional νMOS implementation respectively.

In the **clock-controlled νMOS** TLG [14] [15], shown in Figure 5, a clock-driven switch is attached to the floating gate to initialize the floating-gate charge (reset phase). This switch short-circuits the floating gate and the inverter output, thus biasing the inverter at the most sensitive point of the inverting characteristics. This is the same auto-offset cancellation technique used for CTL gates. At the same time the logical threshold of the gate is correlated with the physical threshold of the inverter. That means that, in each reset phase, the floating-gate charge is refreshed, avoiding the problems of parasitic capacitances and long-term stability. The inverter threshold is also automatically readjusted, reducing the sensitivity to process and ambient parameters variations, and increasing the fan-in of the gates. The gate is not very fast: a neuron with 32 synapses of 5-bit accuracy in 0.8 μm CMOS exhibit delays in the range 3–17 ns [16]. These dynamic versions of the νMOS have relatively high static power and might require multiple clock phases.

The static power consumption of the basic νMOS TG can be eliminated, and its speed increased, by a current comparison between a νMOS transistor and a reference device, using a positive feedback circuit [14]. The symmetry of the layout is important in this solutions. Figure 6 depicts the circuit schematics of TLGs operating on this basis. Fig. 6a shows a configuration called **sense-amplifier νMOS** TLG [15]. Other variations are described in [17] [18] and [19]. Although these circuits do not have an offset cancellation mechanism, fluctuation in device parameters can be compensated by the differential configuration. Speed improvements by a factor of 5 and power savings for this gate over the static νMOS are reported. Finally, Fig. 6b shows the configuration

called charge recycling threshold logic (**CRTL**) gate [20]. In fact, the CRTL gate achieves the lowest power consumption when compared with clocked νMOS [15], and other TLG implementations [19], [21]. CRTL have been tested for process variations at 45 corners, and seem to be robust. A 4-bit carry look ahead adder using CRTL gates was implemented in a 0.25 μm double poly CMOS process [22]. It can be operated at a frequency in excess of 400MHz. At 100MHz with V_{DD} = 2 V, dissipates 0.5 mW, *i.e.*, 15-20% lower power dissipation than other capacitive TLGs Very recently, a novel self-timed threshold logic (STTL) has been proposed [23]. The solution is low power (as being differential), and eliminates the clock at the expense of a double rail signalling and the additional "enable generate" block. It is too early to say if the power reduction due to the elimination of the clock and its distribution is off-balanced by the "enable generate" block required by each gate. Obviously, low power solutions have to be used in designing this block. The only results reported so far is a (7,3) counter in a 0.25μm double poly CMOS, which has a delay of 1.4ns and dissipates 870 μW@2V when driven by a 300MHz enable signal.

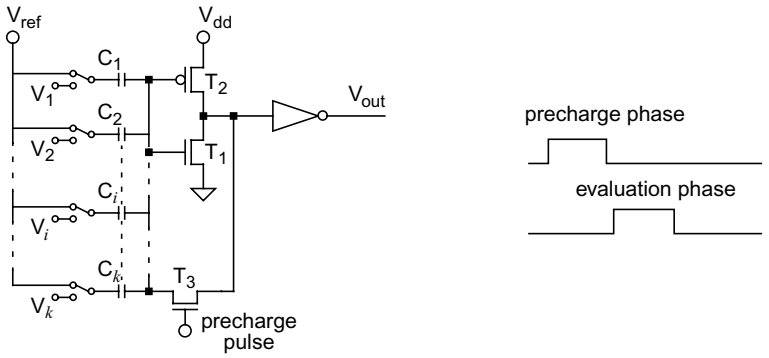

Figure 5: clock-controlled νMOS TGL

4 Analysis

Although originally CTL and νMOS approaches were different: static versus clocked and different mechanisms for setting the threshold value, their current developments have become increasingly similar. Advanced representative solutions from both categories are differential and allow straightforward implementation of both positive and negative weights. In addition they exhibit low power dissipation. Recently [22], the capacitor sharing technique has been introduced which allows significant area reduction in those networks of TLGs where two or more gates share inputs with same associated weights.

Capacitive implementations are multivalued in nature. Each distinct weighted sum of inputs is represented by and analog voltage. This translates in reduced noise margins and sensitivity to process variations. This could limit the effective fan in. In [24] a very thorough analysis with respect to parameter variations, namely capacitances and the sensing amplifiers of νMOS TLGs using a dynamic comparator latch for sensing is carried out. The dominant mismatch originates from the input offset voltage variations of the sensing circuits. Measured results show that the most critical components are the

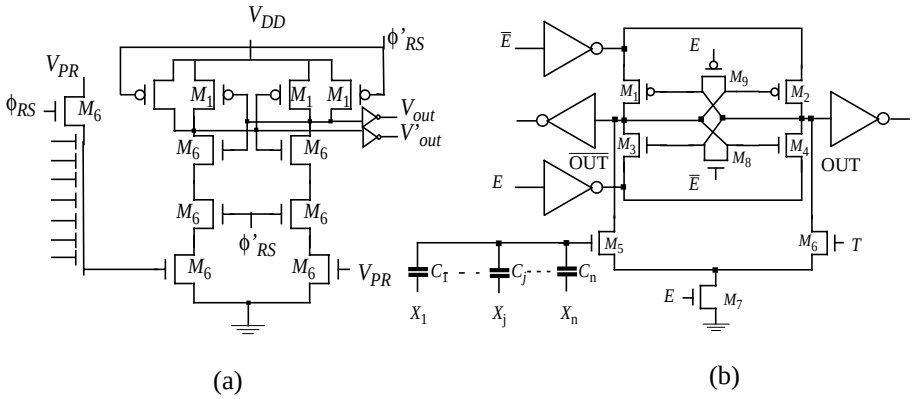

Figure 6: a) sense-amplifier νMOS TGL, b) CRTL

comparators circuits. Improved noise margins can be traded off for increased layout areas and increased power consumption (due to increased capacitances). They conclude that this is a problem that will be exacerbated in future CMOS technologies, since lower supply voltages and increased device mismatch will have a diminishing effect on the threshold window, sensing margins, signal to noise ration, and reliability. In addition, it is claimed that a careful comparison with the area consumption of a standard CMOS logic circuit is absolutely necessary. However, [24] explicitly mentions that there are applications where capacitive devices can be employed advantageously, like threshold logic circuits with low logic depth implemented in fault tolerant architectures requiring high functional densities (e. g. data processing architectures in image sensors). In fact, a commercial finger print sensor array for image processing based on this kind of implementations exits [25].

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