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MAXIMUM POWER POINT TRACKING USING RIPPLE CORRELATION CONTROL WITH AN INTERLEAVED SEPIC CONVERTER FOR PHOTOVOLTAIC APPLICATIONS

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Maximum power point tracking using ripple correlation control with an interleaved SEPIC converter for photovoltaic applications

by

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Thesis

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Dedication

I would like to thank my family and friends for their support. I would also like to thank my advisor Dr Kwasinski for his help and patience while guiding me. I also thank my parents for supporting me in my endeavors.

Abstract

Maximum power point tracking using ripple correlation control with an interleaved SEPIC converter for photovoltaic applications.

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This thesis examines the use of ripple correlation control as a maximum power point tracking algorithm with an interleaved SEPIC converter for use with a solar array. The suitability of existing topologies for use with photovoltaic applications and the tradeoffs involved are discussed. The advantages of interleaving in converters are examined and the benefits it provides to photovoltaic applications are discussed. An interleaved SEPIC converter operated in interleaved mode with a photovoltaic array is studied. The operation of ripple correlation control as a maximum power point tracking technique applied to the interleaved SEPIC converter is examined and simulations with results are presented.

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CHAPTER 1- INTRODUCTION

Solar photovoltaic energy has gained recognition as an alternative source of energy. In photovoltaics, the basic building block is the solar cell which is a pn junction diode where the incidence of light on the pn junction causes the development of a potential difference across the junction which initiates the flow of a current in an external circuit. Several such cells are connected in series parallel connection to form a solar array. The solar array has nonlinear characteristics as shown in fig 1.

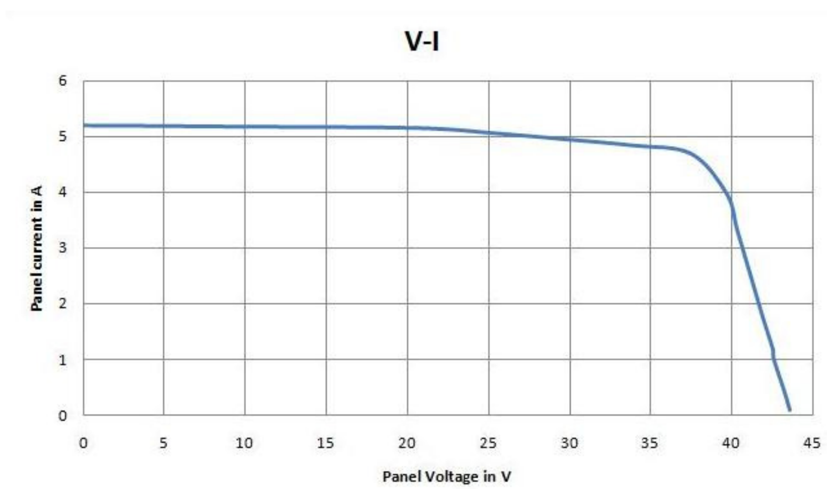

Fig. 1 I-V Characteristics of solar photovoltaic array

The theoretical equation to model the PV cells I-V characteristic based on the single diode model is given in equation (1) from [3].

$$I = I'_{sc} - I_{01}\left(e^{\frac{q(V+IR_S)}{KT}} - 1\right) - \frac{V+IR_S}{R_{sh}} \tag{1}$$

Where

I=PV cell current

I'_{sc}=The light generated

I_{01}=the dark saturation current

q = the charge on an electron (Coulomb)

K = The Boltzmann constant (j/K)

T = Cell temperature (K)

V = PV cell voltage

R_s & R_{sh} =The cell series and shunt resistance

The PV cell current and voltage are dependent on cell temperature and the radiation incident on the cell, since temperature and incident radiation are continuously varying throughout the day when the array is operating, The PV cell characteristics are continuously varying throughout the day, the variation with incident radiation in figure 2 and with temperature is shown in figure 3. Variations may also be caused by the partial or complete shading of the array. The interaction of variations due to temperature, incident radiation and shading etc. give rise to various combinations of the characteristics presented in figures 2 and 3.

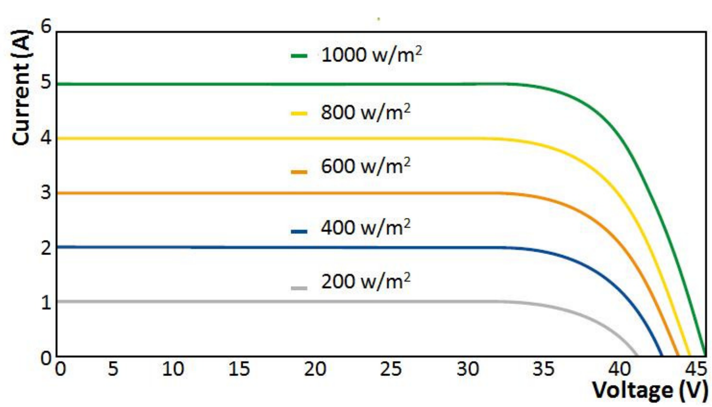

Fig. 2 I-V Characteristics variation with radiation intensity [3]

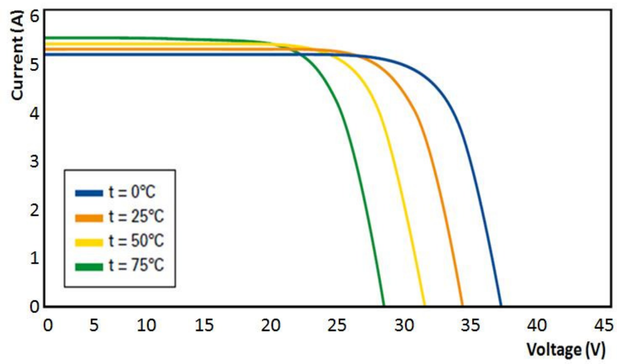

Fig. 3 I-V Characteristics variation with temperature [3]

The efficiency of conversion of the incident radiation to electrical energy in the PV cell is low and is of the order of about 15% [24]. Compared to the cost of electrical energy available from conventional sources the cost of energy from photovoltaics is still fairly high so it is important that the maximum available amount of energy be extracted from the solar array. Apart from the cost, converters used for photovoltaic applications also suffer from reliability issues and one of the common reasons for failure are failed electrolytic capacitors used in filters [25]. Thus it is important not only to maximize the extracted energy but also to ensure that the converter does not require failure prone components like large capacitors.

The maximum power can be drawn from the array by operating it at the voltage and current corresponding to the knee of the curve which is the maximum power point of the curve. The maximum power point however is continuously changing as the array characteristics change. The variation in the maximum power point and the equivalent array impedance is shown in figures 4 and 5. If a fixed load was connected to the array terminals, maximum power will not be extracted under varying conditions

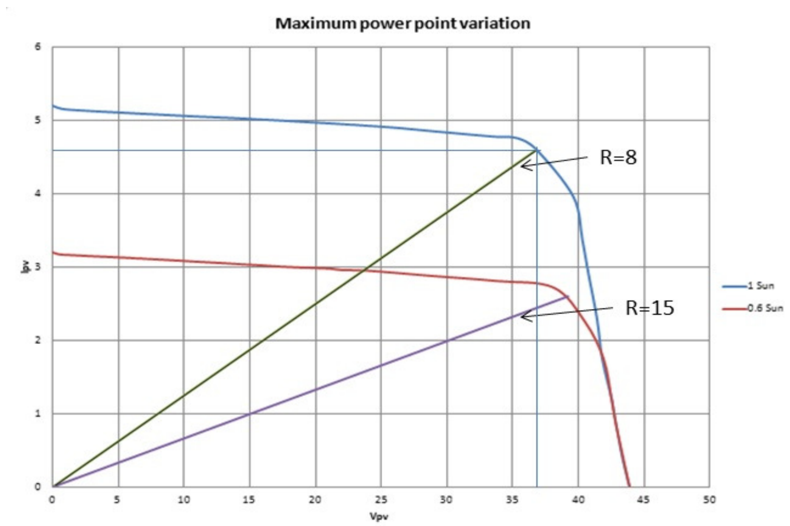

Fig. 4 I-V curves with panel resistance for varying conditions

The resistance of the array corresponding to the maximum power point under a particular set of conditions is 8ohms and under a different set of conditions is 15ohms so loading it with a fixed resistance will not draw the maximum available power from the array under all possible conditions as the load impedance is not matched with that of the array.

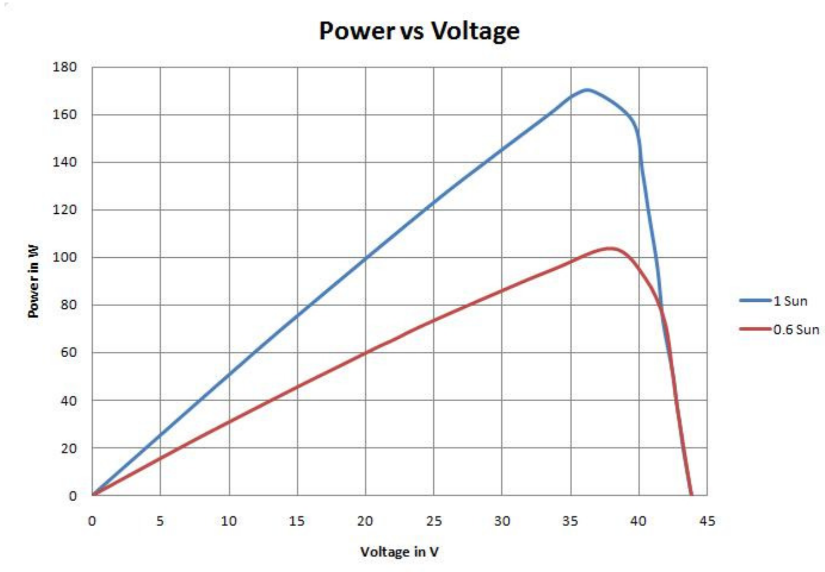

Fig. 5 Maximum power point variation

If the maximum power is to be extracted from the array then a maximum power point tracking (MPPT) circuit is introduced between the array and the load. The MPPT circuit is a DC-DC converter that is operated such that the fixed load resistance matches that of the array under varying conditions. It operates as the DC equivalent of a transformer with variable turns ratio. The MPPT is done by varying the duty cycle of the switching element in the converter. Varying the duty cycle causes the voltage and the current at the output of the converter to change thereby varying the impedance seen at the input of the converter which is also the output of the solar array. The MPPT circuit has two parts to its implementation one of which is the actual converter circuit through which the energy from the array flows and the other is the control circuit through which the algorithm which is used to track the maximum power point of the array is implemented. Various choices of topologies are available for the converter circuit and for the control algorithm. These are discussed further in the following sections.

CHAPTER-2 CONVERTER TOPOLOGIES

Various different dc-dc converter topologies have been used as MPPT circuits. Irrespective of their differences they all try to extract the maximum amount of power from the solar array with as little loss of energy as possible within the circuit itself. The nonlinear characteristics of the solar array were presented in fig 1 and the variation of power with panel voltage in figure 5. The MPPT circuit tries to operate such that the current and voltage at the array terminals are those corresponding to that of the maximum power point; this translates into being able to match the load impedance to the array impedance under all conditions.

The array being a DC power source, the current drawn from the solar array should ideally be ripple free for efficient extraction of energy, but the DC-DC converter is a switching converter which inherently introduces a certain amount of ripple in the array current thereby reducing the efficiency with which energy can be recovered from the array. Usually this ripple is minimized by using a filter at the array terminals. While this is a solution, the magnitude, cost and life of the filter components are dependent on the type of converter used. Converters based on buck, boost and buck/boost derived topologies are used for tracking the maximum power point and each of them have relative merits and demerits. Thus a converter that is capable of operating with the array while drawing current with the least ripple magnitude and able to provide an output voltage with very low ripple without requiring large filter components would be most suitable to extract energy. The MPPT circuit is also required to track the maximum power point under all possible conditions so that the maximum amount of energy is extracted from the array. Different DC-DC converters satisfy these requirements to different extents and are discussed in further detail below.

2.1 BUCK CONVERTER

A typical buck DC-DC is converter shown in fig 6. The equations determining the relation between input and output parameters are as per equation 2,.

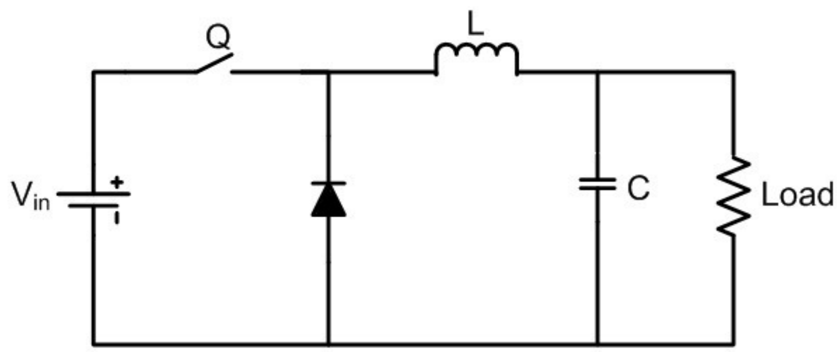

Fig. 6 Basic Buck converter

$$\begin{cases} V_o = V_{in} \times D \\ I_o = \dfrac{I_{in}}{D} \\ R_{in} = \dfrac{R_o}{D^2} \end{cases} \quad (2)$$

WhereV_{in},I_{in} R_{in} andV_o,I_o R_o are respectively the voltage, current and resistance at the input and output of the converter and 'D' is the duty cycle of the switch Q

Buck converter circuits are only capable of stepping down the input voltage and making the load resistance appear larger than it actually is at the array terminals. The circuit implementation is simple but the PV array current is discontinuous and would require a large capacitor at the array terminals to smooth the input current. However the use of a large capacitor which is usually electrolytic is not preferred as it is prone to failures [22].

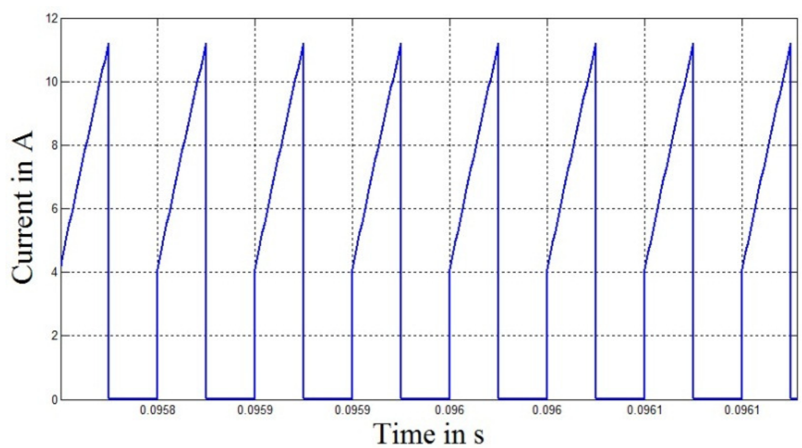

Fig. 7 Input current

Since they only step down the voltage, if the MPPT is to be integrated into the module, Load voltage would necessarily have to be lower than the panel voltage to operate successfully [7] else panels may need to be connected in series so as to achieve a fairly large input voltage. The buck converter thus is able to effectively track the MPP and sweep the IV characteristics of the PV panel in most if not all conditions. Despite these reasons, the buck converter is still used as an MPPT circuit. [4,7].

2.2 BOOST CONVERTER

A typical boost converter circuit shown in fig 7 has an inductor as the input interface. When MPPT converters based on boost topologies are operated in the continuous conduction mode, they draw a smooth current from the PV array which can further be smoothed by using a small capacitor at the array terminals as compared to the buck converter which requires a large capacitor to smooth the array current.

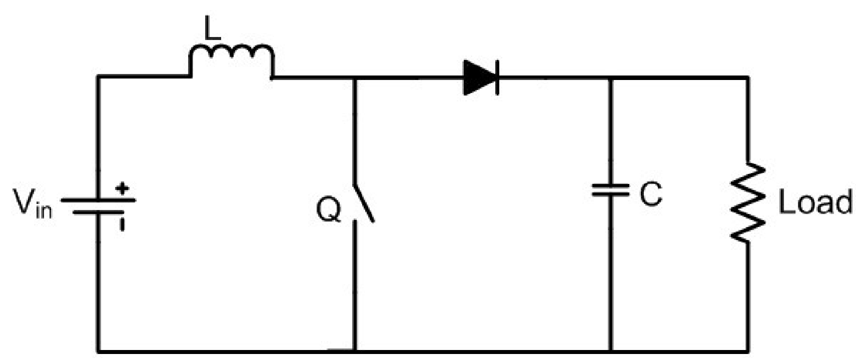

Fig. 8 Boost converter

In steady state the average voltage across the inductor is zero which gives us

$$\left\{\begin{array}{l} V_{in} \times DT = V_o \times (1-D)T \\ V_o = \dfrac{V_{in}}{1-D} \\ I_o = I_{in} \times (1-D) \\ R_{in} = R_o \times (1-D)^2 \end{array}\right. \tag{3}$$

WhereV_{in},I_{in} R_{in} andV_o,I_o R_o are respectively the voltage, current and resistance at the input and output of the converter and 'D' is the duty cycle of the switch Q

As long as the voltage required by the load is larger than the PV array voltage, the boost converter can successfully operate as an MPPT circuit. Since continuous current drawn by the boost converter and it is almost constant in magnitude save for a small switching ripple, it is more efficient at drawing power from the array [8]. The equations of voltage current and resistance for the boost converter are shown in equation 3. The boost converter can only make the load resistance appear smaller than it is at the terminals of the solar array. The current at the input of the boost converter is shown in Fig. 9, Compared to the buck converter input current, that of the boost is smooth and continuous.

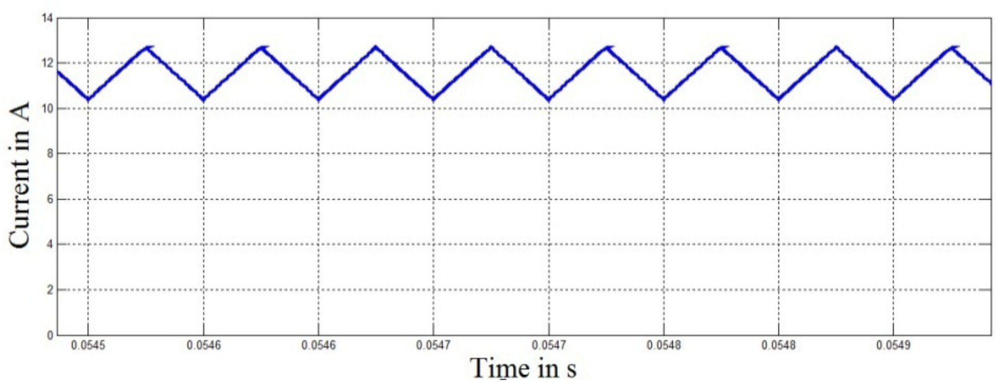

Fig. 9 Boost converter input current

2.3 DERIVED TOPOLOGIES

Buck Boost derived converters are capable of stepping up and down the input voltage and are very suitable for sweeping the entire IV characteristics of the PV array. Like in the boost converter based MPPT, the input is connected to the PV array through an inductor. When operated in the continuous conduction mode, the array current is continuous and almost constant with a small ripple as in the case of the boost converter can be further smoothed. In this case however there is no condition that the load voltage be higher than the array voltage as in the case of the boost converter.

These converters are more complex and require more components to implement. The Cuk and the SEPIC are converter topologies which fit the above description. The output of the Buck boost and Cuk converters is reversed in polarity compared to the input whereas the output and the input of the SEPIC have the same polarity. A typical SEPIC is shown in the fig 10. In continuous conduction mode, the input current is almost constant save for a small ripple current.

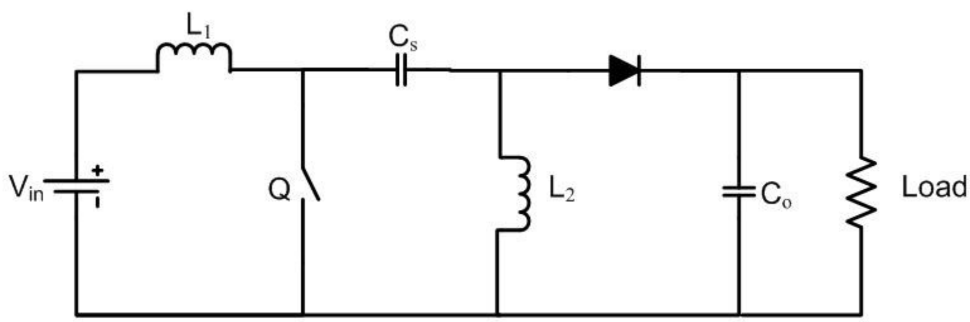

Fig. 10 Basic SEPIC converter

Considering that the SEPIC converter is in continuous conduction mode, the output voltage equation of the SEPIC converter is derived below.

When the switch Q is closed for a shown in fig 10, the input voltage is applied across the inductor L_1. The voltage across the capacitor C_s is applied across the inductor L_2, The diode D acts as an open switch and the capacitor C_o discharges through the load. If the switching frequency is high and the capacitors are large, the voltages across the capacitors C_1 and C_2 can be assumed to be constant. In steady state the voltage across the capacitor Cs is the input voltage V_{in}. Thus when the switch Q is open, the voltage across the inductor L_1 is $-V_o$. Since the effective voltage across an inductor in steady state is zero,

$$\begin{cases} V_{in}(DT) - V_o(1-D)T = 0 \\ V_o = V_{in}\dfrac{D}{(1-D)} \\ I_o = I_{in}\dfrac{(1-D)}{D} \\ R_{in} = R_o\dfrac{(1-D)^2}{D^2} \end{cases} \tag{4}$$

Where V_{in}, I_{in} R_{in} and V_o, I_o R_o are respectively the voltage, current and resistance at the input and output of the converter and 'D' is the duty cycle of the switch Q

The SEPIC shown in fig 10 is a boost topology based converter that is capable of stepping up or stepping down the input voltage and hence is capable of sweeping the entire IV characteristic of the PV array while keeping the voltage polarity at the output same as the input. The input interface is through an inductor and this helps smooth the current from the solar panel. The SEPIC working in the continuous conduction mode also has the advantage of having comparatively lower ripple values than the Buck or the Boost converter [9] and hence requires a relatively smaller filter. Since the voltage can be increased or decreased, the load resistance can be matched to the array impedance in all conditions.

Chapter 3-Interleaving.

Interleaving of DC-DC converters is a well-established concept. It is widely used in power supplies and power factor correction circuits. In interleaved operation of dc dc converters also known as multiphase operation, several identical converters all switching at the same frequency are operated in parallel but with a uniform phase shift between them. This causes the ripple at the input and the output terminals of the converter to have a frequency that is a multiple of the switching frequency of each individual converter times the number of converters. The ripple amplitude is reduced due to the phase shifting effect of the individual cells, the effective increase in frequency and reduction in amplitude is shown in Fig 11 where I is the total input current and I_1 and I_2 are the phase currents for a 2 phase interleaved converter. This results in a reduced filter size when compared to one required for a single converter without interleaving.

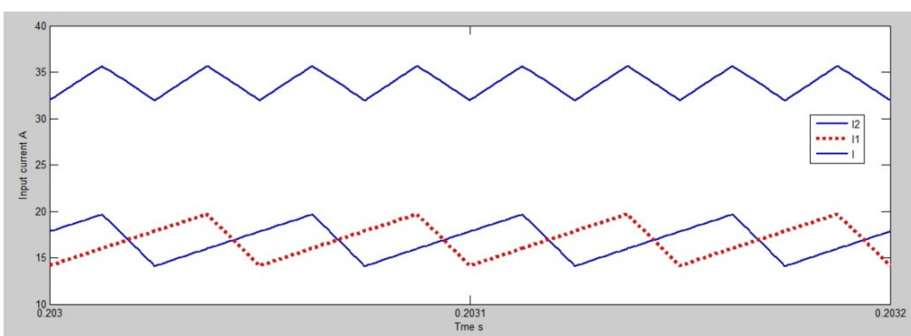

Fig. 11 total Input current and individual phase current

It should however be noted that the duty cycle of the DC-DC converters is a varying parameter, thus the degree of ripple cancellation is also variable. The most optimum cancellation of ripple is a function of the duty cycle of the converter and the number of phases. A method of measuring the variation of the ripple cancellation as duty cycle is varied is by using the factor Fc as shown in equation 5 [1,11,15]. The factor Fc is a ratio of the ripple magnitude of the interleaved converter to the magnitude of the ripple in one individual phase or converter.

$$F_c = \frac{\Delta I}{\Delta I_p} = N \frac{\prod_{i=1}^{i=N-1} \left|\frac{i}{N} - D\right|}{\prod_{i=1}^{i=N-1} \left\{\left|\frac{i}{N} - D\right| + \frac{1}{N}\right\}} \tag{5}$$

Where

$\Delta I =$ The ripple magnitude in the interleaved converter

$\Delta I_p =$ The ripple magnitude in one individual converter

$N =$ The number of individual converters

$D =$ The duty cycle

A plot of the factor F_c versus duty cycle for 2,3 and 4 interleaved converters operating in continuous conduction is shown is shown in fig 11.

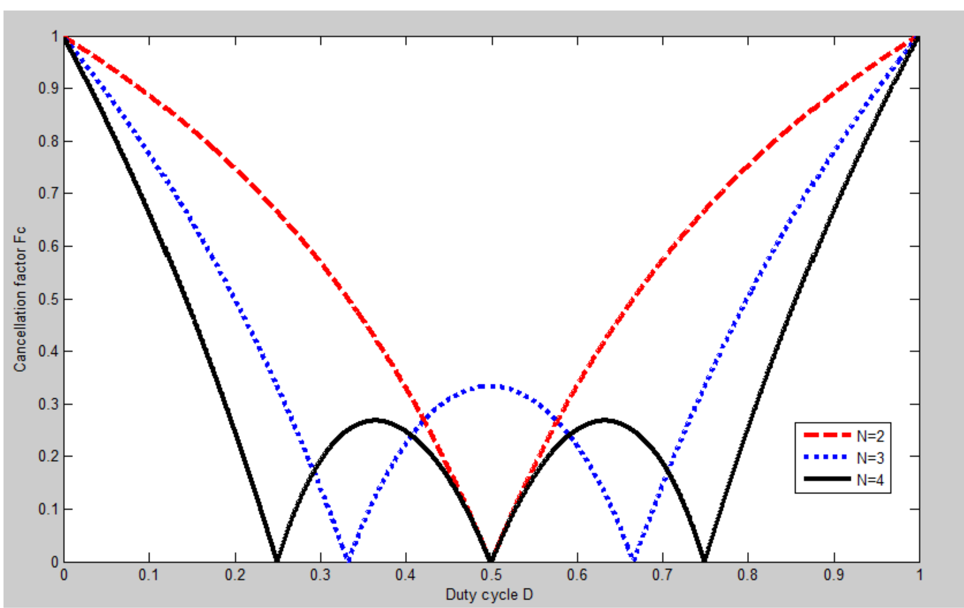

Fig. 12 factor F_c Vs duty cycle

Thus we observe that the factor F_c is not constant but varies and the most cancellation occurs at a duty cycle of 50% for a converter with 2 interleaved phases. The range of duty cycles over which there is a greater amount of ripple cancellation is greater for a converter with greater number of interleaved phases, but this also results in an increase in the number of components and in the complexity of the circuit. It can also be shown that the maximum ripple in case of an interleaved converter is that of one individual phase and the minimum is almost zero and occurs at particular duty cycles depending on the number of interleaved phases as shown in figure 11 [16].

The advantages gained by interleaving converters are mainly due to an increase in the ripple frequency and a reduction in the ripple magnitude and hence a reduction in the size of the filter components, a reduction in the switching frequency of individual phase converters and hence a reduction in the switching losses. It can be viewed as a simple technique to increase the performance of the converter [18]. Interleaving does however cause an increase in the number of components. This increase is most noticeable in the number of inductors but can be accommodated by using coupled inductors in the same phase. This would not only give us the benefit of a saving in volume but also reduce the required inductance and further reduce the ripple [16]. SEPIC described under derived converters in chapter 2 are widely used in interleaved operation in power factor correction circuits and in power supplies. Despite being subjected to higher voltage and current stresses they are preferred over simpler alternatives like the buck or boost converters due to their ability to both increase and decrease the output voltage. An example of an interleaved SEPIC is shown in figure 13.

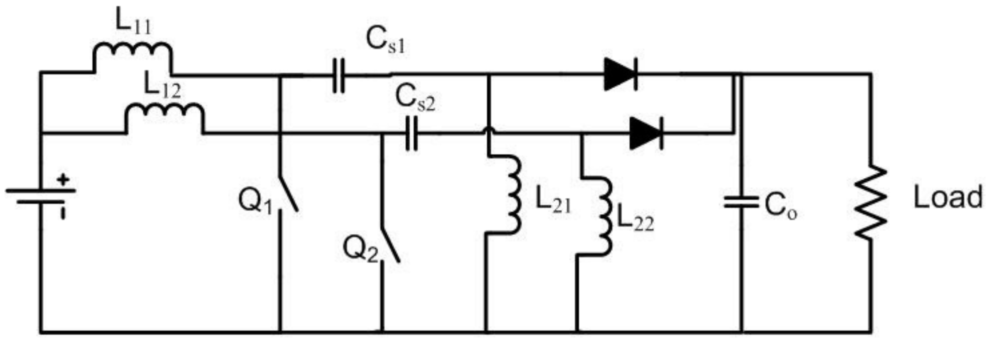

Fig. 13 Interleaved SEPIC with no common output stage

The interleaved SEPIC is usually operated in the discontinuous conduction mode in power factor correction units and in power supplies [25]. However there have been applications of the interleaved SEPIC for photovoltaic applications where they are primarily chosen for the low input ripple current [11]. A plot of the individual phase input current I_1 and that of the effective input current I of an interleaved converter when switching with a duty cycle of 50% for a 2 phase interleaved SEPIC converter is shown in figure 14.

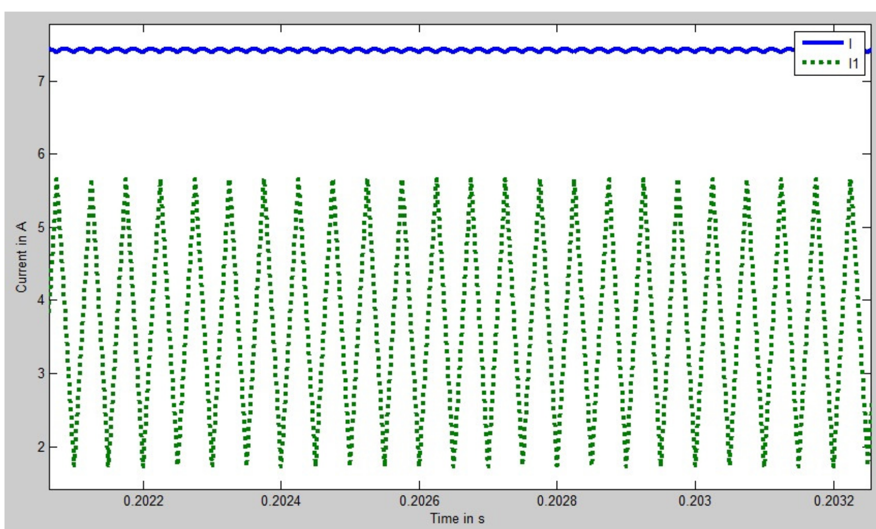

Fig. 14 Interleaved ripple and Phase ripple

Chapter-4 Maximum power point tracking

In chapter 1 the current voltage characteristics of the solar array were described and the array was found to be able to deliver the maximum amount of power only at one point on the characteristic which corresponds to the knee of the curve called as the maximum power point. In order that the DC-DC converter operate at this point, it is necessary to have a control algorithm which operates the switches in the converter so that the load resistance appears to match that of the panel at the maximum power point. There are several methods by which it is possible to ensure that the converter is operating at the maximum power point, two very popular methods perturb and observe and incremental conductance method and the method implemented here the ripple correlation control are discussed below.

4.1 HILL CLIMBING METHOD / PERTURB AND OBSERVE

Two very popular methods of implementing MPPT are by using the hill climbing method. This method reaches the maximum power point by intentionally perturbing the duty cycle of the converter and observing the change in the power. In the figure x if the converter is currently operating to the left of the MPP then on perturbing, the $\frac{dP}{dV} > 0$ hence the duty cycle is so adjusted that the voltage and current of the converter is increased. Similarly if on perturbing, the $\frac{dP}{dV} < 0$ then the duty cycle is so adjusted that the voltage decreases but the current decreases. If the converter is operating at the MPP then $\frac{dP}{dV} = 0$ and the duty cycle is maintained as is. A variation of the hill climbing method uses a variable perturbation step size as opposed to constant perturbation step size to achieve a faster convergence to the MPP. In the perturb and observe method of tracking the MPP, the voltage of the converter is varied by varying the duty cycle and the change in the power is observed. This is similar to the hill climbing method but achieves the variation by changing the voltage. The hill climbing method and the perturb and observe method do not perform very well under rapidly changing conditions [13, 20].

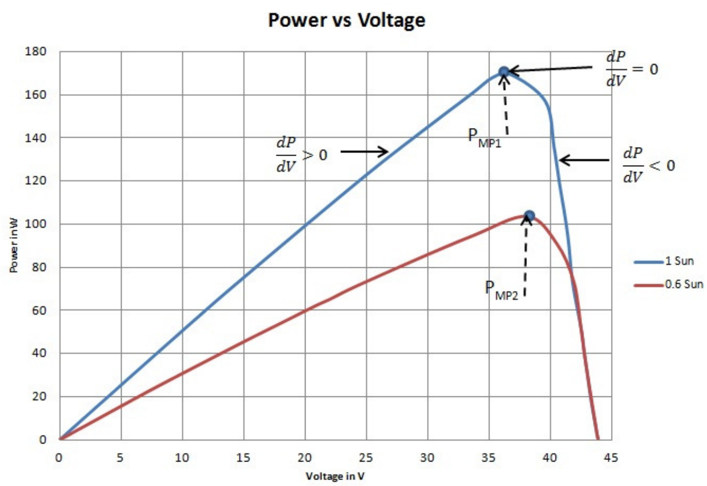

Fig. 15

4.2 INCREMENTAL CONDUCTANCE

The incremental conductance method is based on the fact that at the MPP, the $\frac{dP}{dV} = 0$. From which we have

$$\left\{ \begin{array}{c} \frac{d(I \times V)}{dV} = 0 \\ \frac{d(I \times V)}{dV} = V \times \frac{dI}{dV} + I = 0 \\ \frac{dI}{dV} = -\frac{I}{V} \end{array} \right. \qquad (6)$$

Thus at the maximum power point, the incremental conductance is the same as the instantaneous conductance. As in the case of the hill climbing and perturb and observe methods, the incremental conductance is compared with the instantaneous conductance to zero in on the maximum power point [13].

When the operating point is to the left of the MPP, $\frac{dI}{dV} > -\frac{I}{V}$

and when operating to the right of the MPP, $\frac{dI}{dV} < -\frac{I}{V}$

and when operating at the MPP, $\frac{dI}{dV} = -\frac{I}{V}$

In the tracking methods discussed in the sections 4.1 and 4.2, it is necessary to introduce a perturbation which aids in tracking the maximum power point. A method which does not require the external perturbation but makes use of the inherent switching ripple of the DC-DC converter is discussed in the next section.

4.3 RIPPLE CORRELATION CONTROL.

In ripple correlation control the natural switching ripple in the current and voltage from the panel is used in tracking the maximum power point [12]. This method is based on the correlation that exists between the time derivatives of either panel voltage or current and the time derivative of power. In figure 15

The product $dP/dV > 0$ to the left of the maximum power point

$dP/dV = 0$ At the maximum power point

$dP/dV < 0$ to the right of the maximum power point

Since $dP/dV$is not available from the circuit an alternative approach is used [12]. The product $dP/dV$is multiplied by $(dV/dt)^2$ this gives us$dP/dt \times dV/dt$ which can be obtained from the circuit. Integrating this product with respect to time as in equation (7) gives the duty cycle to operate the converter by pulse width modulation while driving the converter to operate at the maximum power point [12, 14].

$$d = -k \int \frac{dP}{dt} \times \frac{dV}{dt} \tag{7}$$

Where d is the duty cycle of the converter and k is a constant. The negative sign is used because an increase in the duty cycle causes the panel current to increase and since the array current and voltage are inversely related the voltage reduces.

There are various methods by which the ripple correlation control can be implemented. One method used in [14,] uses high pass filters with the cutoff frequency set above the converters operating frequency to obtain the derivatives of panel current and voltage.

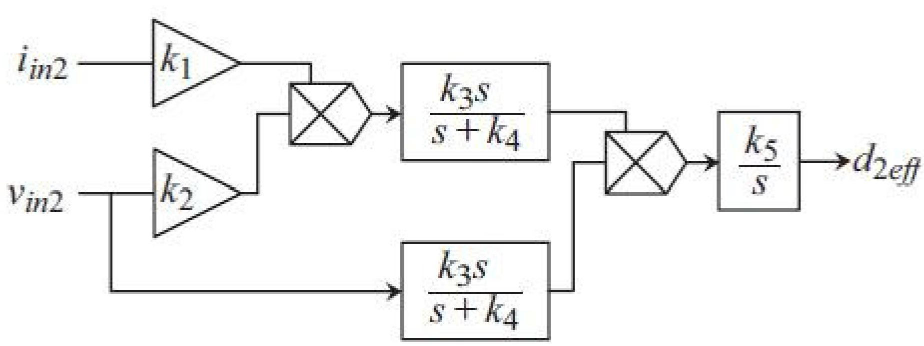

Fig. 16 Ripple correlation control block diagram [14]

Chapter 5-Design and Simulation

5.1 ARRAY MODEL

A circuit based model of the British Petroleum BP3170B, a 170 watt module [3] was built using a four segment piecewise linear approach as described in [17] while neglecting the variation due to temperature. The panel specifications at standard and normal operating conditions are given in table 1

BP3170B	STC (1000w/ m^2)	NOTC(800w/ m^2)
Maximum power P_{max}	170W	122.4W
Voltage at P_{max}	35.6V	31.7V
Current at P_{max}	4.8A	3.84A
Short circuit current I_{sc}	5.2A	4.21A
Open circuit voltage V_{oc}	43.6V	39.7V

Table 1 Solar array BP3170B specifications

The model was constructed for the parameters corresponding to those at an incident radiation of 1000w/m^2 at standard conditions. The circuit based model is as shown in figure 17 and the I-V characteristics of the model are as shown in fig 1. The values of the circuit parameters were solved for and found to be

V_t = 3.17V
V_m = 13.4V
V_b = 26.95V
R_t = 4.04Ω
R_m = 38.11Ω
R_{sh} = 436Ω
R_s = 1Ω

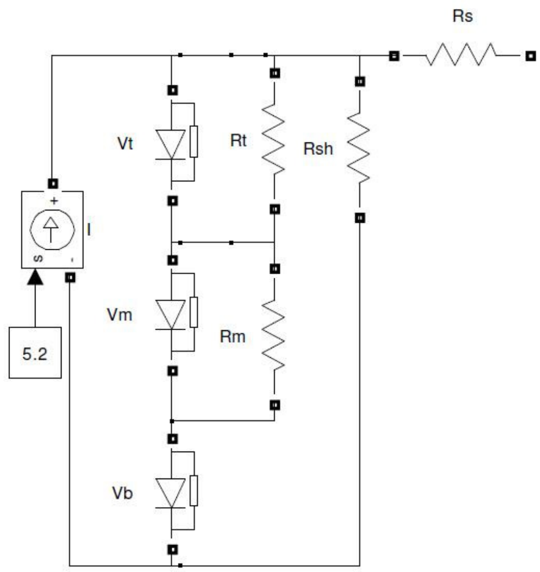

Fig. 17 Circuit based model of PV array

5.2 INTERLEAVED SEPIC MODEL WITHOUT COMMON OUTPUT STAGE

The SEPIC for the MPPT circuit was designed such that at 50% duty cycle it is operating at the maximum power point at standard conditions. The 50% duty cycle condition is so chosen so that the ripple cancellation is maximum at the maximum power point corresponding to conditions at standard temperature and a radiation intensity of 1000 w/m^2. It is very likely that the panel will operate at another power point or that the characteristics change due to the addition of other panels or that aging will change the characteristics and so will the load, so it is to be noted that the 50% condition is just used as a reference to illustrate the effect of ripple cancellation. Under these conditions, assuming that the converter is 100% efficient the input voltage is the same as the output voltage and the input current is the same as the output current. The switching frequency f_s was chosen to be 25Khz.

and. $V_{in} = V_{out} = 35.6V$ and

$I_{in} = I_{out} = 4.8A$

Referring to the figure 13, If the input current ripple ΔI in inductor L_1 is allowed to be 1A, then

$$\Delta I = \frac{V_{in}}{L \times f_s} \tag{8}$$

which gives us

$$L = \frac{V_{in}}{\Delta I \times f_s} \tag{9}$$

Where V_{in} is the voltage corresponding to the maximum power point, this gives us the value of the inductor L_1 as 1.424mH.

If the voltage ripple across the series capacitor C_s is allowed to be 1V, then

$$\Delta V_{c1} = \frac{I_{out}}{C_s \times f_s} \tag{10}$$

Which gives us Cs= 192µF

Similarly if the output voltage ripple is allowed to be 1V, then

$$\Delta V_{co} = \frac{I_{out}}{C_o \times f_s} \tag{11}$$

Which gives us Co= 192 µF

For the converter to remain in continuous conduction,

$$L_1, L_2 > \frac{V_{in}}{2 \times I_{out} \times f_s} \tag{12}$$

This gives us L_1, L2>148.4µH, but the inductance required to keep the current ripple within bounds exceeds this value and so can be neglected. The value of the inductance L_2 was chosen to be 424 µH.

Using this design for the SEPIC, two identical designs are operated in interleaved fashion and are compared for their effectiveness in reducing the ripple content at the array terminals as compared to a single SEPIC working alone.

The figure 18 shows the ratio of the ripple in the interleaved SEPIC to that in a lone SEPIC and how the ratio changes with the duty cycle. The ripple magnitude in the interleaved SEPIC is almost zero at a duty cycle of 50% and is in good agreement with that predicted as per figure

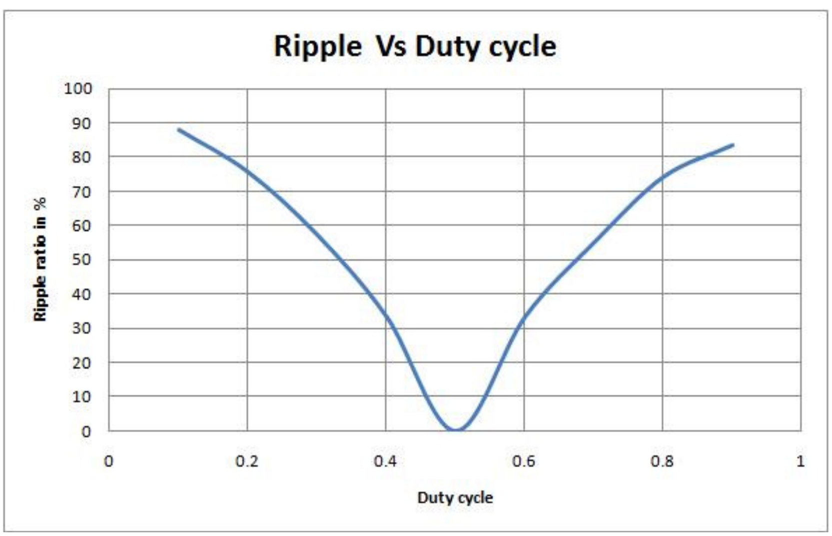

Fig. 18 Ripple ratio Vs duty cycle

5.3 INTERLEAVED SEPIC MODEL WITH COMMON OUTPUT STAGE

In the above design of the SEPIC, we make use of an identical set of components which act as the second phase. Is is however possible to use come of the components in common so that the component count can be reduced. This results in a circuit somewhat similar to a multiple input SEPIC described in [26], The figure 19 shows a multiple input SEPIC.

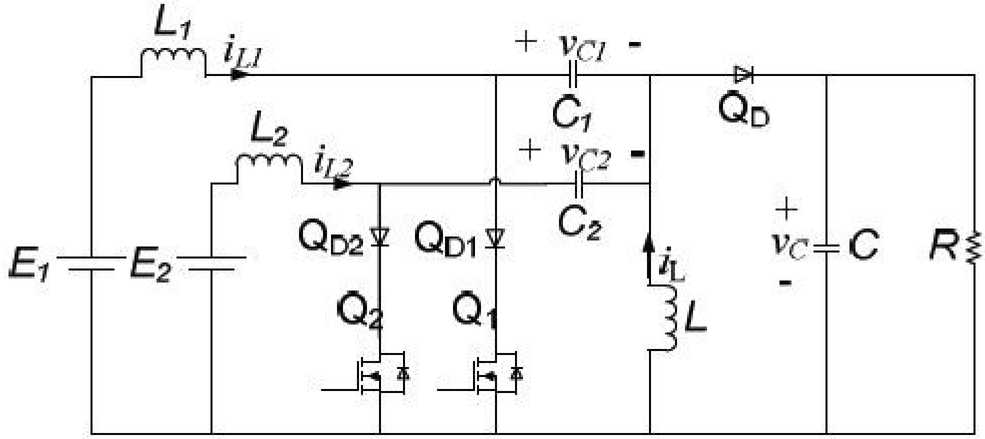

Fig. 19 Double input SEPIC [26]

In the double input SEPIC in figure 19, the two input voltages are different which would cause the voltages across the capacitors C1 and C2 to be different, and when the switches Q1 and Q2 close it would result in connecting two capacitors at different voltages in parallel resulting in a short circuit. Hence the two blocking diodes QD1 and QD2 which effectively make the switches forward conducting and bidirectional blocking. The output voltage equation for the double input SEPIC is given by equation 13 [26].

$$V_o = \frac{E_1 \times D_1 + E_2 \times D_{2eff}}{(1 - D_2)} \tag{13}$$

Where E_1 and E_2 are the two input voltages and D_1 and D_2 are the duty cycles of the two switches Q1 and Q2. Referring to figure 19, If $E_1 > E_2$ and $D_2 > D_1$, It is evident that the voltage across capacitor C1 being greater than that across capacitor C2 will not let the switch Q2 conduct even if it has a gate input. Thus the switch Q2 will only conduct for that portion of its duty cycle when the switch Q1 is off. Hence the use of D_{2eff} which is defined as that portion of the duty cycle D_2 of switch Q2 during which it conducts given by the equation 14

$$D_{2eff} = D_2 - D_1 \tag{14}$$

In the operation of the interleaved converter, the switches are operated out of phase and the duty cycles are the same and so, which limits the maximum duty cycle to 50%.

$$D_{2eff} = D_2 = D_1 \tag{15}$$

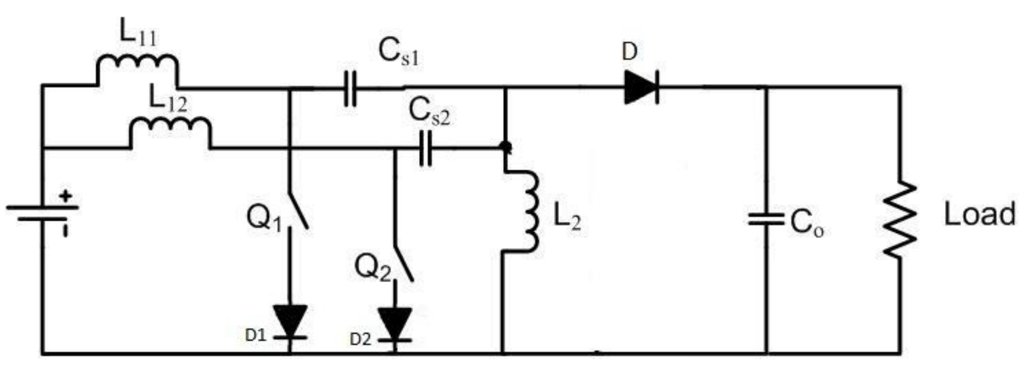

Fig. 20 Multiple input SEPIC used in interleaving

The figure 20 shows the multiple input SEPIC used in interleaving operation. Operating the multiple input SEPIC in interleaved fashion causes the ripple cancellation effect of the interleaved SEPIC discussed in section 5.2 to cease to exist. Instead each of the phases has an input current that has ripple at twice the switching frequency of each phase. The current drawn from the source while having switching ripple at twice the switching frequency also has about twice the ripple magnitude of that in each phase. Figure 21 shows the current I from the source and I1 and I2 in each phase of the above converter. All of the waves are in phase but are at twice the switching frequency. The waves were generated for a duty cycle of 24.7%.

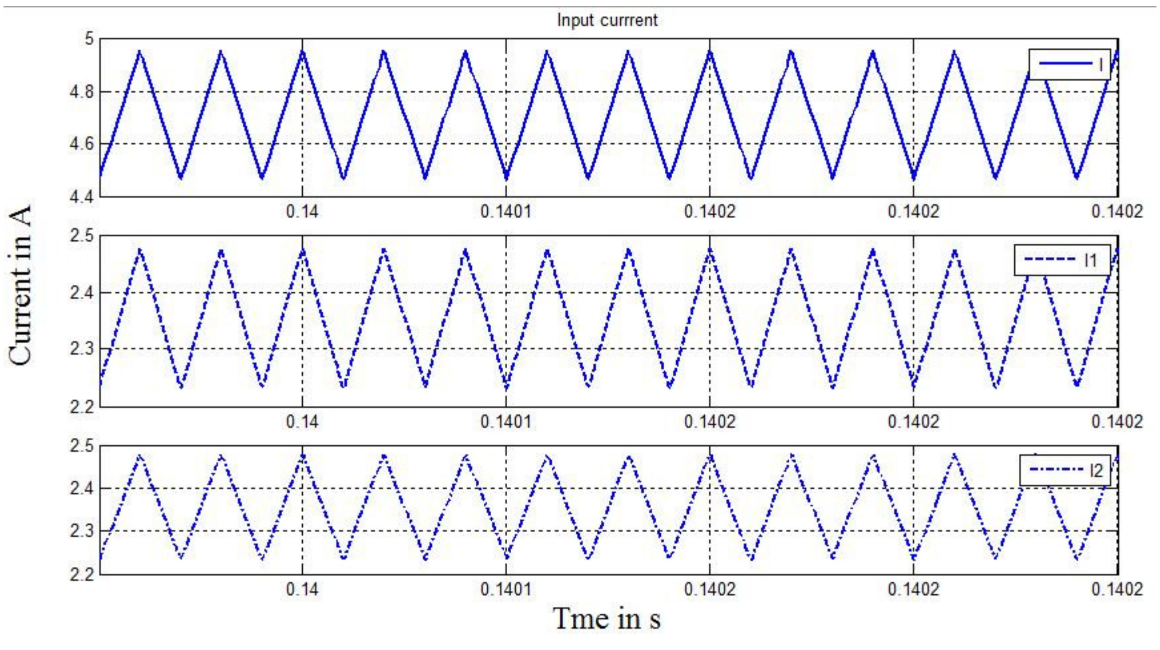

Fig. 21

The double frequency ripple in individual phases despite the switches operating at the designed frequency is explained as follows. Considering phase 1 in figure 20, when the gate signal Vg1 to switch Q1 is high, current I1 in inductor L11 increases as shown in figure 22, and the Cs1 discharges into inductor L2 through the switch Q1 causing current

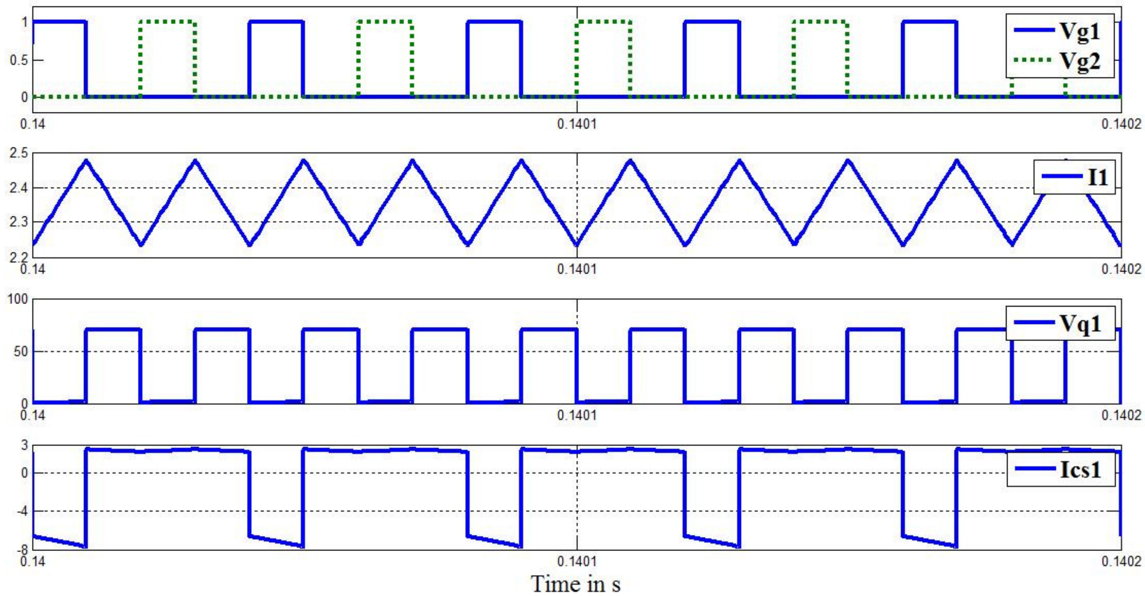

Fig. 22 Voltage and current waveforms for interleaved SEPIC with common output stage.

Ics1as shown in figure 22. When Vg1 goes low, the switch Q1 opens and the voltage across it goes high and the current I1 through inductor I decreases in the process charging the capacitor Cs1. As this is happening, Vg2 goes high causing switch Q2 to conduct, this causes the voltage across the switch Q1 to go down to almost zero causing the inductor current to increase again as shown in figure 22. The switch Q1 being off does not conduct and so the current flows through the capacitor Cs1 thus the current Ics1 charges the capacitor causing Vcs1 to increase. A similar process causes the double frequency current to flow in the second phase as well. Thus the two currents are always in phase due to the double frequency effect thereby the ripple cancellation cannot take place. But the ripple frequency does increase and there would still be a reduction in the size of the filter components.

5.4 MPPT WITH RIPPLE CORRELATION CONTROL

In the interleaved converter, each phase is operating at a frequency of 25Khz But the ripple frequency at the array terminals is 50Khz, thus to find the time derivatives of the array current and voltage, high pass filters with a cutoff frequency of 52.5Khz was used. The ripple correlation control was applied to both the interleaved SEPIC topologies. The components designed for the SEPIC in the first topology were used in the simulation of the second topology as well thereby giving a basis for comparison. The results of the simulation using the ripple correlation control are presented below.

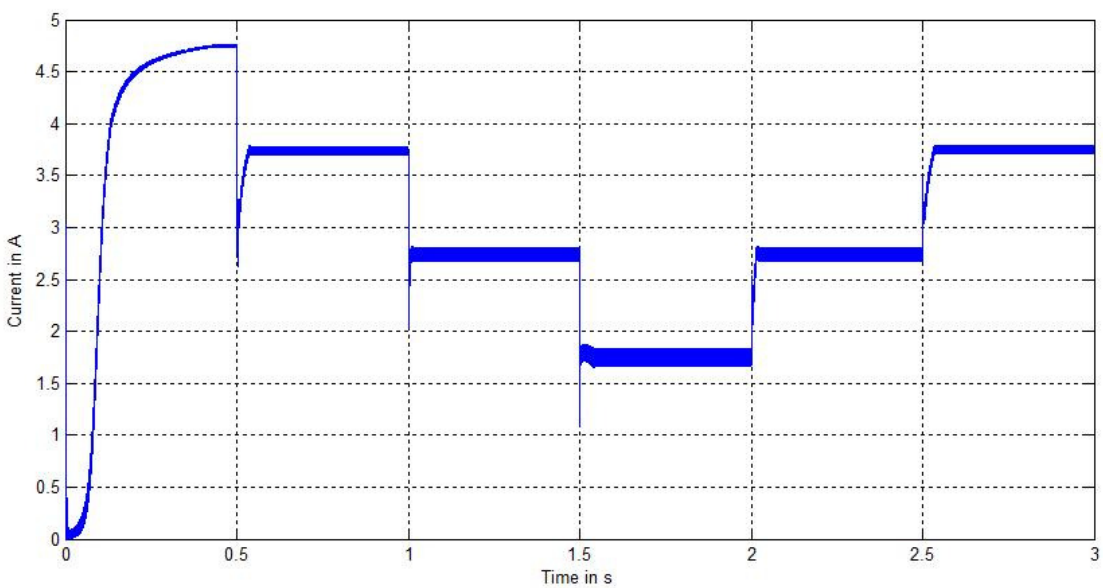

Fig. 23 Panel current Vs time for varying irradiance SEPIC topology 1

For the interleaved SEPIC without a common output stage the time to reach the maximum power point is different for different levels of irradiation this is because the circuit was designed so as to have maximum ripple cancellation corresponding to the maximum power point under standard conditions. Maximum ripple cancellation happens at a duty cycle of 50% as per design and the smaller the ripple the longer is the time taken to converge as per fig 6 of [12]. This is further evidenced by the relatively short times in which the maximum power point is reached when not under standard conditions as in these cases the duty cycle that the converter is operating at is not 50%. The variation in duty cycle of the converter to follow the maximum power point is shown in figure 23. It is to be noted that the further away from the 50% mark that the duty cycle is, the faster is the tracking of the maximum power point as the ripple magnitude is larger there.

For the interleaved SEPIC using a common output stage, there is no effective ripple cancellation but there is a reduced ripple due to the increased frequency. The figure 24 shows the panel current when the second SEPIC topology is used for tracking the maximum power point.

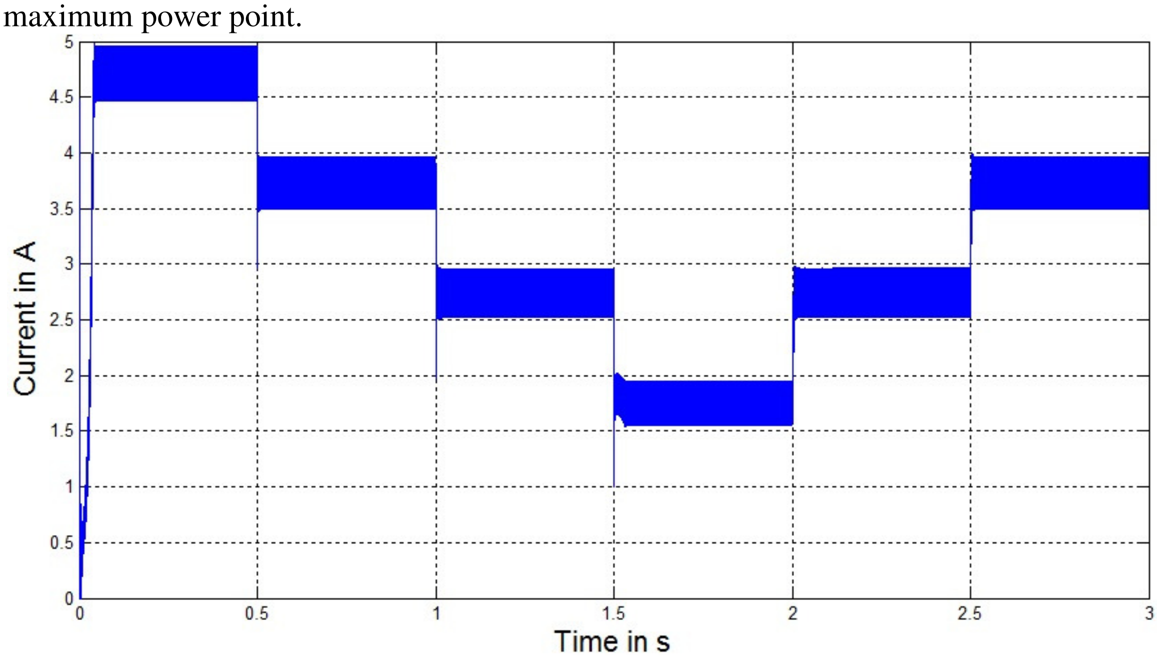

Fig. 24 Panel current Vs time for varying irradiance SEPIC topology 2

In figure 24, the ripple in the panel current is larger than that in figure 23. This is because the currents in the 2 phases are in phase leading to the increase in the ripple magnitude in the panel current as it is the sum of both currents as shown in figure 21. It is however clearly much faster in reaching the maximum power point when compared to the first topology of the SEPIC. The tracking times of the two topologies for a step change in insolation is shown in figure 25.

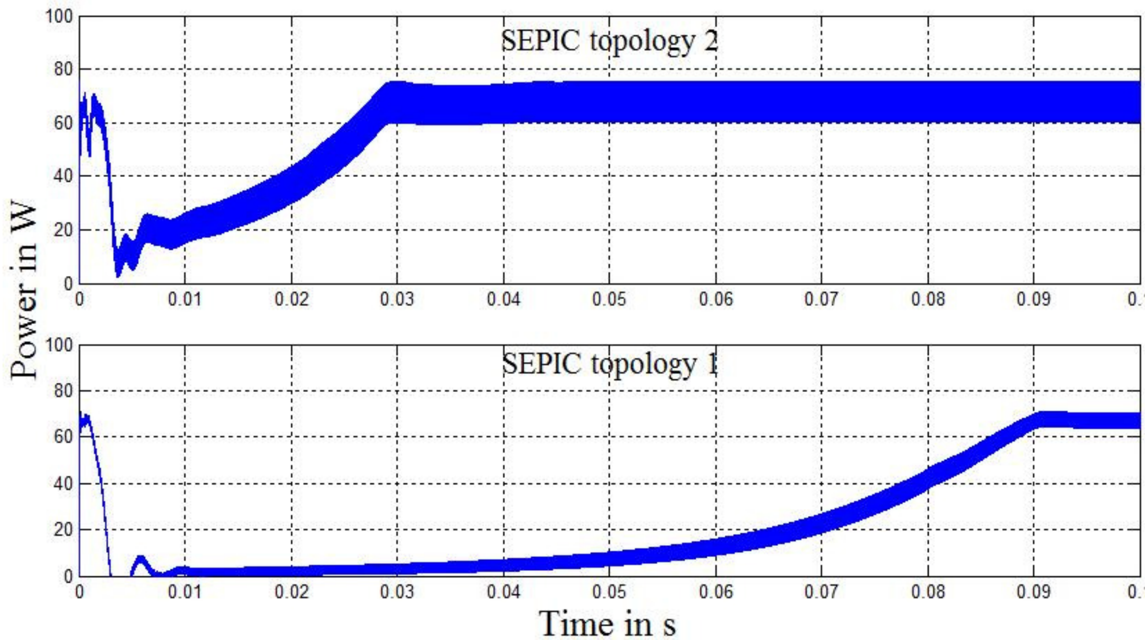

Fig. 25 Power Vs time for tracking the maximum power point

The efficiency of tracking of the system defined as

$$efficiency = \frac{p_{tracking}}{P_{maximum}} \tag{13}$$

Where $P_{tracking}$ is the power that the maximum power point tracking circuit is operating at and $P_{maximum}$ is the power at the maximum power point for that level of insolation for four different conditions of insolation are tabulated in table 2. The effect of changing insolation was simulated by using different values of short circuit current in the circuit model of the solar array in figure 16.

I_{sc} in A	P_{max} in w	$P_{tracking}$ in w Ist topology	% efficiency	$P_{tracking}$ in w 2nd topology	% efficiency
5.2	170.8	170.7	99.94	169.7	99.35
4.2	138.6	138.25	99.74	137.55	99.24
3.2	104.6	103.75	99.18	103.59	99.04
2.2	68	67.73	99.6	67.85	99.78

Table 2 Tracking efficiency variation.

The tracking efficiency of the second topology is slightly lower than that of the first topology but is more than made up for in the relatively shorter time in which it reaches the maximum power point and also in the component count.

Chapter 6-Conclusion

The use of an interleaved SEPIC for maximum power point tracking of a solar panel using ripple correlation control was explored. The SEPIC was implemented using two different topologies. The requirements of low input current ripple and high efficiency of tracking with short time to reach the maximum power point were satisfied by the combination of the control circuit and the topologies to different extents. The requirements of the filtering components were reduced due to an increase in the switching frequency combined with the ripple cancellation due to interleaving in the first topology. But due to the low value of the ripple the time to reach the maximum power point was larger.

In the second topology the ripple frequency was twice the switching frequency and the magnitude of the ripple was larger as there was no ripple cancellation but the maximum power point was reached in a much shorter time. The efficiencies of tracking were compared, The time for the converters to reach the maximum power points under different conditions of insolation was observed. The time to converge when there was least ripple in the circuit input current was found to me the longest in the first topology. The second topology exhibited relatively quick tracking due to the larger magnitude of the ripple. The long tracking time in the first topology is not a very desirable property and thus the use of the current ripple in one of the phases of the converter as opposed to using the input current of the interleaved converter may be a possible solution. In the second topology the ripple cancellation did not exist at all but there was an effective increase in the ripple frequency but had the advantage of a reduced component count. Thus a tradeoff exists in the topologies studied with respect to time to reach the maximum power point and the ripple in the input current and a smaller component count.

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Vita

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