A Direct Digital Frequency Synthesizer with Single-Stage Delta-Sigma Interpolator and Current-Steering DAC

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Abstract

This paper presents a direct digital frequency synthesizer (DDFS) with a 16-bit accumulator, a 4th-order single-stage pipelined delta-sigma interpolator and a 300MS/s 12-bit current-steering DAC based on Q^2 Random Walk switching scheme. The delta-sigma interpolator is used to reduce the phase truncation error and the ROM size. The measured spurious-free dynamic range (SFDR) is greater than 80 dB for 8-bit phase value and 12-bit sine-amplitude output. The DDFS prototype is fabricated in a 0.35um CMOS technology with core area of 1.11mm^2.

Key Words: DDFS, delta-sigma interpolator, CMOS, DAC, Q^2 Random Walk

Introduction

For many application, direct digital frequency synthesis (DDFS) provide distinct advantages over the traditional frequency-agile phase-locked loop (PLL) based synthesizer, including fast settling time, sub-hertz frequency and sub-degree phase resolutions, continuous-phase switching response, and good spectral purity [1]. Unlike PLL based synthesizer, DDFS is compatible with digital CMOS ICs and is often embedded in the baseband ASIC of a transceiver system. As shown in Fig. 1, a conventional DDS includes a digital accumulator that generates the phase word based on the input frequency word *W*. The DDS utilizes a look-up table to convert the phase word to a sinusoidal amplitude word, whose width is normally limited by the finite number of input bits of the digital-to-analog converter (DAC). Deglitch filters are added after the DAC to remove the spurious components generated in the data conversion process.

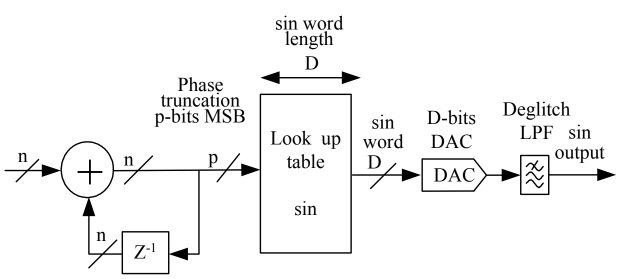

Fig. 1 Conventional DDS

According to Fig. 1, an ideal DDS output can be expressed as

$$A_{out} = A\sin\left(\frac{2\pi Wt}{2^n T_{clk}}\right) = A\sin\left(\frac{2\pi Wi}{2^n}\right) \quad (1)$$

where A is the full-scale output magnitude of the DAC and the time variable $t=T_{clk}i$. While a pure sinusoidal waveform is desired at the DDFS output, spurious tones can also occur mainly due to the following processes:

(i) The synthesizer step is defined as $f_{clk}/2^n$. Fine resolution can thus be achieves using large accumulator size, i.e. n=32. However, the large accumulator requires a huge look-up with 2^n addresses. Look-up table normally takes the majority of the DDFS area. In order to reduce the look-up table ROM size, the phase word is normally truncation process introduces quantization noise, which can be modeled as a linear addictive noise to the phase of the sinusoidal wave. It can be phase truncation is given by $SNR_p=6.02p-3.992$dB, where p is the number of phase bits.

(ii) The ROM word width is normally limited by the finite number of bits of the available DAC. Similarly, the SNR due to finite width of amplitude word is given by $SNR_A=6.02D+1.76$dB, where D is the number of DAC bits. In practical designs, $p=D+1$ should be chosen to ensure that the DDFS output noise is dominate by the ROM word width, namely by the finite number of DAC bits.

To reduce the quantization noise associated with the phase word truncation, delta-sigma techniques have been applied to different locations in a DDFS [2-3]. A complicated 2nd-order delta-sigma modulator, in addition to the phase accumulator, is used in [2] to produce a theoretical SFDR of 110dB without DAC. A simple delay unit is used in [3] to generate the first-order delta-sigma shaping effect. Insufficient noise shaping is shown at its output spectrum. The DDFS in [2] did not implement the DAC and the work in [3] was not verified in hardware at all. None of delta-sigma DDFS techniques reported so far includes high-order delta-sigma interpolator and thus has only a limited noise shaping effect. High-order delta-sigma is needed to achieve large SFDR, fine resolution and small look-up table. This paper presents a novel DDFS architecture using a high-order single-stage delta-sigma interpolator to remove phase truncation error. We also implemented a 300MS/s 12-bit current-steering DAC with a novel Q^2 Random Walk switching scheme.

High-order delta-sigma Interpolator

A. Phase Truncation Error Reduction

Considering the quantization errors due to phase truncation e_p, and amplitude truncation e_A, and assuming the phase quantization error is small relative to the phase, the resulting DDFS output can be expressed as

$$A_{out} = A\sin\left(\frac{2\pi Wi}{2^n} + e_p(i)\right) + Ae_A(i)$$
$$\approx A\sin\left(\frac{2\pi Wi}{2^n}\right) + Ae_p(i)\cos\left(\frac{2\pi Wi}{2^n}\right) + Ae_A(i) \qquad (2)$$

Thus, the phase error is amplitude modulated on the quadrature signal with respect to the desired signal output. Equation (2) provides a simple model for the prior art DDFS output and its associated quantization errors.

To avoid aliasing during data conversion, the synthesized frequency is required to be smaller than the DDFS clock frequency. Thus, oversampling is required in DDFS, allowing noise-shaping techniques to be used to shift the phase quantization error to a higher frequency band, where the noise can eventually be removed by the deglitch filter behind the DAC. As shown in Fig. 2, a k*th*-order delta-sigma noise shaper with a high-pass transfer function $(1-Z^{-1})^k-1$ is added behind the phase truncation. The resulting DDFS output can be expressed as

$$A_{out} = A\sin\left(\frac{2\pi Wi}{2^n} + e_p(i)(1-z^{-1})^k\right) + Ae_A(i)$$
$$\approx A\sin\left(\frac{2\pi Wi}{2^n}\right) + Ae_p(i)(1-z^{-1})^k\cos\left(\frac{2\pi Wi}{2^n}\right) + Ae_A(i) \qquad (3)$$

It can be seen that the phase error e_p is high-pass filtered by the delta-sigma interpolator before the amplitude modulation via the look-up table. This process greatly reduces the close-in phase noise and de-correlates the phase truncation error. The high-pass shaped quantization error is eventually removed by deglitch low pass filters. Thus, the spurious components due to phase truncation are greatly reduced or eliminated at the DDFS output.

B. Implement of Pipelined delta-sigma Interpolator

In fractional-N frequency synthesis, a delta-sigma noise shaper is employed to randomize the fractional spurious components and to shift the spurs to a higher frequency band, where they can then be filtered out by PLL filter [4-6].

Two types of delta-sigma modulators have been used in fractional-N frequency synthesis. One has a single-loop modulator [5], and another has cascaded accumulators called MASH [4]. The single-loop modulator can have a single-bit or multi-bit output depending on the desired quantization noise floor. The multi-loop MASH architecture normally has a single-bit output per accumulator and the order of the MASH delta-sigma interpolator is equal to the number of accumulators. For DDFS applications, the number of phase bits at output of the delta-sigma interpolator is determined by the affordable ROM size and the system SFDR requirement. It is obviously inconvenient to use multi-loop delta-sigma topology in DDFS. We propose a novel single-loop high-order delta-sigma architecture, which can provide multi-bit output for various phase truncation requirements. The circuit is absolutely stable and gains advantage of superior close-in noise shaping capability.

To achieve fine resolution of the synthesizer, a large size of accumulator is required. To reduce the look-up table size, many of the accumulator output bits need to be truncated. High-order delta-sigma is thus needed to remove the phase truncation error such that a large SFDR and a fine resolution can be achieved. For high-speed application, the single-loop delta-sigma interpolator can be implemented in a pipelined format. Fig. 3 illustrates the pipelined single stage 4*th*-order delta-sigma interpolators. The architecture implements the noise shaping high-pass transfer function of $(1-Z^{-1})^4-1$ for the truncated (n+1-p) LSB bits, which is labeled with "A" in the figures. The output phase word of the p MSB bits is used as the look-up table address. To avoid using multipliers, which can be the area and speed bottlenecks, we manipulate the function such that only shifting operations are involved, In Fig. 3, notation "<<" means left shift. Thus, "<<2" represents left shift by 2 bits, namely, multiplying by 4. The presented pipelined 4*th*-order delta-sigma interpolator with 16 input bits and 8 truncated phase bits. The presented high-order single-loop delta-sigma topology can also be used in delta-sigma fractional-N synthesizers to achieve ultra-fine resolution and low phase noise.

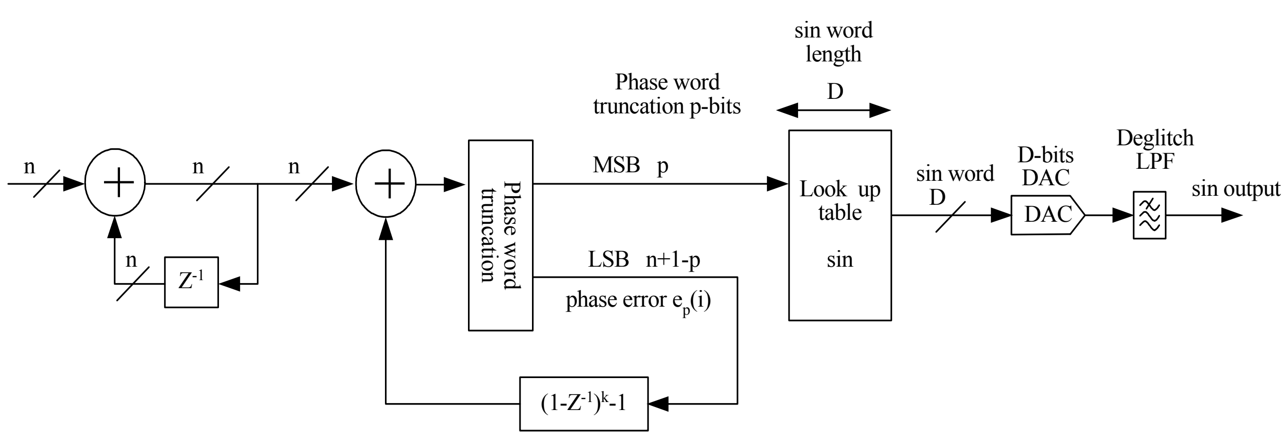

Fig. 2 Proposed DDFS using a k*th*-order delta-sigma noise shaper to shape the phase truncation error

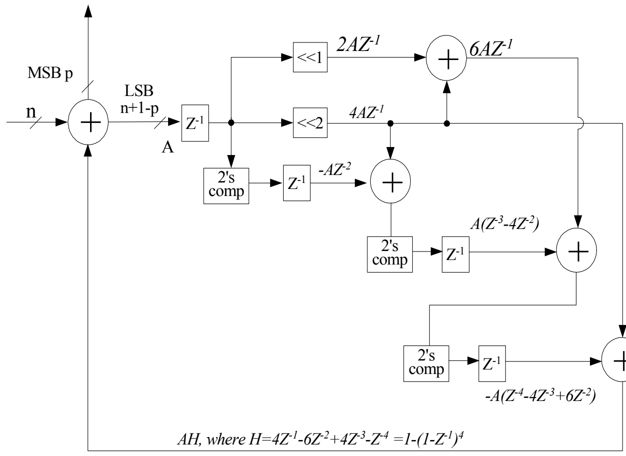

Fig. 3 A 4*th* order single-stage delta-sigma interpolator.

The proposed DDFS architecture using the 4*th*-order delta-sigma interpolator was simulated in MATLAB. The 4*th*-order delta-sigma interpolator has a 60dB/dec high-pass noise shaping slope without the DAC. The noise shaping slope after the DAC becomes 40dB/dec for a 4*th*-order delta-sigma interpolator due to the additional pole added by the DAC. In order to model the DAC nonlinearity, the INL of the DAC is assumed to be 1LSB and the equivalent output electronic noise (Gaussian noise) is assumed to be 15(dB). Note that Noise (dB) =10*log(Pn/Pq), where Pq=(LSB)^2/12, and Pn is the noise power. Fig. 4 shows the DDFS output spectrum after the DAC that employs a 4*th*-order delta-sigma interpolator for phase truncation. Fig. 4 demonstrates that the high-pass noise shaping effect of the DDFS with a 4*th*-order delta-sigma interpolator with 40dB/dec noise shaping slope. Due to DAC's sample and hold effect (sin function), the two sides of the delta-sigma noise shaping curve are not symmetric.

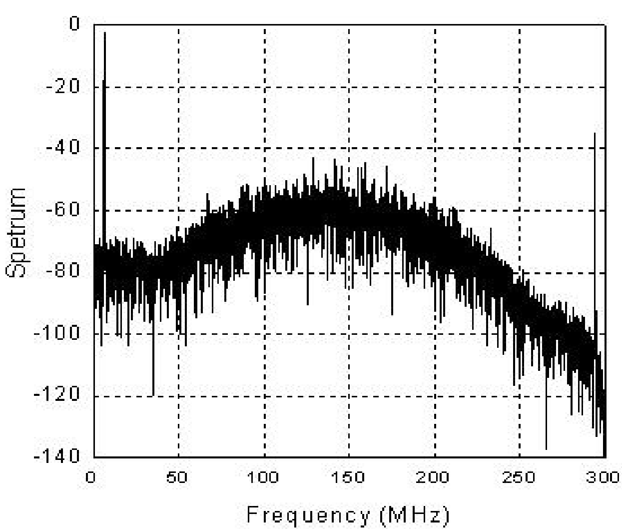

Fig. 4 Simulated DDFS output spectrum with a 4*th*-order delta-sigma interpolator.

12-bit Current Steering DAC

The on-chip 12-bit DAC is implemented by using the 8/4 segmented current-steering architecture. The 8 MSBs of the digital binary inputs are thermometer-decoded to control 255 current sources, each having 16-LSB current weighting, while the remaining 4LSBs controls 4 binary-weighted current sources. The output currents of all current sources, which are switched ON and OFF according to the digital input codes, are summed and driven into any resistive load in order to generate the required analog output voltage. The DAC comprises current cell matrix, current switch matrix, decode circuit and a bias generator as shown Fig. 5.

In the current cell matrix, it is difficult to make current sources identical due to layout mismatches, output impedance of the current source and switch, edge effects, voltage drops in the supply lines, thermal gradients, doping gradient and oxide thickness. The nonlinear secondary effects cause graded, symmetrical, and random errors, resulting in the reduced linearity of DAC's. The proposed DAC employs a novel switching scheme to minimize the degradation of integral linearity caused by mismatches of current sources. This switching scheme will be referred to as quad quadrant (Q^2), as four (quad) units in every quadrant altogether compose one current source [7]. In double central symmetric current matrix, the Q^2 Random Walk scheme is adopted to improve the nonlinearity due to symmetrical error and the two-dimensional graded error of the DAC. The proposed DAC employs extra digital latches just in front of the unit current cells to synchronize the digital inputs as well as employs the cascaded current sources to minimize the current variation effect. This is to overcome the skew between the row and column select signals in the local decoder.

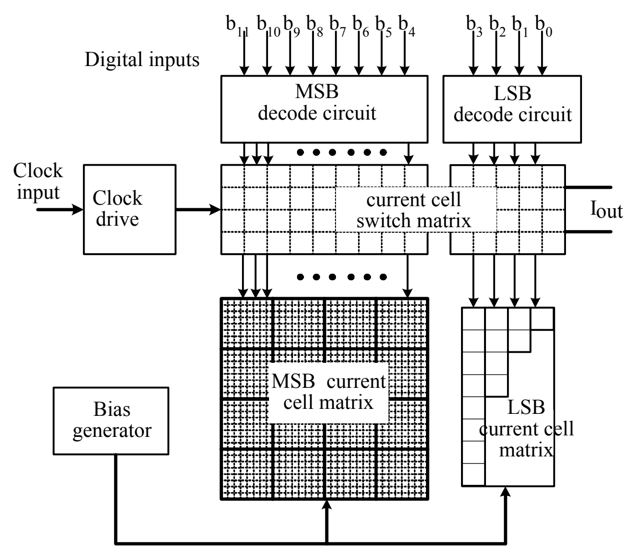

Fig. 5 Simplified DAC architecture with current steering matrix.

Experimental Result

The prototype DDFS IC was fabricated in 0.35μm CMOS technology with 2-poly and 4-metal layers. A 16-bit accumulator is used and its 8-MSBs are truncated for addressing the look-up ROM. The phase truncation reduces the ROM size to 1/256. To demonstrate the delta-sigma effect, a 12-bit DAC is integrated. Thus, the DDFS output quantization noise is dominated by the phase truncation error.

Fig. 6 gives the measured DDFS output spectrum after a 5*th*-order Butterworth LPF with corner frequency at 5KHz. The measured SFDR is 82dBc with synthesized frequency at $W{\cdot}f_{clk}/2^{16}=15\times20/2^{16}$ *MHz =4.578KHz* and clock frequency at 20MHz. Fig. 7 demonstrates that the noise shaping slope of 40dB/dec due to a pole introduced by the DAC. The measured DDFS output spectrum agrees well with the simulated spectrum shown in Fig.3. The delta-sigma noise shaper moves close-in phase truncation spurious components to a higher frequency band up to half of the clock frequency, where they can be easily removed by the LPF. Due to DAC's sampling and hold effect, attenuation occurs at $f>0.5f_{clk}$, which causes two sides of noise shaping curve unsymmetrical. Fig.8 shows the die photo of the fabricated DDFS prototype chip with die area of 2.2×1.9mm^2, in which the accumulator and delta-sigma interpolator occupies 0.2×0.3mm^2, the sin ROM occupies 0.3×0.3mm^2 and the DAC occupies 1.9×0.5mm^2. Total power consumption of the entire chip operating at 300MHz clock frequency is less than 200mW with a 3.3V power supply.

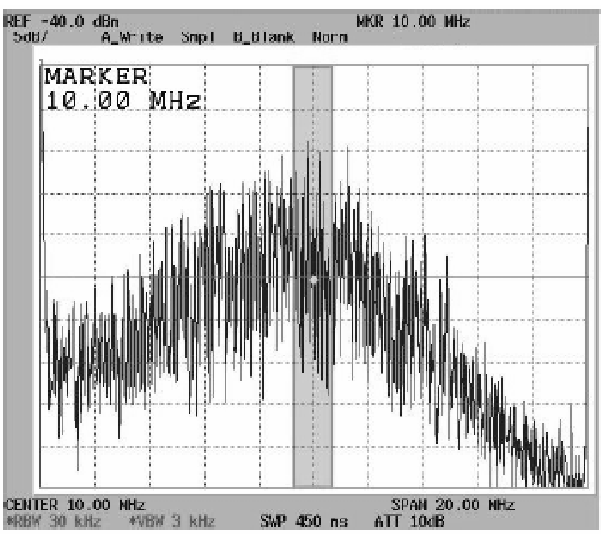

Fig.6. Measured DDFS output spectrum after the DAC and before the deglitch filter.

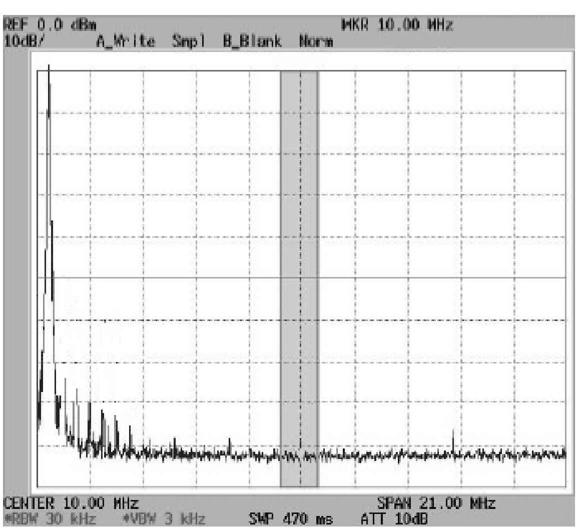

Fig. 7. Measured DDFS output spectrum after the deglitch filter

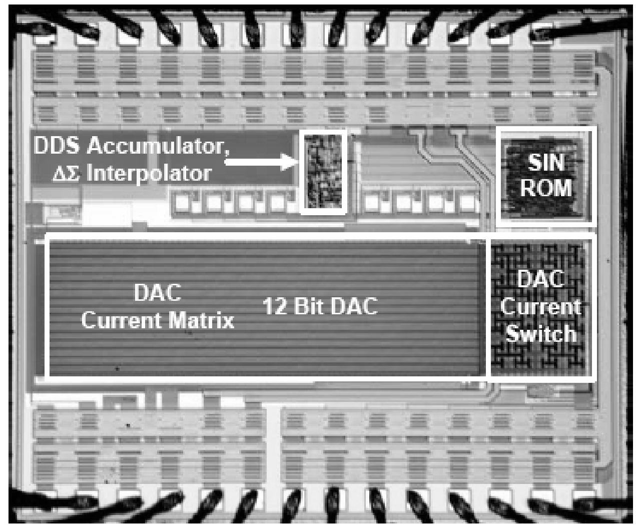

Fig. 8 Die photo of the DDFS prototype

Conclusion

This paper presents a DDFS with a 16-bit accumulator, a 4th-order single-stage pipelined delta-sigma interpolator and a 300MS/s 12-bit current-steering DAC based on Q^2 Random Walk switching scheme. The use of delta-sigma noise shaping can effectively reduce the phase truncation error and the ROM size while maintaining the high frequency tuning resolution. The presented DDFS is capable to reach the equivalent output noise of PLL based synthesizer or be used as a low noise fine tune reference in addition to the PLL synthesizer in a hybrid frequency synthesis.

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