Enhanced Resolution Jitter Testing Using Jitter Expansion

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Abstract

This paper presents a hardware jitter expansion technique to enable high-resolution jitter measurement of multi-GHz digital signals. To realize high-resolution timing analysis, the jitter is reconstructed on a low-speed signal and jitter measurements are made on this signal instead of the original high-speed signal. The reconstructed jitter on the low-speed signal occurs on a proportionately larger time-scale as opposed to the original jitter on the high-speed signal. Consequently, the jitter on the low-speed signal can be measured easily using conventional jitter measurement techniques and mapped back to its corresponding value relative to the high-speed signal. The approach allows one or two orders of magnitude smaller jitter values to be measured than standard jitter measurement techniques available today. The proposed hardware is easily implemented as a front-end to any existing jitter measurement system. Simulation data and hardware measurements are presented to prove the viability of the proposed scheme.

1. Introduction

The quest for high bandwidth wired and wireless data communication places significant demands on the performance of the underlying electronics. Precise cycle-to-cycle and periodic jitter performance is required from Gbps serial data communication circuitry for error free data communication. It is well understood that the data communication bit-error rate (BER) is directly related to the signal jitter value and can be predicted from measurements of the same [1]. However, to accurately measure jitter values down to 50 – 100 ps for a 1 GHz clock or 5 – 10 ps for a 10 GHz clock, very high bandwidth signal measurement devices are necessary. The bandwidth of a stand-alone device such as a time interval analyzer (TIA) or a real-time oscilloscope is currently limited to 6.25Gbps due to a maximum sampling rate capability of 40Gsps [2]. Even if higher sampling speed becomes possible in the future, the test measurement setup for wideband systems may be too expensive to be deployed in high volume production. Such instrumentation will be susceptible to signal interference, variations of the channel's characteristic impedance and inter-connect/cable noise in off-chip signals [3].

This paper presents a jitter expansion technique for overcoming the high sampling rate requirements for jitter measurement of high-speed signals while simultaneously alleviating the impact of induced noise on the integrity of the same. In the proposed jitter test approach, the jitter in a high-speed signal is reconstructed on a low-speed signal in such a way that the "equivalent phase noise" of the jitter on both signals is similar. However, as the transformed jitter occurs on a low-speed signal instead of on the original high-speed input signal, the reconstructed jitter is expanded significantly in the time domain. As an example let this expansion factor be 1000. Then a 10 psec RMS jitter value for a 1Gbps input signal can be reconstructed on a 1Mbps signal with 10 nsec RMS jitter. The expanded jitter of the 1 Mbps output signal, 1 nsec RMS value in this case, is 1000 times larger than the original jitter of the 1 Gbps signal.

In high volume manufacturing, simple circuitry on the tester loadboard (see Figure 1) can be designed to accomplish jitter expansion. The low-speed output of the jitter expansion circuit can be routed to an external tester for analysis without the attendant signal integrity problems that occur with transmission of very high speed signals. The expanded (reconstructed) jitter of the low speed signal can be analyzed with a conventional time interval analyzer (TIA) or a low-speed oscilloscope. The proposed jitter measurement approach has significant potential to offer the following benefits over existing jitter measurement techniques:

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(a) *High resolution and accuracy*: The proposed jitter measurement technique holds the promise of sub-picosecond jitter measurement capability for multi-Gbps signals without the expense of precision external test equipment.
(b) *Simplicity/robustness of jitter expansion circuitry*: The jitter expansion circuit is easy to implement and is robust to component variations and device nonlinearities.
(c) *Ability to calibrate for reference signal noise*: The proposed jitter measurement technique requires the use of a sine wave source with low phase noise value. In case a "perfect" source is not available, it is possible to calibrate for the phase noise of the reference signal (within reasonable bounds).

2. Related work

In [2], [4], a wideband low-noise ATE based method for measuring jitter in GHz signals is described. It is shown that the time-dependent phase deviation of a jittered (multi-GHz) signal from its ideal linear function of time is not affected by frequency translation. Hence, a jittered high-frequency signal can be mixed down to a lower frequency and sampled by lower frequency data converters than would be required for sampling the original signal. The authors propose a sequence of narrow band mixer down-converted measurements to reduce overall measurement noise. However, the method requires the use of a high performance mixer, a programmable VCO with -120dBc/Hz phase noise attenuation at 10 KHz frequency offset and a set of passive filters with low passband attenuation. These can be incorporated only into high-end tester instrumentation.

The method proposed in this paper uses the fact [2], [4] that phase deviation from the ideal (as a function of time) is preserved by frequency translation. However, the manner in which this principle is used in this paper is quite different. First, the proposed technique in this paper *does not use a mixer* for frequency translation. Hence, problems with mixer fidelity are avoided. Second, we *do not use a programmable VCO* but rather only a single measurement with a fixed-frequency reference signal. Hence, the jitter expansion circuit is *very simple and can be easily incorporated on the tester load board*. In the future, this may even lead on on-chip jitter measurement circuitry. Third, the output of the jitter expansion circuit is *a time-domain jittered signal with up to 1000X expanded jitter time scale (as opposed to frequency domain data that must be analyzed to extract jitter information)*.

The embedded timing analysis technique presented by Tabatabaei and Ivanov [5] uses an on-chip time-to-digital converter (TDC). D flip-flop based delay lines generate a trigger signal for the TDC which performs timing analysis for the signal of interest. However, the design complexity of the delay-lines results in die-area overhead [6]. Also, the jitter analysis capabilities are dependent on the performance of the time-to-digital conversion circuitry.

Sunter and Roy describe an on-chip digital jitter measurement technique [6] which is based on Huang and Cheng's on-chip short-time interval analysis [7]. An under-sampling latch in Huang and Cheng's technique uses a sampling trigger clock with a small frequency offset to that of the input data signal. The output of the coherent undersampling latch contains a beat frequency caused by the frequency offset. Thus, the time interval of the input data signal can be analyzed from the beat frequency signal at the latch output. Sunter and Roy used this coherent undersampling technique to perform high resolution jitter measurement. They focus on the fact that the latch output contains timing variation (jitter) originated from the input signal in the beat frequency. However, the undersampling latch falls into the sensitive node of the jitter measurement process [6] and applying a sampling clock externally is challenging [8], [9].

The proposed method utilizes the beat frequency which is similar to that of undersampling latch output. However, the manner in which the beat frequency is generated is different. First, the proposed test structure *does not have a high speed sampler* which is process sensitive. Second, *timing resolution of beat frequency is not limited* by the discrete nature of sampling. Third, we *do not use sampling clock* but rather one-tone sine reference signal.

3. Basic concepts: jitter expansion

The structure of the proposed jitter enhancement circuitry is depicted in Figure 1, and consists of three modules: a voltage combiner, an envelope detector and a comparator. A high-frequency jittered signal ((a), whose jitter value is to be measured) of fundamental frequency f_d and a reference sinusoid f_r (b) from a reference oscillator (VCO) are summed using a voltage

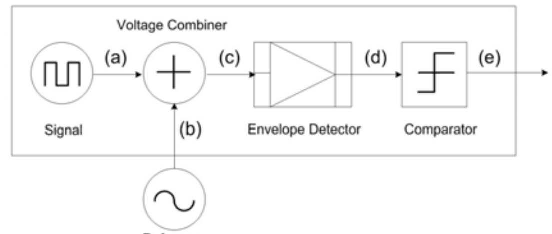

Figure 1. Proposed structure for jitter expansion.

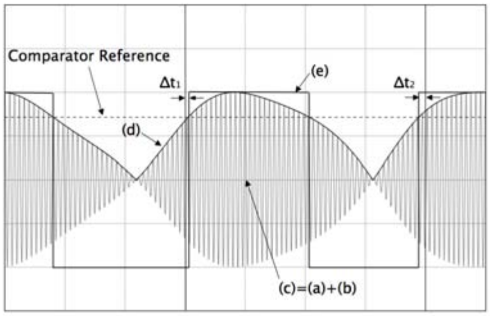

Figure 2. Waveforms of the functional nodes in Figure 1 are depicted. Δt's denote the reconstructed (expanded) jitter at the output of the proposed structure.

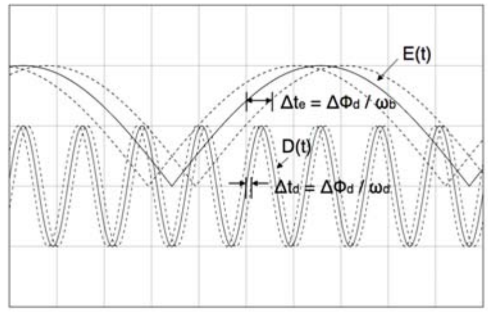

Figure 3. The same phase noise both on the high speed input signal D(t) and the low frequency envelope function E(t) show the significance difference in level crossing time.

combiner. The voltage combiner output (c) is fed to the envelope detector to extract the envelope of the combined two-tone signal (d). The envelope detector consists of a diode and a R-C components filtering out high-frequency carriers. The frequency f_b is the beat frequency of the two signals (a) and (b) in Figure 1 and the function of the envelope detector is to “pass” the beat frequency f_b, while attenuating the signals f_d and f_r.

As depicted by the signal (d) in Figure 2, the envelope function contains the original input signal jitter information. The envelope has the same phase noise as the signal fd and this maps onto a significantly larger jitter in the time domain of the signal (e) of Figure 1 as shown in Figure 2.

The output of the comparator is fed into logic circuitry for jitter analysis or measured directly by a TIA or digital oscilloscope. The comparator must modulate the input signal into a square wave without adding noise resulting in extra jitter. However, the operating speed of the comparator is low, so this problem is not a hard design problem.

4. Jitter in signal analysis

4.1. Phase noise at each functional nodes

In the following, we focus on the problem of detecting jitter in a clock signal as opposed to a data signal. The clock signal in fact, consists of an infinite number of odd harmonics of the fundamental tone. For ease of analysis and considering band-limitation of the signal in practice, we will assume that the input signal (whose jitter value is to be measured) is a single-tone sinusoid with added phase noise. Thus, *D(t)* with phase noise is modeled as a single tone sinusoid shown in Equation (1).

$$D(t) = \sum_{n=odd} (-1)^{(n-1)/2} \frac{A_d}{n} \cos\left(n\omega_d t + \Delta\phi_{d,n}(t)\right)$$
$$\approx A_d \cos\left(\omega_d t + \Delta\phi_d(t)\right) \qquad \textbf{(1)}$$

where A_d is the input signal amplitude and $\Delta\varphi_d = \Delta\varphi_{d,1}$ is the instantaneous input signal phase deviation. On the other hand, the VCO output generates the reference sine *R(t)* as given by,

$$R(t) = A_r \cos\left(\omega_r t + \Delta\phi_r(t)\right) \qquad \textbf{(2)}$$

where A_r is the reference signal amplitude and $\Delta\varphi_r$ is the instantaneous reference signal phase deviation. The output of the signal combiner which adds the signals *D(t)* and *R(t)* is given by Equation (3).

$$C(t) = A_d \cos\left(\omega_d t + \Delta\phi_d(t)\right) + A_r \cos\left(\omega_r t + \Delta\phi_r(t)\right) \qquad \textbf{(3)}$$

By tracking the envelope of the two-tone signal through the following envelope detector, the envelope function corresponding to Equation (4) which has the fundamental frequency term ω_b (= $\omega_d - \omega_r$) and its harmonics is extracted.

$$E(t) = \sqrt{A_d^{\,2} + A_r^{\,2} + 2A_d A_r \cos(\omega_b t + \Delta\phi_d(t) - \Delta\phi_r(t))} \qquad \textbf{(4)}$$

The corresponding comparator output is then derived as Equation 5 by applying a reference level (see Figure 2).

$$O(t) = \left[E(t) - \sqrt{A_d^{\,2} + A_r^{\,2}}\right]_{pulse} \qquad \textbf{(5)}$$

where the function $[]_{\text{pulse}}$ implies an ideal comparator that detects zero crossing points. Equation 4 and 5 imply that the envelope function of the two-tone signal preserves the phase noise of the original high-speed input signal $\Delta\varphi_d$ and of the reference signal $\Delta\varphi_r$ as well, and the comparator output signal has the corresponding jitter values. Assuming that $\Delta\varphi_r << \Delta\varphi_d$, the $\Delta\varphi_d$ component of phase noise at the lower frequency ω_b (compared to ω_d), results in a large value of jitter at the output of the comparator of Figure 1.

4.2. Jitter expansion factor: at-speed to down speed

We now study the at-speed input signal and the envelope signal in the time domain. The obtained envelope is compared against a fixed DC reference. If the original signal *D(t)* had been fed directly to the comparator, the time difference between consecutive clock edge transitions at the output of the comparator would be given by Equation (6). However, the observed time difference between consecutive clock edges when the envelope of Equation (4) is fed to the comparator is given by Equation (7).

$$\Delta t_d(t) = -\frac{\Delta\phi_d(t)}{\omega_d} \quad \textbf{(6)}$$

$$\Delta t_e(t) = -\frac{\Delta\phi_d(t) - \Delta\phi_r(t)}{\omega_b} \quad \textbf{(7)}$$

In Equation (6), the timing deviation $\Delta t_d(t)$ is the result of the phase deviation $\Delta\varphi_d(t)$ in the at-speed frequency ω_d. On the other hand, the timing deviation $\Delta t_e(t)$ in Equation (7) for the envelope signal is caused by the phase deviation $(\Delta\varphi_d(t) - \Delta\varphi_r(t))$ in the beat frequency ω_b. Assuming the reference signal phase noise $\Delta\varphi_r(t)$ is small enough, the difference between Equation (6) and Equation (7) is the operating frequency ω_d versus ω_b. Hence, the jitter of the comparator output signal *O(t)* is time-expanded by a factor of ω_d / ω_b from the jitter of the original input signal *D(t)* (see Figure 3).

5. Practical consideration

5.1. Design margin of the envelope detector

The envelope detector is the node which falls into attention regarding the circuit design margin and performance variation because the operating frequency is within RF region, while the following block of the comparator is operated must lower frequency band. The parameters of the envelope detector; e.g. the frequency-dependency of the operation and the attack/release time constant, affect the performance to track the envelope of signals. It is important to note that the envelope detector operation does not depend on detailed transistor characteristics. Rather, it follows the large-signal transconductance. As one of the large-signal parameters, the time constant of discharging capacitor in the envelope detector must be properly defined at the circuit design level since the time constant determines the envelope tracking speed. The advantage using envelope detector is that the possible time constant values are relatively wide because of the frequency gap between the at-speed input signal (multi-GHz) and the beat-frequency at the output (several MHz) shown as $1/f_d << \tau << 1/f_b$. Thus good design margin is present on the high-frequency operation block in design.

Frequency-independent operation of the envelope detector is required for many audio applications. However, flat frequency response within desired frequency range is not mandatory for the proposed jitter expansion technique. Since the relevant parameter for jitter detection is the phase of the signal, a non-flat frequency response does not directly affect the jitter detection performance. However, we designed circuits to retain a flat response within the interested frequency range for optimized performance.

5.2. Imperfect reference: noise compensation

It was assumed that the phase noise of the reference signal is small enough in Section IV. However, a perfect external reference signal is hardly equipped in high volume production. Hence, test performance degradation caused by noisy reference signal must be considered. In Equation (4) and (5), the phase deviations of the input signal and the reference signal, $\Delta\varphi_d$ and $\Delta\varphi_r$ respectively, are well denoted without unexpected parameters.

To calibrate for the reference noise effect, we assume that the reference noise is uncorrelated to the input signal noise. To make the assumption reasonable, the reference signal in the following hardware experiments was generated from the individual oscillator. In Equation (8), the standard deviation of the reconstructed timing jitter and the reference sine timing jitter, $\sigma[\Delta t_e]$ and $\sigma[\Delta t_r]$ respectively, are values which can be measured from experiment. The desired value $\sigma[\Delta t_d]$: the standard deviation of timing jitter of the original input signal, is then calculated where the reference phase noise effect on jitter testing is calibrated out. Thus, in case a "perfect" source is not available, it is possible to calibrate for the phase noise of the reference signal (within reasonable bounds) to improve overall jitter measurement capability of the hardware.

$$\sigma[\Delta t_e] = \sqrt{\left(\sigma[\Delta t_d]\frac{\omega_d}{\omega_b}\right)^2 + \left(\sigma[\Delta t_r]\frac{\omega_r}{\omega_b}\right)^2} \quad (8)$$

6. Simulation results

To elaborate the equations described in Section IV, waveforms on each of functional nodes in the proposed test configuration were evaluated in a MATLAB simulation. Jittered input signal *D(t)* was represented as 1GHz clock with the corresponding phase noise and the reference sine *R(t)* was given by perfect sine in the frequency of 0.9GHz (high beat-frequency of 100MHz was selected to reduce the simulation time). The output waveform from the comparator was then derived using transient simulation. To compare jitter value of the input signal *D(t)* to that of the comparator output *O(t)*, jitter histograms for both the signals are compared to each other.

A simulation result for wideband(<500MHz) random jitter is shown in Figure 4: (a) histogram from the actual input jitter for a sample size of 20000 edges and (b) histogram from the reconstructed output jitter for a sample size of 2000 edges. The programmable jitter generation is based on pseudorandom values drawn from a normal distribution. Assuming that jitter histogram follows the normal distribution, similarities between two distributions is proved by comparing their variances. Applied input jitter had variance 2.317e+01 psec and output jitter variance 2.267e+03 psec was measured. With jitter expanding factor of 10, actual jitter distribution from the input is similar to expanded jitter distribution in the limited samples.

To show jitter expansion performance for deterministic and random jitter, deterministic (1MHz) and random (<500MHz) jitter components were applied simultaneously on the input source. Figure 5 shows the simulation results from a combination of random and deterministic effects: (a) histogram from the actual input jitter for 20000 samples and (b) histogram from the reconstructed output jitter for 2000 samples. Because a distribution from a combination of random and deterministic jitter is not normal, cumulative distribution functions (CDFs) were derived from each jitter histogram. Kolmogorov-Smirnov test was then performed on the CDFs of the input and output jitter to see similarities between non-normal distributions of (a) and (b). This simple compatibility test shows input and output jitter distributions are similar to each other with the maximum vertical deviation 0.08 and a scaling of 10.

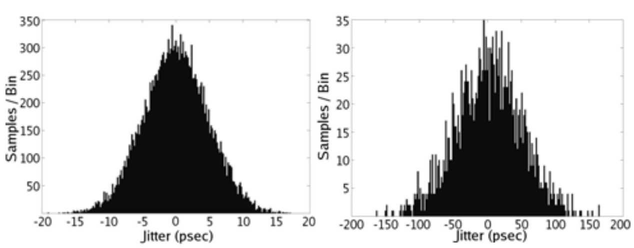

Figure 4. Wideband (<500MHz) random jitter is applied: (a) jitter histogram from 1GHz jittered clock and (b) histogram from the reconstructed jitter in 100MHz comparator output.

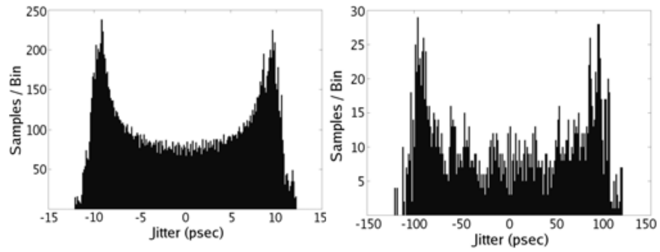

Figure 5. Wideband (<500MHz)) random jitter and 1MHz deterministic jitter are applied: (a) jitter histogram from 1GHz jittered clock and (b) histogram from the reconstructed jitter in 100MHz comparator output.

7. Hardware validation

The proposed test structure was validated on hardware. Figure 6 shows a picture of the test setup. The test accuracy was evaluated on two jitter types: deterministic and random, applying incremental jitter value at the input. In order to construct equivalent phase noise of the jitter at the input source, phase modulation of a signal generator (Agilent E4432B) was used. Another signal generator (HP 8648D) was used as a single tone sinusoidal reference of 2.399GHz frequency (the beat frequency of 1MHz in this case). A digital oscilloscope (Agilent DCA-J 86100C triggered by Agilent 81133A) was utilized at the output to measure jitter value of the output signal.

Increasing deterministic phase noise values (0.00Rad.(RMS) to 1.00Rad.(RMS)) were applied to the 2.4GHz input signal to be measured and the low-speed output of the jitter expansion structure was measured on the oscilloscope. Figure 7 shows the plot with the actual input jitter value(RMS) of the input signal versus that of the measured 1MHz(beat-frequency) output signal with a scaling of 2400 which is the observed expansion factor of the test structure. As seen from Figure 7 (a), the relation between actual input jitter and measured output jitter is approximately linear, showing a high degree of dependency. After noise compensation according to Equation (8), the reference noise effect was calibrated as shown in Figure 7 (b).

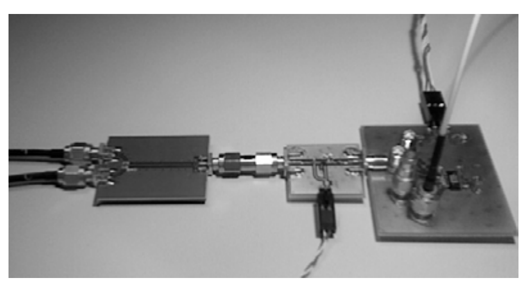

Figure 6. Hardware evaluation of the proposed structure.

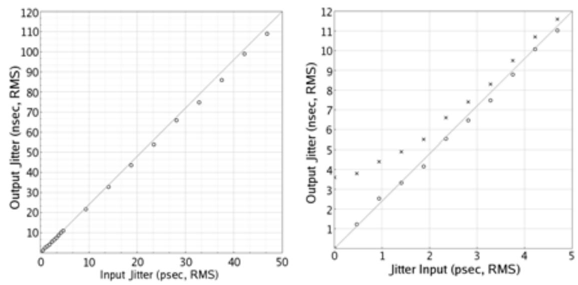

Figure 7. Deterministic jitter (50kHz) is applied: (a) input jitter versus reconstructed jitter at the output after calibration, (b) before(denoted by cross) and after(denoted by circle) calibration for the reference noise.

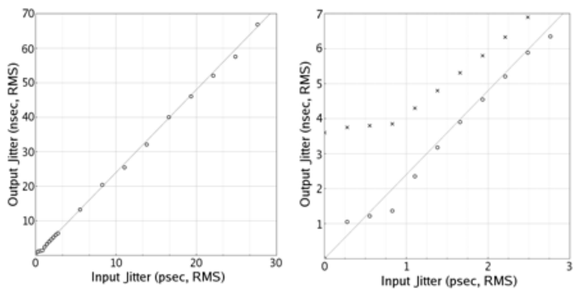

Figure 8. Random jitter (<50kHz) is applied: (a) input jitter versus reconstructed jitter at the output after calibration, (b) Before(denoted by cross) and after(denoted by circle) calibration for the reference noise.

In the same test setup, incremental values of random phase noise were applied to the input signal. As seen from Figure 8, two quantities of actual input jitter and measured output jitter are proportional for randomly generated jitter. After reference noise is calibrated out (denoted by cross), the proposed test structure shows abilities for picosecond(or better) accuracy timing analysis for two types of jitter.

8. Conclusion

In this paper, a hardware jitter expansion technique as a front-end to any existing jitter measurement setup is proposed. The relation between the actual input jitter and the reconstructed jitter at the output shows a high degree of dependency. The key advantages of the method proposed in this paper are high resolution and accuracy, simple and robust test structure and calibration ability for reference signal noise.

In the future, we will further conduct hardware validation, implementing the presented jitter expansion hardware and the following post-processing digital logic circuit on a chip to show the promise of on-chip jitter testing for multi-Gbps signals.

9. Acknowledgment

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