Growth of Vanadium on Silicon Substrates

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ABSTRACT

Vanadium has been grown on (111) oriented silicon substrates using the hydrogen reduction of VCl_4. The reaction kinetics related to the growth of the deposits has been investigated. V-Si diodes fabricated from the deposited vanadium on silicon samples were found to have a barrier height of 0.70 ± 0.04v in agreement with that theoretically predicted in other studies.

Recent interest in the chemical deposition of metals on semiconductor substrates has been stimulated by potential applications in the fabrication of diodes and metal-base transistors. Deposition of molybdenum on silicon has been reported by Casey *et al.* (1) and Lindmayer (2); the latter author reported that 100Å thick molybdenum layers on silicon were not single crystal. Crowell *et al.* (3) have reported deposition of polycrystalline tungsten films on silicon, germanium, and gallium arsenide substrates. The purpose of this paper is to present data on the growth of vanadium on silicon substrates and to study the feasibility of V-Si diode fabrication from these structures.

A schematic diagram of the deposition apparatus used is shown in Fig. 1. The deposition apparatus was the vertical reactor, RF-heated type, conventionally used for the hydrogen reduction of silicon tetrahalides (4). The VCl_4 was prepared by the reaction between vanadium and chlorine. The chlorine was passed over vanadium at 800°-1000°C. The chlorine was purified by passing it through graphite heated to 650°C. The VCl_4 was condensed at 0°C in a cold finger for subsequent controlled vaporization in a purified hydrogen flow. During deposition, hydrogen was passed over the VCl_4 at the rate of 0.5 l/min and another 4 l/min flow of hydrogen bypassed the cold finger and flowed into the reactor. The VCl_4 partial pressure was controlled by thermostating at temperatures from —15° to 25°C. The VCl_4 vapor pressure values used for calculating partial pressures of VCl_4 were obtained by extrapolating the data of Simons and Powell (5) below 39.5°C. It was assumed that the only significant compound formed from the $V\text{-}Cl_2$ reaction was VCl_4. The vanadium was obtained from Gallard-Schlesinger Chemical Corporation and was 99.9%. Silicon substrate samples were 1.5 ohm-cm, n-type single crystal wafers oriented in the (111) plane and were electrochemically polished. Over-all deposited thickness was determined by masking a portion of the substrate with a silicon chip and measuring the resulting step in the vanadium deposit with a Zeiss interference microscope. Vanadium was deposited with an over-all average thickness up to 10μ.

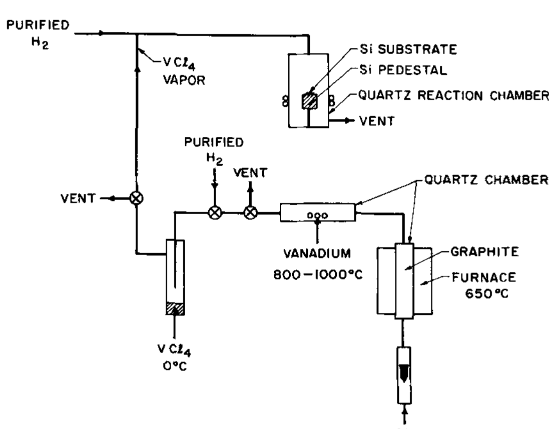

Fig. 1. Schematic diagram of apparatus

Variables affecting the deposition rate of vanadium which have been studied are the silicon substrate temperature and the partial pressure of VCl_4. The effect of temperature was studied between 1140° and 1300°C at a VCl_4 partial pressure of 0.2 Torr. For study of the variation of deposition rate with partial pressure variation, the VCl_4 was varied between 0.08 and 0.9 Torr, and silicon substrate samples were held at 1300°C. Figure 2 shows the variation of the vanadium deposition rate with temperature. The kinetic data for the deposition rate between 1140° and 1300°C could be fitted to an Arrhenius type equation

$$r = Ae^{-\Delta H_a/RT}$$

where ΔH_a, the apparent activation energy for the over-all reaction, was 72 ± 2 kcal/mole.

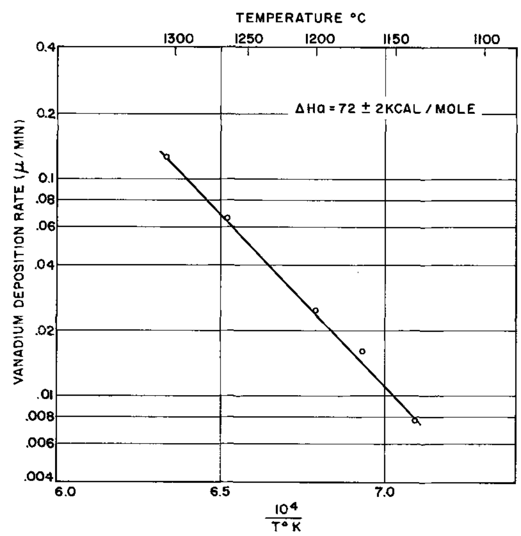

Fig. 2. Temperature dependence of vanadium deposition at 0.2 Torr VCl_4 pressure.

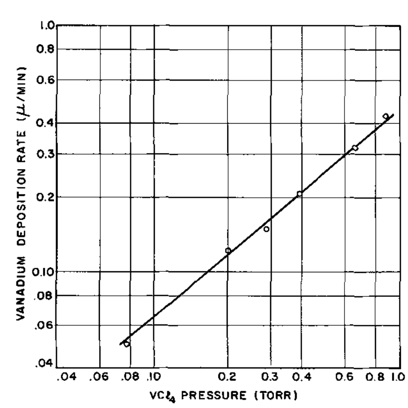

Fig. 3. Effect of VCl_4 partial pressure on deposition rate at 1300°C

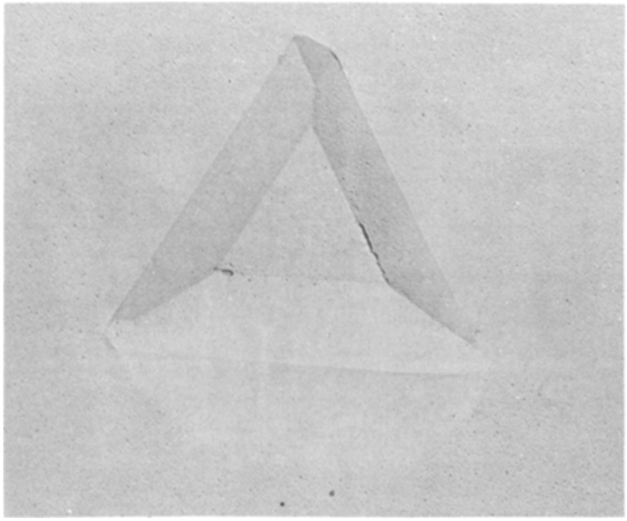

Fig. 4. Electron micrograph of deposited vanadium crystallite. Magnification 8000X.

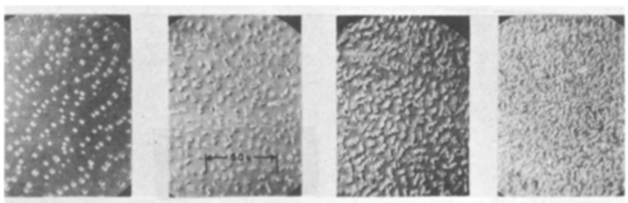

Fig. 5. Micrographs showing increasing density of deposited vanadium crystallites for average deposit thickness from 1 to 5μ (left to right).

Figure 3 shows the effect of the partial pressure of VCl_4 on the deposition rate of vanadium. Over the pressure range studied the deposition rate obeyed a relation of the type

$$r = kp^{n}{}_{VCl_4}$$

The slope of the deposition rate-pressure line in Fig. 3 gives a value of $n = 0.9$, indicating that the deposition reaction is close to first order. It can be assumed that the low partial pressures of VCl_4 used favor a heterogeneous reaction. Tyzack and England (7) have concluded that the following reduction reaction of VCl_2 to form vanadium is rate-controlling

$$VCl_2 + H_2 \rightarrow V + 2HCl$$

Their conclusion is apparently based on the increasing positive value of $\Delta G°$ with decreasing temperature below about 1250°C.

Vanadium crystal growth was observed to take place by island formation similar to that observed by Manasevit *et al.* (6) for epitaxial silicon growth on sapphire. The surface deposits were analyzed for vanadium by an electron probe microanalyzer. The electron probe used for these studies was a Microscan, manufactured by the Cambridge Instrument Company. This scanning type electron probe permitted two-dimension displays of the sample surface and showed the deposits to be vanadium particles or clusters. Transmission electron diffraction patterns obtained from vanadium deposited surfaces indicate that the vanadium crystallites are of the same (111) orientation as that of the silicon substrate and are single crystalline. No evidence of silicides was observed. Figure 4 shows a typical vanadium crystallite as viewed by electron microscopy. Optical microscopic examination of vanadium deposited surfaces showed that the deposits consisted of an array of discrete vanadium crystallites. Vanadium crystallite density varied with the over-all average depth of deposited vanadium. Figure 5 shows this density variation, for average depth of deposit from 1μ increasing to 5μ.

Vanadium-silicon diodes were made from vanadium which was deposited approximately 10μ thick and which covered approximately 80% of the silicon surfaces. The diodes were made using the procedure previously described for tungsten-silicon diodes (3): Au-Sb ohmic contacts were alloyed to the back surface of the silicon substrates at 370°C, 10 mil diameter gold dots were evaporated on the deposited vanadium surface, and samples were etched in 10:1 HNO_3:HF to remove vanadium from the unmasked areas. Because the substrate temperature during vanadium deposition is 100°C lower than the V-Si eutectic temperature, and diffraction studies did not show silicide formation, the junction is believed to be of the nonalloyed type. Current-voltage and capacitance-voltage measurements were used to investigate the V-Si diode characteristics. Typical forward current density-voltage plots are shown in Fig. 6. These curves can be fitted by the diode equation (8)

$$J = J_s[e^{(qV_a/nkT)} - 1]$$

where V_a is the voltage applied across the junction, n is an empirical constant, and J_s is the saturation current density. The value of n obtained from Fig. 6 is about 1.1 for current densities ranging from 10^{-4} to

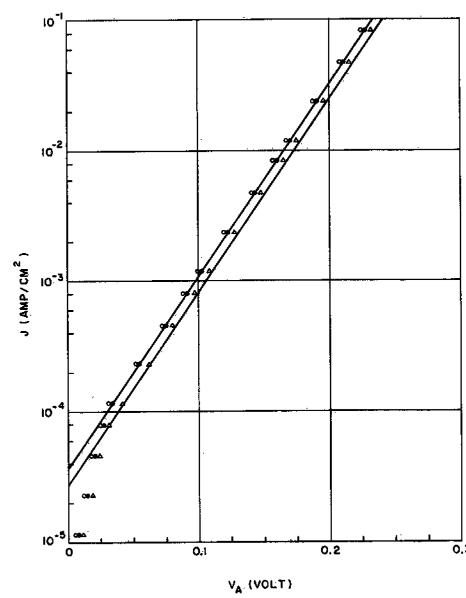

Fig. 6. Forward current-voltage characteristics for V-Si diodes

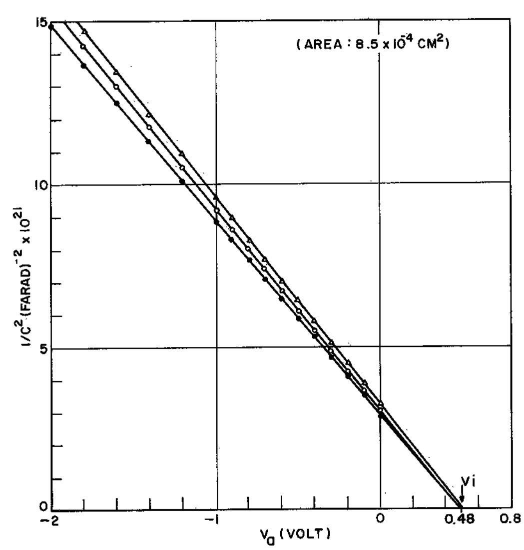

Fig. 7. Capacitance-voltage characteristics for V-Si diodes

10^{-1} amp/cm^2. The value of J_s is $(3.0\text{-}3.6)\times10^{-5}$ amp/cm^2. The barrier height, Φ_B, was found to be 0.70 ± 0.04v based on the assumption that the Richardson equation

$$J_s = A^* T^2 e^{(-q\Phi_B/kT)}$$

can be used to relate the barrier height, Φ_B, and J_s (3). A theoretical value of A^*, 258 amp/cm^2/K^2, has been used (9). The J_s is the sum of the currents for V-Si and Au-Si diodes, because, as discussed above, approximately 80% of the areas are covered by vanadium and 20% covered by gold. However, the barrier height of Au-Si diode is about 0.80v (10) which is 0.1v higher than the presently measured barrier height. The correction in Φ_B of V-Si diode is less than 0.025v. The reverse characteristics of the diodes were qualitatively consistent with the diode equation with a reverse current density of the order of 10 ma/cm^2 at 10v.

Capacitance-voltage measurements on V-Si diodes are shown in Fig. 7. The doping level, N_D, determined from resistivity measurement, was 3.8×10^{15} cm^{-3}, and from the slope of the $1/C^2$ *vs.* V_a plot 4.3×10^{15} cm^{-3}. The barrier height can also be determined from the data in Fig. 7 by use of the equation (3, 11)

$$\Phi_B = V_i + V_f + kT/q - \Delta\Phi$$

where V_i is the voltage intercept, 0.48 ± 0.04v, V_f, the depth of the Fermi level below the conduction band, is 0.288v for 1.5 ohm-cm, n-type silicon, and $\Delta\Phi$ is the image force barrier lowering (12), approximately 15 mv for V-Si diodes. Thus Φ_B was found to be 0.71 ± 0.04v. Since the measured capacitance over the voltage range will only be affected by the combined diode system to less than 2%, the correction for Φ_B of V-Si diode is again of the order of 0.025v.

The consistency of the value of the barrier height obtained from the above measurements and the fact that n is close to unity and $1/C^2$ is linearly dependent on V_a indicate the existence of a Schottky junction. The barrier height obtained in this study has been found to be in reasonable agreement with that predicted theoretically by Cowley and Sze (13) based on the assumptions that the contact between the metal and the semiconductor has an interfacial layer of the order of atomic dimension and the surface state density at the interface is a property only of the semiconductor surface.

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Any discussion of this paper will appear in a Discussion Section to be published in the June 1967 JOURNAL.

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Selective Epitaxial Deposition of Gallium Arsenide in Holes

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ABSTRACT

Epitaxial deposition of gallium arsenide in holes etched into gallium arsenide substrates was investigated. Single crystal deposits with excellent surfaces were obtained. The effect of substrate orientation on the degree of lateral overgrowth above the substrate surface was studied. Depositions in {100} oriented substrates produce faceted deposits, whose upper surfaces are several microns above the substrate surface. Epitaxial hole deposits with surfaces level with or nearly level with the substrate surface are obtained with accurately oriented {111}-B substrates.

The importance of selective epitaxial deposition has long been realized in integrated circuit technology. Generally the technique involves epitaxial deposition onto the substrate only in certain areas which are exposed by windows in a protective film (*e.g.*, SiO_2). This technique has been investigated both for silicon (1) and gallium arsenide (2) substrates.

Extension of the technique to include selective depositions in substrate holes has not been widely reported. The investigations which have been reported, such as the recent studies by Jackson (3), have been directed toward the epitaxial deposition of silicon in holes etched into a silicon substrate. However, the selective deposition of gallium arsenide in substrate holes has been generally neglected.

Due to the availability of semi-insulating gallium arsenide, the three-dimensional integrated circuit or functional electronic block has become increasingly promising (4). In view of this as well as the accelerating importance of integrated circuits in general, an investigation of the nature of epitaxial deposition of GaAs in substrate holes was undertaken.

Experimental

Both semi-insulating (Cr doped) and n-type (Te doped) gallium arsenide substrates were employed. The crystals were x-ray oriented and cut into 25 mil thick slices, which were then polished with a sodium hypochlorite solution according to the method of Reisman and Rohr (5). Either {100} or {111}-B surfaces